Germanium Photodetectors on Amorphous Substrates for Electronic-Photonic Integration

by

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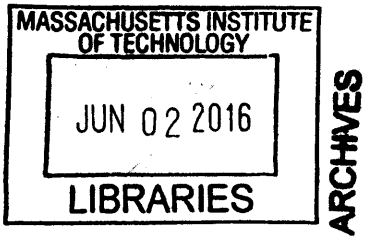

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Abstract

Silicon photonics has emerged as a leading technology to overcome the bandwidth and energy efficiency bottlenecks of standard metal interconnects. Integration of photonics in the back-end-of-line (BEOL) of a standard CMOS process enables the advantages of optical interconnects while benefiting from the low cost of monolithic integration. However, processing in the BEOL requires device fabrication on amorphous substrates, and constrains processing to $\leq$450 °C. In this thesis, a germanium photodetector is fabricated while adhering to these processing constraints in order to demonstrate a proof of concept for BEOL integration.

In order to obtain high quality active material, crystalline Ge was grown on SiO_2 by implementing selective deposition in geometrically confined channels. The emerging Ge grains were coalesced to fill a lithographically defined trench, forming the active area of a photodetector. The Ge was measured to have a significant tensile strain of 0.5 %, which was caused by thermal expansion mismatch with the substrate, and concentrated by small voids from imperfect coalescence. The associated resolved shear stress was determined to be below the critical resolved shear stress, verifying that dislocation generation does not occur in this material. The strain was shown to increase the absorption of Ge at long wavelengths, allowing for implementation along the entire telecom window.

A Schottky barrier to *p*-type Ge was developed by the addition of a 1 nm tunneling Al_2O_3 layer between an Al/Ge metal contact. This successfully de-pinned the Fermi level, creating a barrier height of 0.46 eV. The Schottky contacts enabled the fabrication of metal-semiconductor-metal (MSM) photodetectors on standard epitaxial Ge with state-of-the-art dark current densities of 2.1×10^{-2} A cm^{-2}. Gain was observed in these photodetectors, with internal quantum efficiencies (IQE) of 405 %. MSM detectors were also made using Ge on SiO_2, exhibiting an IQE of 370 %. This is the first demonstration of IQE >100 % in a Ge MSM or *pin* photodetector and proves the feasibility of making high performance active photonic devices while adhering to BEOL processing constraints.

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Finishing this thesis was more challenging than I expected it would be when I started at MIT nearly six years ago. I doubt I would have been able to complete my PhD if it were not for a tremendous amount of help along the way.

My two advisors, Kim and Jurgen have both helped guide me through this entire process. There were some challenges associated with having two advisors. At times I was pulled in different directions as Kim was always more interested in materials development and analysis, while Jurgen was always more interested in final device performance. Ultimately, it was in my benefit to constantly have both perspectives pushing me to have a well-rounded project. It seems as if there is nothing that Kim does not know, and Jurgen has always been available when I knock on his door at a random time seeking his help. They were both crucial to my work in different ways.

I had a tremendous amount of help from all of the EMAT students. They were always willing to discuss results and help in any way they could. Kevin McComber's work really motivated this entire thesis by demonstrating the method for growing crystalline Ge on amorphous substrates. He also took two full days to walk me though the process of how to do it in the lab and how to use the UHVCVD. Rodolfo Camacho was instrumental in teaching me how to use and maintain the UHV. Yan Cai is brilliant, hard working, humble about her work, and always willing to help me when I asked for it. It is always entertaining talking with Corentin. He thinks about science in a very mathematical way (which is very different from the way I think) and he enjoys talking politics and is not afraid to speak his mind. I appreciate both of these characteristics. Brian Albert and I worked very closely for the past two years and I am grateful for how much he helped me in the lab, with TA'ing Kim's class, and with general concerns with our research. Neil Patel is finishing his thesis within two weeks of me and was a part of the group the entire time I was. Between our trip to Japan together to commiserating about the challenges of finishing up together, he has made my time in the group much more enjoyable.

I also have to thank the entire Fitzgerald group. They essentially took me in as a

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Chapter 1

Introduction

The entire field of electrical interconnection is reaching a bottleneck. In order to keep up with Moore's Law, device dimensions continue to shrink in order to allow for denser integration of transistors in microprocessors [1]. However, as the feature size of silicon complementary metal oxide semiconductor (CMOS) transistors continue to shrink, the industry is obtaining diminishing returns. One of the main limitations to perpetual progression of computing power is the limitations imposed by the interconnects. As features sizes continue to decrease, microprocessors suffer from increased interconnect delay and increased power consumption of interconnects, which limit the ultimate performance and energy efficiency of these units.

Metal interconnects have become increasingly complex as device dimensions continue to shrink within integrated circuits. Figure 1-1 shows an example of the metal interconnect stack in one of Intel's Broadwell processors in the 14 nm node. As the size of the electronic devices continue to shrink, the size of the metal interconnects must also shrink. However, this creates an increased RC delay due to increased resistance from smaller metal cross-sections. Once feature sizes reached 180 nm line-widths, the interconnect delay began dominating the total system delay [3, 4]. The reduced line-widths also create an increased problem with heat dissipation, due to Joule heating, caused by increased electrical resistance. By the 130 nm node, interconnections

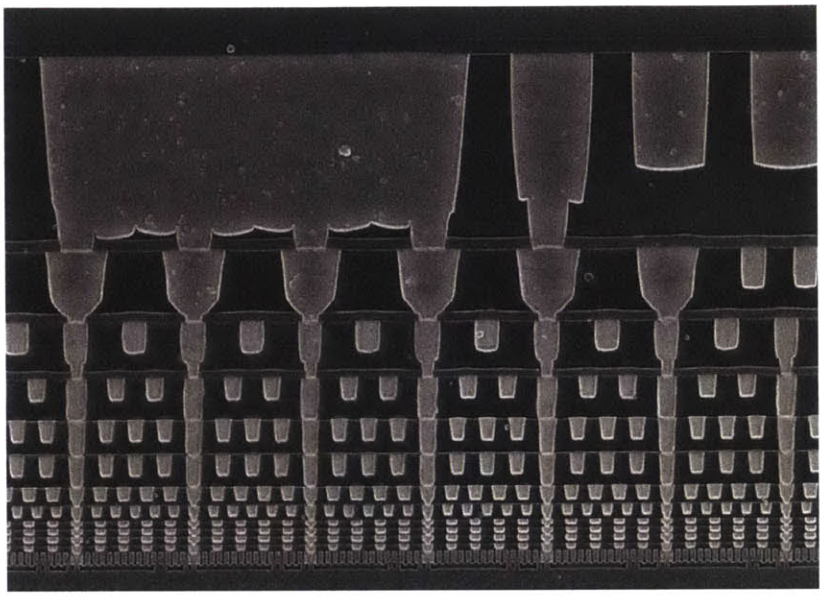


Figure 1-1: An example of a cross-sectional view of a 12 level interconnect stack from a 14 nm generation Intel Broadwell Processor. The small metal layers on the bottom are the local interconnects and the large metal layers on top are the global interconnects. From [2].

were already consuming 50 % of the total microprocessor power [5]. For context, this means that in the United States, server interconnects consumed more power than all solar power that was generated within the United States in 2007 [6]. The associated electricity use is growing at a rate of 12 % to 17 % per year [7]. The International Technology Roadmap for Semiconductors (ITRS) states that "power management is now the primary issue across most application segments" [8]. In addition, metal interconnects become limited by the Skin Effect at high bandwidths. As bandwidths increase, the electrical signal travels at the surface of the metal, thereby reducing the effective wire cross-sectional area. This increases the resistance of metal interconnect, additionally increasing Joule heating and power consumption. The combination of these factors leads to a limit in the benefits that metal interconnects can attain with increasing data rates and decreasing feature sizes. The recent enhancements, in bandwidth of metal interconnects, have come at the expense of increased latency and increased power consumption [9]. A promising way to overcome these problems is the

by the introduction of photonic interconnects.

Photonic interconnects can solve the problem of heat dissipation due to the fact that photons do not generate heat while they travel through waveguides. Optical fibers have a very high data capacity, and can transmit data at much higher bandwidths than metal interconnects. Another benefit of photonic interconnects is the ability for high levels of multiplexing. With optical interconnects, multiple discrete signals can be transmitted at different wavelengths along a single waveguide, without interacting with each other. This is called wavelength division multiplexing (WDM) and allows for much more data to be transmitted though a single interconnect.

Optical communication has already proved its potential via the introduction of optical fiber systems. This paradigm shift to optical systems has yielded dramatically increased bandwidths. Optical communication is already widespread in telecom types of applications in which high data rates are required over long distances. This is due to the reasons listed above, namely the low loss and high bandwidths of optical fiber systems.

1.1 Silicon Photonics

Electronic interconnects are struggling to continue to increase bandwidths while maintaining low power consumption. It is in the combination of these two limitations that photonic interconnects show their inherent benefits. Optical interconnects have the potential to increase the interconnect density, increasing the bandwidth, while simultaneously reducing the interconnect energy. This is due to the fundamental physical differences between the two types of interconnections.

The bit rate that can be transmitted through an electrical interconnect is limited by the resistive losses of the metal line. Due to metal resistive losses, in order to transmit high data rates over long distances, repeater amplifiers are required to maintain signal integrity. The total bandwidth that can be transmitted through a given cross-

sectional area, known as the bandwidth density, of metal wire is inherently limited. The maximum bandwidth that can be transmitted through a metal interconnect (B) is given by [10]:

$$B \leq B_0 \frac{A}{L^2} \tag{1.1}$$

where:

B = Maximum Bandwidth of a Metal Interconnect
B_0 = 10^{16} bit/s
A = Cross-Sectional Area of the Wire
L = Length of the Interconnect

For a given interconnect distance, it is impossible to increase the maximum bandwidth of the line without increasing the cross-sectional area of the line, which therefore decreases the bandwidth density. On the other hand, photonic interconnects do not suffer from resistive losses. This means that they can transmit much higher bandwidths over long distances, and within a limited cross-sectional area. In addition, different wavelengths of light do not exhibit cross-talk with each other and hence, multiple signals can be transmitted down the same interconnection line, using wavelength division multiplexing, to further increase the bandwidth density.

In addition to the bandwidth density benefits of optical interconnects, there may also be energy benefits. The drawback with electrical interconnections is that the entire interconnection line must be charged to the signaling voltage for each bit to be transmitted. The energy per bit for an electrical interconnection is given by the energy required to charge the interconnect up to the signaling voltage. In this case, the metal interconnect can be considered as a capacitor and the energy requirement per bit is as follows:

$$E_e \geq C_l V_s^2 \tag{1.2}$$

where:

E_e = Energy Per Bit for an Electrical Interconnect
C_l = Capacitance of the Metal Line
V_s = Signaling Voltage

The capacitance of the line is approximately a constant for a well-designed line and is equal to $\sim 2\,\mathrm{pF\,cm^{-1}}$ [10]. Therefore, reducing the signaling voltage, V_s, is the only way to reduce energy, per bit, of an electrical interconnection line. In contrast, the energy consumption per bit of optical interconnection is determined by completely different physics. In order to transmit an optical signal, there is no need to electrically charge the entire interconnection to the signaling voltage. Instead, the energy per bit is dominated by energy required to charge and discharge the photodetector capacitance, C_d, and the signaling voltage, V_s, which the link is electrically connected to. The total energy per bit of a photonic interconnect, E_p, is given by:

$$E_p \geq C_d V_s \frac{\hbar\omega}{q} \tag{1.3}$$

where:

E_p = Energy Per Bit for a Photonic Interconnect
C_d = Capacitance of the Photodetector
V_s = Signaling Voltage
$\hbar\omega$ = Photon Energy
q = Elementary Charge

In order for the photonic link to require less energy per bit, the charge in the photodetector must be less than the charge required to bring the metal line up to the signaling voltage. Therefore, must be achieved. This is assuming the external quantum efficiency of the photodetector is unity, and neglecting additional transmission losses in the photonic link. If it is assumed that a wavelength of 1.55 µm is used in the photonic link, . In comparison, signaling voltages in electrical interconnects can be as low as 0.1 V, or less [6]. Consequently, in order for photonic links to consume less energy than electrical links the relation must be satisfied, with the detector capacitance

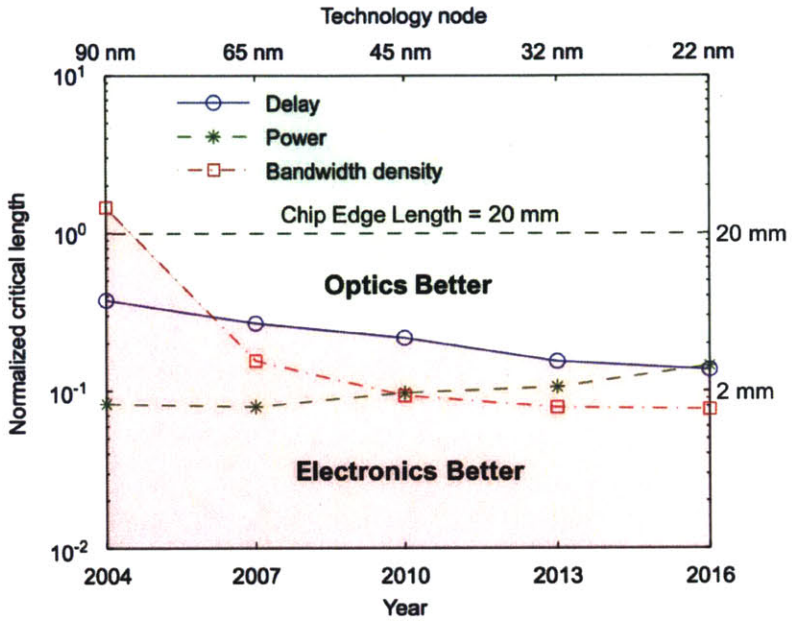


Figure 1-2: The critical length, beyond which it is advantageous to implement optical interconnects over electrical interconnects. The length has been normalized to the total chip length. From [13].

approximately an order of magnitude lower than the electrical line capacitance. The capacitance of the line increases linearly for the electrical case, while the detector capacitance remains constant for a given design. Therefore, there is a cross-over length, above which photonic links become more energy efficient than electrical interconnects. Neglecting losses in the waveguides, and energy lost in electrical to optical conversion, this cross-over length can be as short as 50 µm [6]. Other studies yield higher cross-over lengths with values in the several millimeter to ~15 mm range [11, 12].

In addition, there is a cross-over length in terms of delay. When the signal propagates in a metal interconnect, the delay scales with the RC time constant, which scales with length (since capacitance increases with length). For optical data transmission, there is some delay associated with modulators, detectors, and amplification. However, these do not scale with length. The remainder of the delay is associated with the speed of light for the signal to propagate from the source to the destination.

Therefore, there is a cross-over in terms of delay as well. This cross-over length is plotted for power, delay, and bandwidth density as a function on time in Figure 1-2. The cross-over length is a function of technology node (time). By the 22 nm node, this cross-over length is approximately 10 % of the total chip length. Therefore, if a signal must be transmitted further than 10 % of the chip length, then it is advantageous to transmit the data optically as opposed to electrically. Therefore, optical interconnects are ideal for long distance global interconnects within a single chip. The replacement of global interconnects with optical interconnects in place of metal will yield decreased delay, decreased power consumption, and increased bandwidth density.

1.2 Back End of Line Photonics

There are four main components that make up a typical optical interconnect: a light source, a modulator, a waveguide, and a detector. The light source is the source of the photons. The modulator is a device that encodes the digital signal by effectively switching the light on and off. The waveguide is medium in which the light travels, and directs the light along a given path. The detector converts the optical signal back into an electrical signal. Each of these discrete devices have already been independently demonstrated and each of them are completely compatible with standard CMOS processing constraints [14–17]. Previous efforts have already demonstrated germanium based *p-i-n* heterojunction diodes that can be used as electro-absorption modulators and detectors [15,16]. These devices show a lot of promise as the key devices in optical interconnects. However, in comparison to the electronic devices, these devices are very large. They may range in size, but modulators and detectors are in the range of 50 to 80 microns long and 0.5 to 1 micron wide for germanium-silicon active regions. This is orders of magnitude larger than electrical devices, since electrical device feature sizes are in the tens of nanometers size range. Therefore, the introduction of photonic devices will consume a lot of valuable real estate on the silicon wafer.

In order to follow Moore's law of increasing transistor counts, there is no room to put such large photonic devices onto the silicon substrate. A solution to this problem is to introduce three-dimensional integration of the photonic devices. In order to allow transistor counts to continue to increase, the photonic devices need to be taken off of the substrate and integrated in a level above the electronics level, in the back-end-of-line (BEOL). This would introduce all of the benefits of the optical interconnect, without sacrificing any of the valuable real estate on the crystalline silicon wafer. In addition, the initial goal of photonic interconnects is to replace electrical global interconnects. Global interconnects are located at the top of the interconnect stack, furthest from the substrate. Therefore, placing the photonic interconnects high within the interconnect stack reduces the architectural modifications that must be adopted for the integration of photonic interconnects. BEOL integration of photonics is considered valuable, yet challenging [18–22].

The electrical and optical properties of photonic devices are very dependent on their crystalline quality. Ideally, photonic devices have a single-crystalline active region. Grain boundaries and defects can increase dark currents, induce optical scattering, act as carrier recombination centers, and decrease the overall performance of these devices [23–25]. In order to fabricate single crystal devices with low levels of defects and contamination, the devices are typically grown on the substrate via ultra-high vacuum chemical vapor deposition (UHVCVD). Germanium is typically grown at 600 °C to 700 °C and may be annealed at temperatures up to 900 °C in order to reduce the threading dislocation density [26–28]. An important aspect of this process is that the crystalline silicon substrate is used to seed epitaxial growth of Ge films.

Germanium has emerged as an excellent candidate for the active region in active optoelectronic devices [29,30]. The direct bandgap of Ge, 0.8 eV, corresponds with an optical wavelength of 1.55 um, which is the wavelength that has the lowest absorption loss in silicon dioxide [31]. At this wavelength, absorption losses in Si-core, SiO_2-clad waveguides can be neglected with respect to scattering losses [32, 33]. In addition

to having an appropriate bandgap, Ge has a high carrier mobility, with an electron mobility of $3900\,cm^2\,V^{-1}\,s^{-1}$ and a hole mobility of $1900\,cm^2\,V^{-1}\,s^{-1}$ approximately 4 times higher than the carrier mobilities in Si. In addition to the attractive material properties, Ge is completely CMOS compatible. Ge is already included in CMOS technology as a method to create strained Si transistors [34], and therefore Ge is fully compatible with integration into Si electronics and integrated circuits.

Although the Ge itself is fully compatible with Si integrated circuits, there are many significant processing challenges that arise when attempting to moving the germanium optoelectronic devices away from the crystalline substrate. When the devices are grown above the substrate, there is no longer a crystalline seed to grow Ge epitaxially. A completely new growth technique must be utilized in order to obtain large-grain Ge without a crystalline growth seed. In addition, Ge growth and annealing occurs at high temperatures. If the photonic devices are integrated above the electronics level, then the electronics and metal interconnects will already be fabricated. At high temperatures, there may be significant dopant diffusion and silicidation of metal contacts, thereby altering the performance of the electronics that have already been fabricated. Therefore, in order to preserve the electronic devices, processing temperatures must be kept below 450 °C. Therefore, the active region of the devices has to be grown at low temperature, without a crystalline seed.

A schematic of the proposed microprocessor architecture is shown in Figure 1-3. In the left schematic, the current front-end integration design is shown where the photonic devices are fabricated on the substrate along with the transistors. The schematic on the right side shows the proposed design, in which photonic devices integrated within the interconnect stack. This frees up the substrate to be used for dense integration of transistors, but also restricts the thermal budget allowed for photonic device fabrication to not exceed 450 °C. It also eliminates the potential for epitaxial growth on a crystalline substrate.

Recent research has proven a technique to grow good quality Ge without the

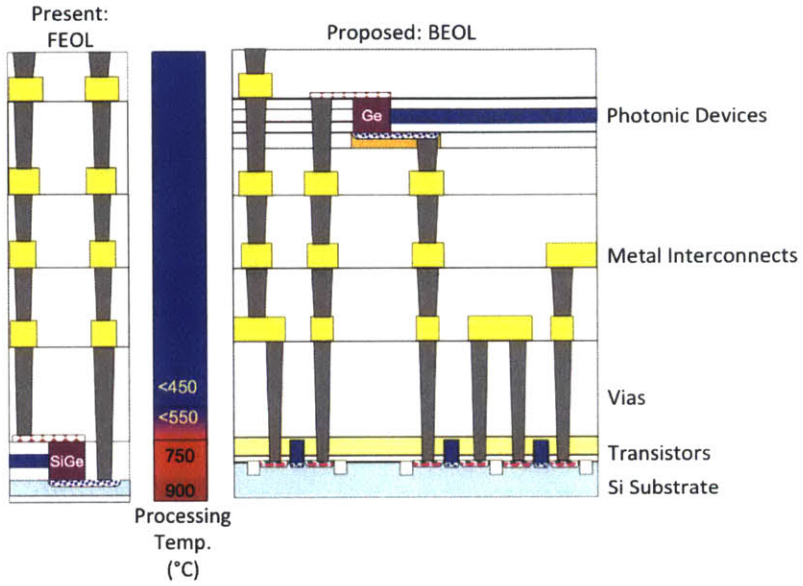


Figure 1-3: Cross-sectional schematic of a microprocessor interconnect stack. Current photonic devices (left) are fabricated in the front-end-of-line (FEOL), in which high-temperature epitaxy is permitted on the crystalline substrate. The right side shows the proposed architecture, in which photonic devices are integrated in the back-end-of-line (BEOL). Photonic devices are in purple and transistors are in blue. Processing temperatures, as a function of distance from the substrate, are shown in the scale on the left. From [19].

crystalline seed, at temperatures below 450 °C [21]. The technique is based on two-dimensional geometrically-confined lateral growth (2D GCLG). Essentially, the Ge is selectively nucleated on a small amorphous Si seed. Many different Ge crystals nucleate and grow in all different orientations. Some crystallographic orientations grow faster than others. The amorphous Si seed is recessed within a high aspect-ratio silicon dioxide channel, and therefore only the fastest growing Ge grains emerge from the channel. With the correct design of the channel dimensions, this technique can ensure that the only thing that emerges from the channel is a single grain of crystalline Ge. This growth technique has shown a viable proof of concept, however, it has never been used to fabricate actual devices.

In order to integrate optical interconnects into the back-end of a microprocessor, significant barriers must be achieved. Specifically, how to fabricate high quality Ge

for active regions of optoelectronic devices while adhering to back-end processing constraints, and how to develop this material into an actual device. This thesis addresses these topics by developing a germanium MSM photodetector which adheres to the back end processing constraints.

1.3 Thesis Outline

This thesis presents the path towards the proof of concept for the feasibility of active photonic devices that can be monolithically integrated with the back end of line of a standard CMOS process. The proposed proof of concept is a Ge photodetector which implements a MSM device structure.

In Chapter 2, a technique is developed for growing high quality Ge on amorphous substrates while adhering to BEOL processing constraints. Two dimensional geometrically confined lateral growth (2D GCLG) is used as a method to grow single crystal Ge on amorphous SiO_2 substrates. This technique is then expanded upon in order to fill a lithographically defined trench with Ge. The trench will serve as the active material in the final photodetector. Different device designs are explored, including the use of aligned or staggered seeds. A trade-off is determined with respect to ease of fabrication versus expected final device performance. The shortcomings of this approach are pointed out and potential new designs are presented which can overcome these shortcomings.

In Chapter 3, the material quality of the Ge is characterized. Optical characterization techniques are employed due to their high spatial resolution as well as ease of sample preparation. Raman spectroscopy is utilized in order to measure the Raman frequency in the Ge, which is correlated to the strain state of the Ge. Very high tensile strains are measured. The measured strain is significantly greater than what is predicted by a thermal mismatch model. The accuracy of the measurement is verified by photoluminescence (PL) measurements. PL was used to determine the band gap

of the Ge, which was also correlated to the strain state. The strain measured by PL verifies the strain measured by Raman, confirming its validity. Cross-sectional images show the presence of small voids in the Ge. Finite element stress/strain modeling is performed, showing that the voids act as stress/strain concentrators and therefore account for the large strain present in the Ge. The resolved shear stress is calculated and shown to be significantly below the critical resolved shear stress, and therefore it is determined that dislocations can not nucleate in the Ge.

In Chapter 4, Schottky barriers on Ge are developed. It is shown that any direct metallization to *p*-type Ge produces ohmic contacts, which would result in MSM detectors with very high leakage currents. The contacts are always ohmic due to Fermi level pinning close to the valence band. Multiple surface cleaning procedures are shown to be incapable of passivating the defect states at the interface and relieving the Fermi level pinning. Thin interlayers are shown to effectively passivate the interface states and de-pin the Fermi level, resulting in the formation of Schottky barriers. The addition of an amorphous Si layer to passivate the Ge, then a thin tunneling HfO_2 layer is shown to de-pin the Fermi level and form Schottky contacts. However, the HfO_2 is shown to be unstable at elevated temperatures. Therefore, a thin 1 nm Al_2O_3 layer is used between the Ge and the Al contact. This is also effective at de-pinning the Fermi level and results in large Schottky barriers which are stable at elevated temperatures.

In Chapter 5, the Schottky contacts developed in Chapter 4 are utilized in MSM photodetectors. Interdigitated metal contacts are designed and tested on blanket Ge. Low leakage current is observed while maintaining high responsivities. This device structure is transferred to selectively grown Ge in 1 µm wide trenches. These MSM photodetectors are proven to have state of the art low dark current. In addition, they have the highest responsivity measured in a Ge MSM or *p-i-n* photodetector due to the presence of gain. A model is developed in order to relate contact spacing to the detector responsivity in order to forecast the performance of a device fabricated with

higher resolution lithography. Finally, the Schottky contacts developed in Chapter 4 are added to the material developed in Chapter 2 in order to fabricate Ge MSM photodetectors that are BEOL compatible. Fabrication challenges created a highly defective Ge surface, and therefore leaky diodes with high dark current. However, significant photocurrent was measured with responsivities indicating quantum efficiencies greater than 100 %, therefore confirming the presence of gain. These detectors serve as a proof of concept for active photonic devices that are capable of monolithic integration into the back end of line of a standard CMOS process.

Chapter 2

Germanium Growth on Amorphous Substrates

2.1 Introduction

In order to fabricate high performance photodetectors, it is first necessary to make high quality active material. High quality material can be defined by three main attributes. The material should be crystalline, or have the largest grains possible, the concentration of point defects should be minimized, and the concentration of extended defects, or dislocations, should be minimized.

This chapter focuses on the first attribute, increasing the grain size as much as possible. Grain boundaries act as disruptions to the crystallinity of the material, and therefore can create defect states within the band gap of the material. These defect states can act as Shockley-Read-Hall trap assisted recombination sites, which can reduce the responsivity of a photodetector. They can accumulate contaminants. They can block charge conduction, therefore rectifying current flow. They can also act as scattering sites, reducing carrier mobilities [35]. Due to their adverse effect on electrical properties, their presence should be minimized and therefore the grain size should be maximized in order to have the highest quality active material possible.

2.2 Two-Dimensional Geometrically Confined Lateral Growth

2.2.1 Technique

Two-dimensional geometrically confined lateral growth takes advantage of selective deposition, grain growth velocity anisotropy, and twinning, in order to deposit single crystal Ge on an amorphous substrate. A schematic of the basic process flow is shown in Figure 2-1. First, a silicon substrate is oxidized in order to create an oxide pseudo-substrate. This is the amorphous substrate that the Ge deposition occurs on. Then, a thin a-Si film is deposited on the oxide. The film thickness is typically around 50 nm. The a-Si is then patterned into a thin line (100 nm to 300 nm in width). After the a-Si line is patterned, a 200 nm to 500 nm thick oxide overlay film is deposited by plasma-enhanced chemical vapor deposition (PECVD). Then, a reactive ion etch (RIE) is performed to etch a window through the oxide overlay, to the oxide pseudo-substrate, exposing the a-Si line. Then, the a-Si line is etched through with a selective RIE. At this point, there is a thin a-Si line embedded in oxide, and exposed to air at one end. The schematic in part (a) of Figure 2-1 shows what the processing looks like up to this point. Next, a selective wet etch is performed with TMAH in order to undercut the a-Si. At this point, shown by part (b) in Figure 2-1, there is an a-Si line that is recessed within a high aspect-ratio channel that has oxide sidewalls. Finally, the structure is ready for Ge growth. The growth takes place within an ultra-high vacuum chemical vapor deposition reactor (UHVCVD) at 450 °C. The process is completely CMOS compatible and all processing takes place at or below 450 °C so that the process can be implemented in BEOL integration.

During the Ge growth in the UHVCVD, the Ge selectively deposits on the Si, and not on the oxide. Therefore, polycrystalline Ge deposition initiates on the a-Si seed at the back of the oxide channel. If the correct oxide channel geometry is chosen,

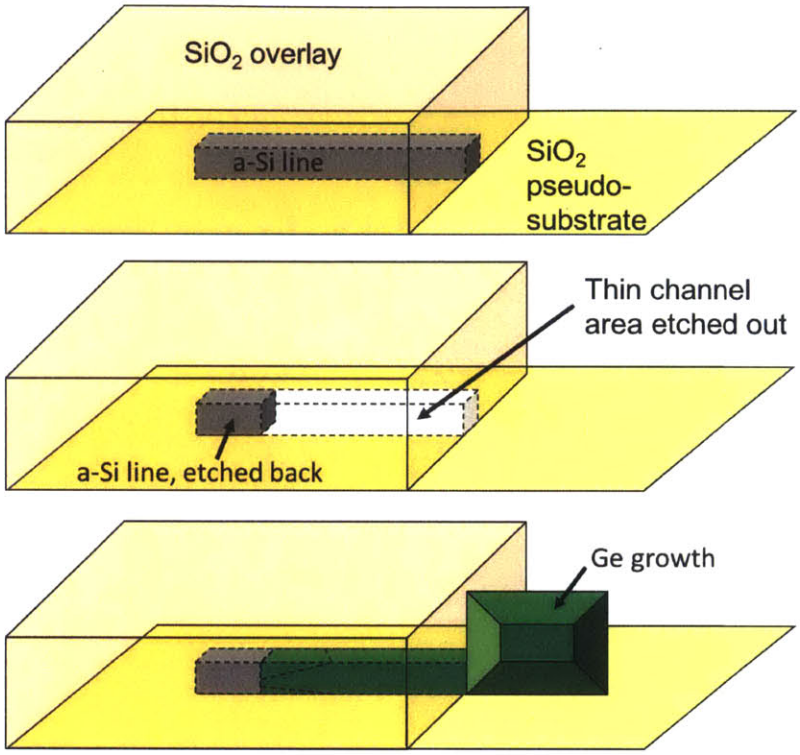


Figure 2-1: Fabrication process for 2D GCLG.

then, by the time the Ge emerges from the channel, only a single grain emerges and the emerging Ge is crystalline. Once the Ge emerges from the channel, the exposed Ge is now single crystalline, and further growth can occur epitaxially. This is shown schematically in part (c) of Figure 2-1. A representative example of a Ge growth via the 2D GCLG method is shown in Figure 2-2. The large facets on the Ge crystallite indicate that the growth is crystalline.

2.2.2 Mechanism

The two-dimensional geometrically confined lateral growth technique takes advantage of grain growth velocity anisotropy, Ge selective deposition, and twinning in order to obtain single crystalline Ge on amorphous substrates at low temperature.

When the Ge growth begins, the Ge nucleates on the Si only, and not on the SiO_2. Since the Si growth seed is amorphous, the Ge grains which nucleate have a

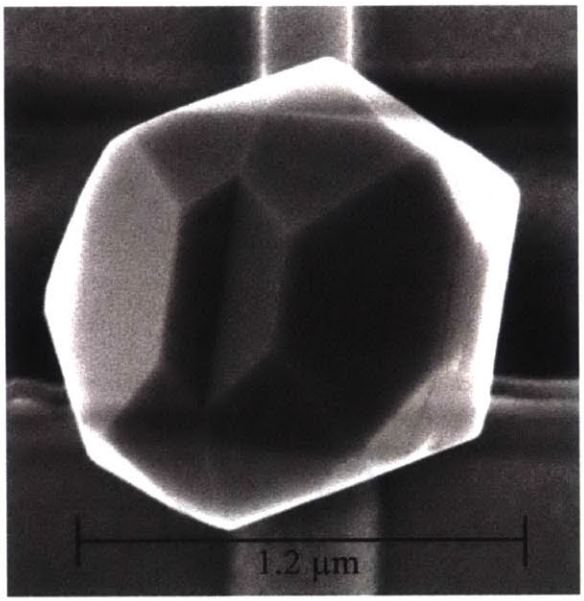


Figure 2-2: A representative example of Ge grown by the 2D GCLG method. The image is obtained by plan-view SEM. The bright vertical line below the Ge growth is the confining channel from which the Ge emerged. The large facets indicate that the Ge growth is crystalline. From [21].

randomized orientation. The GeH_4 decomposes via pyrolysis and Ge adsorbs onto the Si surface. The then diffuses along the surface until a stable cluster of adatoms forms. The stable clusters form all over the Si surface and are the initial grains from which the polycrystalline film grows. The initial grains that nucleate have a random grain orientation. During the growth process, the faster growing grains overtake the slow growing grains such that the grain growth velocity anisotropy tends to eliminate the slow growing grains [36]. The initial film is an array of randomly distributed and randomly oriented grains. The figure shows that as the film thickness increases, the film becomes textured, such that the fast growing grain orientations overtake the slow growing grain orientations. This is exactly what happens in the 2D GCLG technique. The slow growing $\langle 111 \rangle$ oriented grains are overtaken by the faster growing $\langle 110 \rangle$ and $\langle 100 \rangle$ oriented grains.

If this grain growth anisotropy model is followed, then it is predicted that the fastest growing grain orientation, the $\langle 100 \rangle$ orientation, will dominate the growth. However,

the Si growth plane is recessed within a high aspect ratio SiO_2 growth channel and the channel sidewalls stop this from occurring. This is due to the tendency for Ge to form $\Sigma 3$ twins. These $\Sigma 3$ twin grain boundaries have an interface energy of approximately zero, and therefore form readily [37]. Twin grain boundaries are completely coherent without the presence of dislocation at the interface. Even if a grain is oriented such that the $\langle 100 \rangle$ direction is oriented towards the opening of the growth channel, it is unlikely that it will emerge from the channel, assuming that the channel aspect ratio is high. This is because it is likely to form a twin before it can emerge from the channel. When Ge forms a twin, the angle between the newly formed grain and the original grain is 60°. This means that while the original grain had its fast growing direction oriented towards the channel exit, the grain after the twin will have its fast growing direction oriented towards the channel wall. Therefore twinning effectively pins the $\langle 100 \rangle$ oriented grains by causing them to self terminate in the oxide sidewalls. On the other hand, a grain that initially has a $\langle 110 \rangle$ orientation can continue to grow in a $\langle 110 \rangle$ direction even after twinning [36]. This is because there exists $\langle 110 \rangle$ directions that form a 60° angle between them. While the $\langle 100 \rangle$ grain will be oriented towards the channel sidewalls after twinning, the $\langle 110 \rangle$ grain may still be oriented towards the channel exit even after twinning. Therefore, if the channel geometry is designed correctly, then only the grains that have a $\langle 110 \rangle$ orientation will emerge.

Growing Ge from the bottom of a channel allows for selection of specific grain orientations, but the careful design of the channel is required in order to obtain single crystalline growth. The number of grains that emerge from the channel is related to the channel's aspect ratio. If the channel is shallow and wide (low aspect ratio), then the channel walls will not cause significant confinement in order to terminate the twinned $\langle 100 \rangle$ grains. In addition, multiple grains will nucleate with their fast growing grains oriented towards the channel exit, and therefore multiple grains may emerge. However, if the channel is narrow and deep (high aspect ratio), then there will be significant confinement of the mis-oriented grains. In addition, if the Si surface

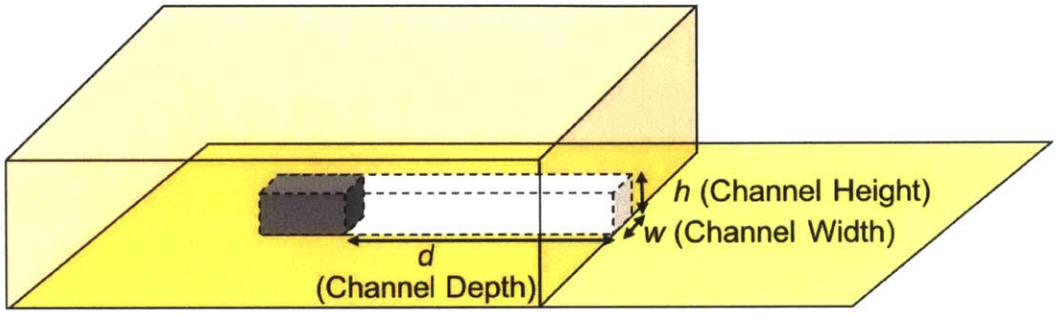


Figure 2-3: Definitions of the channel dimensions that the Ge grows from in the 2D GCLG process.

in which the Ge grows on is smaller, then a smaller number of Ge grains will nucleate and it is less probable for multiple grains to emerge from the channel. If the aspect ratio is too high, then no grains may emerge from a given channel. If the channel is very long and very narrow, then it may be that no grains nucleate such that their fast growing direction is oriented towards the channel opening. Therefore, some channel geometry optimization is necessary.

In order to model the channel, the channel structure is assumed to be a rectangular prism. The a-Si plane at the base of the channel has a height, h, and a width, w. The undercut etch defines the channel depth, d. This geometry is shown schematically in Figure 2-3.

The goal of the model is to predict the number of grains, N_G, which will emerge from a given channel geometry. The channel geometry is determined entirely by its height, h, width, w, and depth, d. In reference [21], first the ratio of Ω_c/Ω_n is calculated. Here, Ω_c denotes the solid angle of the channel opening as seen from the center of the a-Si growth plane at the bottom of the channel. Ω_n denotes the solid angle bounded the four standard stereographic triangles surrounding a single $\langle 110 \rangle$ pole. Figure 2-4 shows an example of the standard stereographic projection of a cubic crystal. The shaded area denotes the four standard stereographic triangles surrounding a single $\langle 110 \rangle$ pole. Therefore, Ω_n represents the range of mis-orientation of a single $\langle 110 \rangle$ pole before a different specific $\langle 110 \rangle$ pole would be closer to the a-Si

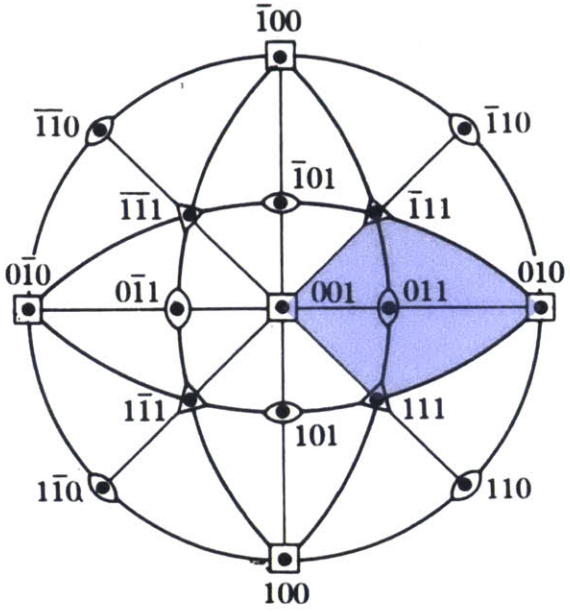


Figure 2-4: The standard stereographic projections of a cubic crystal.

substrate normal direction.

The values of Ω_c and Ω_n are calculated by the following:

$$\Omega_c = 4 \arcsin\left(\frac{hw}{\sqrt{(4d^2 + w^2)(4d^2 + h^2)}}\right) \tag{2.1}$$

$$\Omega_n = 2\pi \cdot \left(\frac{4}{24}\right) = \frac{\pi}{3} \tag{2.2}$$

where:

Ω_c = Solid and formed by channel opening from the perspective of a-Si nucleation seed
Ω_n = Solid angle of four standard stereographic triangles around a single (110) pole
h = Height of channel
w = Width of channel
d = Depth of channel

The ratio of Ω_c/Ω_n indicates the probability of a randomly nucleated grain to have its $\langle 110 \rangle$ direction oriented such that it will intersect with the opening of the channel. This gives the likelihood of a randomly oriented grain exiting the channel

within a sufficient growth time. It assumes that if a grain is oriented such that its ⟨110⟩ direction intersects with the channel wall, then the growth will terminate and will not emerge from the channel.

In order to complete the model, the probability of a grain emerging from a channel Ω_c/Ω_n is multiplied by the number of grains that nucleate on the a-Si plane. The number of nucleated grains is calculated by dividing the area of the a-Si growth plane by the area of the base of a Ge grain on a-Si. The area of the a-Si growth plane is simply the product of the height and width of the channel and is calculated as hw. A_G denotes the average area of the base of a Ge grain on a-Si. Therefore, the total number of grains expected to emerge from a given channel (N_G) is given by:

$$N_G = \left(\frac{\Omega_c}{\Omega_n}\right)\left(\frac{hw}{A_G}\right) \tag{2.3}$$

where:

N_G = Number of grains expected to emerge from channel
A_G = Average base area of a Ge grain nucleated on a-Si at 450 °C (500 nm^2)

With the given model for $N_G = 1$, the number of grains expected to emerge from a given channel geometry can now be predicted. Although this gives the number of grains expected to emerge from a channel, there are some practical limitations imposed on actual channel design. For example, if a channel is very short and wide ($w \gg h$), then a channel geometry could still be designed such that $N_G = 1$. However it is not necessarily realistic for this geometry to completely confine the growth. If the channel width is large, it is unlikely for any grain to be able to overtake all other competing grains before emerging from the channel. Therefore, in order to insure the model accuracy, it is ideal to have an equal channel height and width. This rough design constraint aides in allowing the fast growing ⟨110⟩ grains to overtake the slower growing grains. If the constraint that $h = w$ is imposed, then the equation for N_G can be reduced. By combining Equations (2.1) to (2.3), and setting $h = w$, the following

expression is obtained:

$$N_{\mathrm{G}} = \left(\frac{12}{\pi A_{\mathrm{G}}}\right) \cdot h^2 \arcsin\left(\frac{h^2}{4d^2 + h^2}\right) \tag{2.4}$$

Equation (2.4) is the model for the number of grains expected to emerge from a channel with a square cross-section. Upon inspection, it is evident that there are two ways to reduce N_{G}. To reduce the number of grains emerging from the square channel, the channel can either be designed to have a smaller cross section (reduce h), or be deeper (increase d). When h is reduced, the h^2 term in front of the expression dominates and N_{G} is rapidly reduced. However, when the d term is increased, the arcsine term asymptotically reduces to zero. Therefore, N_{G} is more sensitive to the cross section dimension and reducing this more rapidly provides the opportunity for single crystal growth. The approach of reducing h instead of increasing d also has an additional benefit. The channel depth, d, effectively defines the amount of Ge growth that must occur before the Ge emerges from the channel as a single crystal. Therefore, a large d would yield long growth times. Since Ge deposition occurs at low temperature (450 °C), the growth rate is slow and minimizing d can save hours of growth time. Putting this all together, in order to obtain single crystalline growth, it is ideal to have (1) a low N_{G}, (2) a square cross-section ($h = w$), and (3) a small d.

The crystal quality of the Ge within the trench is important. The more crystalline the Ge is in the trench, the better the optical and electrical properties will be. Since grain boundaries can serve as optical scattering points and carrier recombination centers, ideally the Ge in the trench should be single crystalline. In principle, this could be achieved with a single 2D GCLG crystallite. A single Ge crystallite is all that is needed to seed a crystalline Ge trench. However, the Ge growth rates at low temperature are slow, with growth rates observed at between 75 nm h^{-1} to 100 nm h^{-1}, depending on growth pressure. Therefore, it is impractical to grow a single crystallite to tens of microns in order to fill the trench because growth times would be several

days to weeks long. In addition, this would yield a very large overgrowth above the trench, which would be difficult to planarize. Instead, multiple 2D GCLG channels were used to seed multiple Ge crystallites. With this design, the Ge in the trench will not be single crystalline, however the grains that fill the trench will be large (>1 μm) and the device designer has complete control of the number of grains, as well as the placement of the individual grains.

2.3 Coalescing Ge Grains into Waveguide Trenches

The technique of two-dimensional, geometrically confined lateral growth is a method that was employed to fabricate high quality Ge for the active region in optoelectronic devices. In order to fabricate optimized devices, it is important for the device designer to have control over the device geometry and dimensions. The most basic geometry for the active region in Ge optoelectronic devices is a rectangular prism. There are two main ways in which this geometry is typically fabricated. In the first technique, a Ge thin film is deposited, then patterned using lithography, and then the Ge is etched into the desired structure [16, 38–40] . The second method that is commonly used, is selective growth of Ge in oxide trenches [15, 41–43]. In this method, the Si wafer substrate is oxidized so that there is an oxide film covering the crystalline Si. Then, the oxide is patterned and etched until trenches are opened, exposing the Si substrate below, in lithographically defined regions. Then, Ge growth occurs within the trench, taking advantage of selective deposition, with Ge only depositing on the Si wafer, and not on the oxide. Therefore, the patterning step occurs in the oxide, instead of the Ge directly. Both techniques allow for geometry control since the bounds of the Ge are controlled lithographically. In addition, both techniques can be used to produce a large range in active region sizes. The thickness of the active area is limited by the Ge growth thickness, but the length and the width of the Ge regions are only limited by lithography. In order for the 2D GCLG technique to be useful for application

in a Ge optoelectronic device, the method must be able to create Ge that fills a lithographically defined region. If the device is to be waveguide integrated, which is the ultimate goal, then the ideal shape is a rectangular prism that is on the order of 0.5 µm to 1 µm in width, similar height, and tens of microns in length. There may be some variations of these dimensions and the exact geometry, but this is a generalized goal.

2.3.1 Design

The crystal quality of the Ge within the trench is important. The more crystalline the Ge is in the trench, the better the optical and electrical properties will be. Since grain boundaries can serve as optical scattering points and carrier recombination centers, ideally the Ge in the trench should be single crystalline. In principle, this could be achieved with a single 2D GCLG crystallite. A single Ge crystallite is all that is needed to seed a crystalline Ge trench. However, the Ge growth rates at low temperature are slow, with growth rates observed at around $75\,\mathrm{nm\,h^{-1}}$ to $100\,\mathrm{nm\,h^{-1}}$, depending on growth pressure. Therefore, it is impractical to grow a single crystallite to tens of microns in order to fill the trench because growth times would be several days to weeks long. In addition, this would yield a very large overgrowth above the trench, which would be difficult to planarize. Instead, multiple 2D GCLG channels were used to seed multiple Ge crystallites. With this design, the Ge in the trench will not be single crystalline, however the grains that fill the trench will be large (>1 µm) and the device designer has complete control of the number of grains, as well as the placement of the individual grains.

The technique of two-dimensional, geometrically confined lateral growth is a method that can be used to obtain single crystalline Ge on an amorphous substrate. However, it is a very different crystalline seed than a typical crystalline Si substrate. Although the emerging Ge grain is crystalline, it has a very irregular geometry and does not serve as a typical substrate to seed planar epitaxial growth. Typically, sub-

strates for epitaxial growth are two dimensional and planar. This allows for controlled, uniform epitaxy with regards to growth rate, thickness control, and large area uniformity. However, the crystallite that emerges from the 2D GCLG technique is a small 3D structure. An example of the Ge crystallite that emerges from a channel is shown in Figure 2-2. It still works as a seed for crystalline growth, but the exact shape of the crystallite is unpredictable. In addition, it is too small to seed epitaxial growth to fill a trench, that is tens of microns long, within a reasonable growth time. In order to use the 2D GCLG growth technique for the active area of Ge optoelectronic devices, a novel new technique was designed in order to fill lithographically defined trenches.

Before the device itself was designed, first the individual 2D GCLG channels were designed. Since the Ge growth is seeded from these channels, from now on the 2D GCLG channels will be referred to as seeds. The geometry of the individual seed was first designed in order to yield single crystal Ge crystallites. In order to determine the required channel dimensions, Equation (2.3) was plotted for range of different channel geometries. This plot is shown in Figure 2-5. Here, it is assumed that the height of the seed is held constant at 50 nm. The purpose was to determine the effect of varying the seed width and depth. The height of the seed is determined by the a-Si film thickness, the width is defined by lithography and dry-etching, and the depth is determined by the TMAH undercut etch step.

In Figure 2-5, two dotted lines are drawn, one at $N_G = 1$ and one at $N_G = 2$. These should be considered the upper and lower bounds for an acceptable design. If $N_G < 1$, then it is predicted that a Ge grain will not emerge from the channel every time. For example, if $N_G = 0.5$, then it is predicted that a Ge grain will only emerge from 50 % of the channels with this given geometry. If $N_G = 2$, then it is predicted that 2 Ge grains will emerge from each channel. The ideal channel design is one in which the Ge emerges from the channel every time, however only one grain emerges. Therefore, the target range of N_G is between 1 and 2. Within this range, it is predicted that a Ge grain will emerge from the grain each time. In addition, when

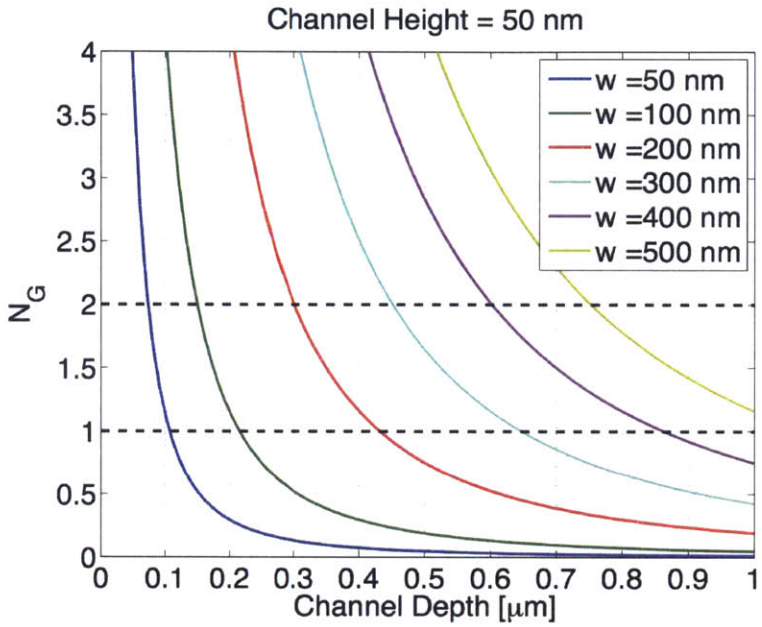


Figure 2-5: 2D GCLG design guide. This figure assumes a fixed channel height of 50 nm. The channel width is increased from 50 nm, which is the ideal value, to 500 nm, which is easier to fabricate in a real system. The purpose of this figure is to determine the channel length that yields an N_G value between 1 and 2.

N_G is less than 2, the model predicts that no more than 2 grains will emerge from each channel. Therefore, the channel should be designed such that the target range for N_G is between 1 and 2.

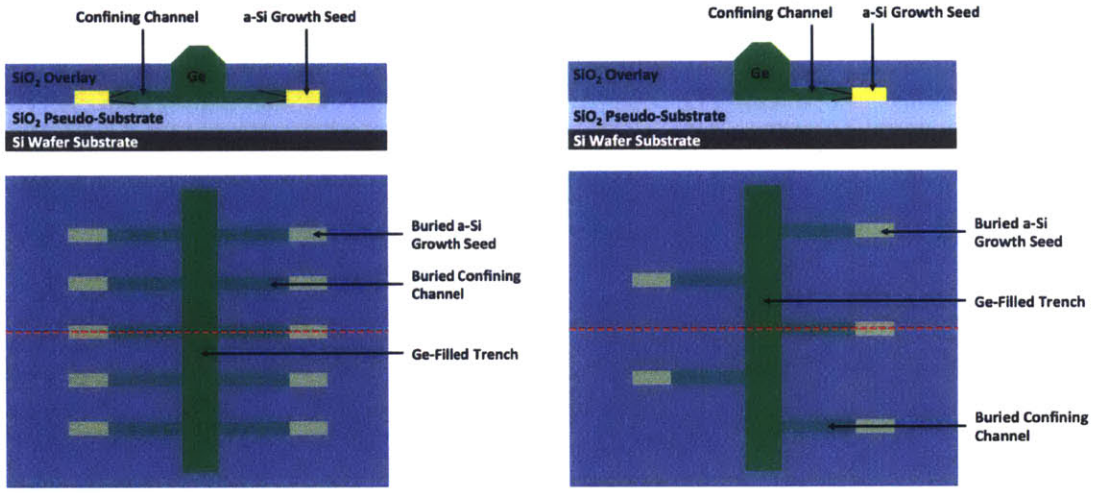
Each individual line in Figure 2-5 shows the same general trend. N_G decreases as the channel depth increases. This makes intuitive sense because as a channel gets deeper, the aspect ratio gets larger. This means that solid angle of the opening decreases. Therefore, the likelihood of a randomly nucleated grain being oriented such that the $\langle 110 \rangle$ direction is pointing towards the channel opening decreases. A second observation is that N_G increases as the height of the channel, h, increases. The explanation of this follows the same logic as before. The larger h yields a larger channel opening, and hence a larger solid angle of the channel opening. The larger solid angle leads to the large chance that a randomly nucleated grain is oriented such

that its ⟨110⟩ direction intercepts the channel opening.

In order to narrow in on exact channel dimensions, first the channel height was selected. The main factor limits the channel height is hydrogen incorporation into the a-Si film. The channel height is determined by the a-Si film thickness, which is deposited by plasma-enhanced chemical vapor deposition (PECVD). Amorphous Si deposited by PECVD is subjected to significant H incorporation into the Si during deposition, with hydrogen concentrations of approximately 10 at. % depending on the deposition conditions [44,45]. At concentrations greater than 10 at. %, microcavities will form with H selectively segregating to these cavities [46]. The problem with hydrogen incorporation is that when heated to 450 °C, the H that is trapped within the film becomes mobile [47], which leads to H coalescence and and the formation of bubbles. The hydrogen bubbles can eventually burst, destroying the planar Si film [48]. Therefore, the a-Si film must be kept thin. If it is too thick, then significant amounts of H become trapped within the film, which cause bubbles and hence destroy the film. In order to eliminate this risk, the a-Si layer was kept thin at 50 nm. Once the channel height is fixed, then the channel width and depth are chosen. The ideal width, for a fixed 50 nm channel height, is 50 nm. However, in reality, the width is limited by the resolution of the lithography. Once the width is determined, then the design rules are applied and Figure 2-5 is consulted in order to determine the depth that will yield an N_G value between 1 and 2. For channel widths of 100 nm, 200 nm and 300 nm, channel depths of 175 nm, 350 nm and 550 nm were targeted, respectively.

Once the individual channels are designed and optimized, then it is necessary to design structure that will fill a trench. As mentioned, for the 2D GCLG technique to be useful for a real optoelectronic device, it must be capable of filling a rectangular prism shaped trench that has a width of around 500 nm, a height of 200 nm to 500 nm, and a length of tens of microns. These dimensions are not arbitrary, but they are the approximate dimensions for waveguide integrated Ge optoelectronic devices, such as photodetectors and electro-absorption modulators. The cross- section of

approximately 500 nm by 500 nm is because this yields a single-mode Ge waveguide for light with a wavelength of 1.55 µm.



(a) Schematic of a trench filled using the aligned seed design.

(b) Schematic of a trench filled using the staggered seed design.

Figure 2-6: Design of a Ge-filled trench with large grains. The bottom schematics represent a plan-view, while the top represents a cross-section. The red dotted line in the plan view image indicates the plane through which the cross-section view is shown.

The design approach utilizes multiple 2D GCLG structures to seed multiple Ge grains. The use of more than one seed means that the Ge within the trench will not be single crystalline. The overall trench filling design is shown schematically in Figure 2-6. Multiple 2D GCLG structures, now to be called seeds, are arrayed with their channels opening into a common trench. The goal of the device is to nucleate multiple Ge crystallites within the trench, and then grow epitaxially until the crystallites coalesce and eventually fill the trench. This is creates a design trade-off between duration of Ge deposition, and number of grains in the trench. A large pitch between seeds yields large grains, but also increases growth time.

This growth technique is very different than typical fabrication techniques. Typically, Ge optoelectronic devices are fabricated in a planar fashion. Either a planar film is deposited and then etched into the appropriate device geometry, or a trench is

etched in SiO_2 and Ge is selectively deposited on a Si substrate. In both conventional techniques, the growth time is set by the desired film thickness. However, in the design shown in Figure 2-6, the growth time is set by the distance between seeds, and the height of the trench. It is not sufficient to grow Ge thick enough to emerge from the channel, but the Ge has to grow vertically enough to fill the trench, and laterally enough to coalesce with the neighboring seeds.

The two designs presented, one in Figure 2-6a and the other in Figure 2-6b, show a similar design to achieve the same goal. Both approaches utilize an array of 2D GCLG seeds to nucleate Ge crystallites within the trench, and then grow epitaxially until the crystallites coalesce, filling the trench. However, the approach in Figure 2-6a has aligned seeds while the design shown in Figure 2-6b has staggered seeds. The approach with aligned seeds minimizes Ge growth time, and allows for ease of fabrication. The growth time is minimized because the seeds are closer to each other and therefore less total growth is required before the Ge grains coalesce. It is also easier to fabricate because a lower tolerance is required in aligning mask levels, while performing the lithography. The fabrication technique is outlined in Figure 2-7.

While the aligned seed approach is easier to fabricate, and allows for shorter Ge growth times, the staggered seed approach minimizes the number of grains in the trench, and therefore maximizes the overall crystal quality within the trench. With the ideal seed and channel design, it can be assumed that one single grain emerges from each seed. Therefore, since the aligned seed design has twice as many seeds as the staggered seed design, it will also have twice as many grains. This yields twice as many grain boundaries. Grain boundaries can act as carrier recombination sites, optical and electrical scattering sites, and create high resistance, current blocking barriers [23, 24]. Therefore, less grain boundaries are beneficial for device quality. These two devices both offer a technique to fill lithographically defined trenches with large grain germanium. The exact number of grains, their physical location, and their size, can be predicted by the number of seeds and the spacing between them. However,

design trade-offs exist between ease of fabrication, crystal quality, and Ge growth time. A larger seed pitch yields larger Ge grains at coalescence, and therefore enhanced overall crystal quality within the trench and better device properties. However, it also means a longer growth time, which can be very significant at low temperatures. For example, depending on germane overpressure, growth times can be between 18 h to 20 h for approximately 1.5 µm of growth, yielding a growth rate of approximately 75 nm h^{-1} . Therefore, a seed pitch of several microns or greater is not realistic for a practical application.

An overview of the fabrication method is shown schematically in Figure 2-7. All steps are CMOS compatible, and occur at or below 450 °C. To start, a layer of SiO_2 is deposited on a Si wafer using a plasma-enhanced CVD (PECVD) deposition technique. The thickness of the SiO_2 is unimportant, because it merely serves as the amorphous pseudo-substrate. The purpose of this layer is to emulate the amorphous dielectric in the back end of the interconnect stack in a CMOS process flow. Once the oxide pseudo-substrate is formed, a thin layer of a-Si is deposited using PECVD, as indicated in (a) of Figure 2-7. The thickness of this layer determines the height of the 2D GCLG channel, and is therefore carefully controlled. For these devices, this layer was 50 nm thick.

Next, as indicated in (b) of Figure 2-7, the a-Si is patterned into thin lines. The widths of these lines determine the width of the 2D GCLG channels and were patterned to be between 100 nm to 300 nm . The stepper that was used to pattern these lines only has a reliable resolution limit of around 1 µm, and therefore a double exposure technique with a sub-micron offset was employed to reduce the line widths. After the double exposure of the photoresist, the remaining photoresist lines were further thinned by dry etching in an oxygen plasma. With this approach, it was possible to pattern lines as narrow as 100 nm with a stepper that is only capable of exposing 1 µm features.

After the a-Si lines are patterned, a SiO_2 overlay was deposited using PECVD, as

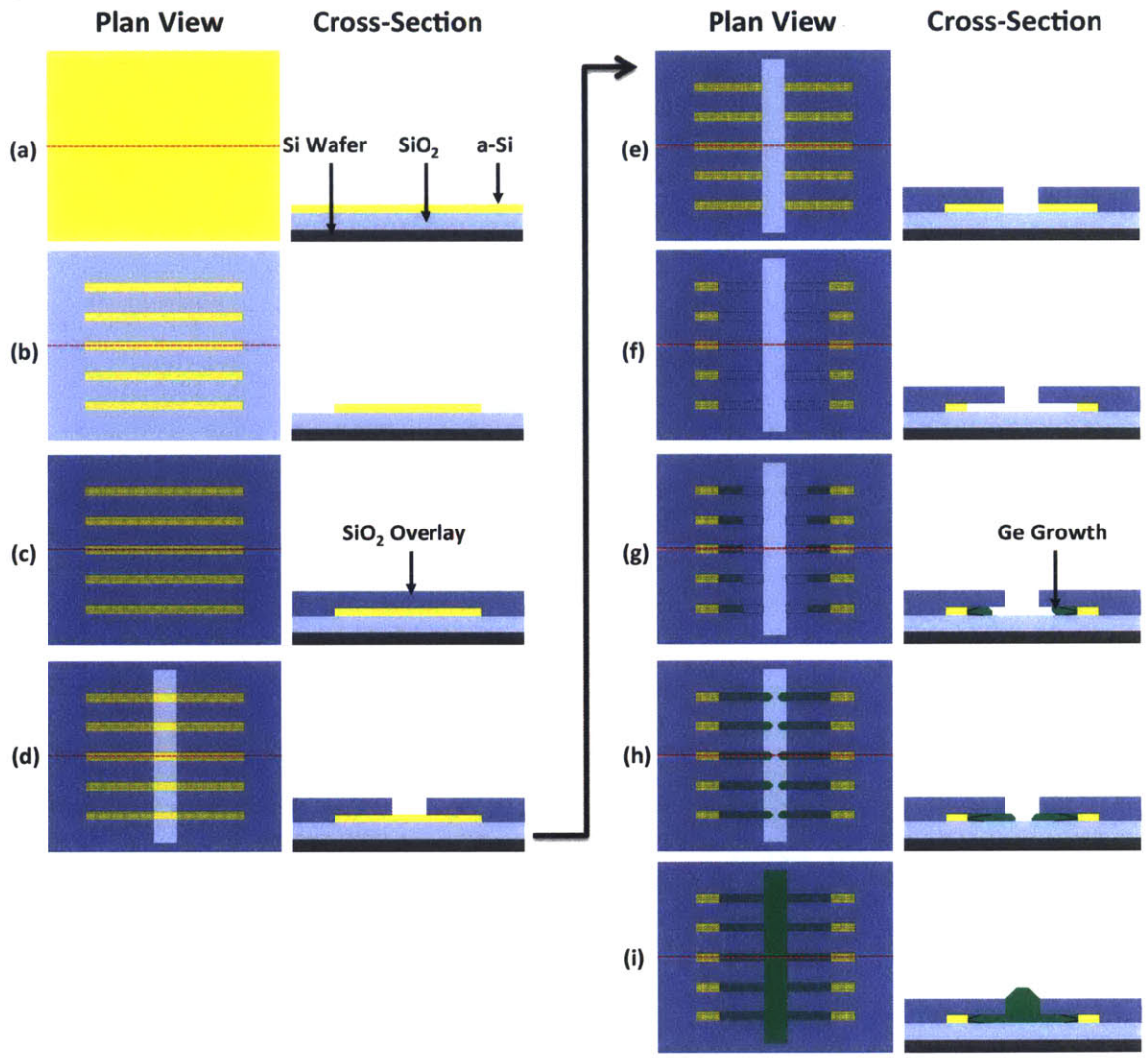


Figure 2-7: Process flow for utilizing 2D GCLG for trench filling. Each step shows a plan view perspective on left. The right side shows a cross-section view through the red dotted line. Part (a) shows a thin blanket a-Si film on an oxide film on a Si wafer substrate. Next, the a-Si is patterned into thin lines, shown by (b). In (c), an SiO_2 overlay is deposited on top of the a-Si lines. In (d) a trench is opened up in the SiO_2 overlay by RIE dry etching, exposing the a-Si. In (e), the exposed a-Si is dry etched. In (f), an undercut etch of the a-Si is performed with TMAH. In (g), Ge deposition begins in UHVCVD. In (h), the Ge emerges from the channels as a single crystal. Finally, in (i), the Ge crystallites coalesce and growth continues until the trench has been filled.

shown in (c). The thickness of this layer determines the height of the trench that is to be filled. This thickness was varied between 200 nm to 500 nm. Next, the trench itself is opened up. This is done by first selectively dry etching through the oxide, as indicated in (d), and then selectively etching the a-Si, as indicated in (e). At this point, the a-Si lines are intersecting the trench sidewalls. Next, the growth channel is defined. This is done with a tetramethylammonium hydroxide (TMAH) wet etch at 80 °C. TMAH selectively etches Si, and not SiO_2 and therefore undercut etches the Si lines, while leaving the SiO_2 overlay intact, as shown by (f). This etch defines the channel depth, and therefore was timed in order to finalize the dimensions of the growth channel, effectively defining N_G of the 2D GCLG structure. Finally, the wafers are ready for Ge growth.

Immediately before Ge growth, the wafers are cleaned in a standard RCA clean, ending with a quick dip in hydrofluoric acid (HF). This is in order to passivate the exposed Si by occupying the dangling bonds in Si with H, inhibiting the formation of a native oxide. Then, the wafers are loaded into an ultra high vacuum chemical vapor deposition (UHVCVD) reactor. The a-Si and SiO_2 films deposited by PECVD have hydrogen incorporation into the films. To remove the H, the wafers were annealed at 450 °C in the UHVCVD reactor tube at a base pressure of 1.8×10^{-8} mbar for two hours to allow the hydrogen to sufficiently out-gas from the films. Finally, Ge growth was initiated with germane (GeH_4) flow at 7.5 sccm at a chamber temperature of 450 °C and a growth pressure of 3.4×10^{-3} mbar . No carrier gases were used. The Ge selectively deposits on the a-Si, and not on the SiO_2, as indicated in (g). Eventually, the Ge emerges from the channels as a single crystal crystallite, as shown by (h). These crystallites are used to seed epitaxial growth until, eventually, the neighboring crystallites coalesce and eventually fill the trench, as shown in (i). The total growth time is 18 hours. Once the trench is eventually filled, the Ge within the trench is non-planar and highly faceted. If the Ge is to be used for an optoelectronic device where low-loss modal propagation is required, such as a modulator, the device must

be chemically and mechanically polished (CMP) before further processing.

2.3.2 Experimental Results

The technique of arrayed seeds was shown to be a viable technique to fill a lithographically defined oxide trench with large grain Ge. There is no fundamental limit to the length of the trench that can be filled with this technique, as it is the seed pitch that determines the growth time, not the overall trench length. An example of a trench that has been filled using this technique is shown in Figure 2-8. The plan view SEM image shown in this figure shows a trench that is greater than 50 µm long, and is completely filled with Ge. The vertical lines in the image are caused by the a-Si seed lines. The SiO_2 overlay deposition process is not planarized and therefore expands the shape of the a-Si seed lines. The vertical lines are SiO_2, but indicate the location of the growth seeds below.

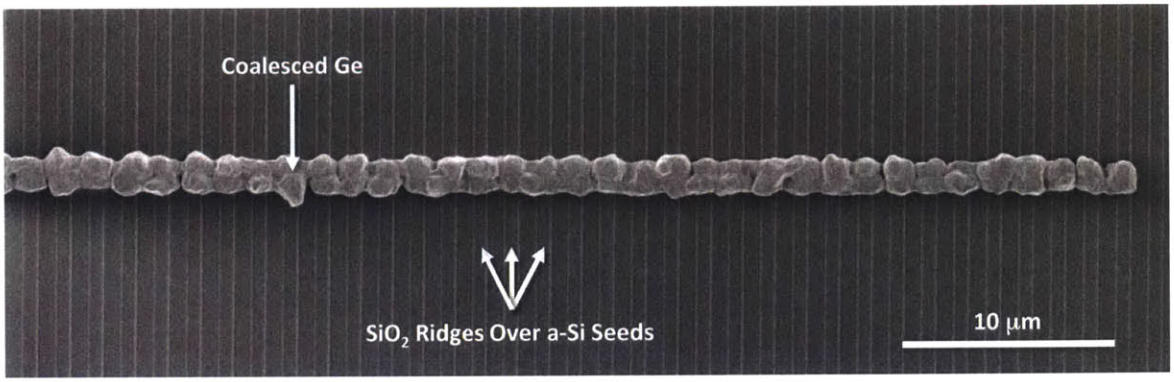
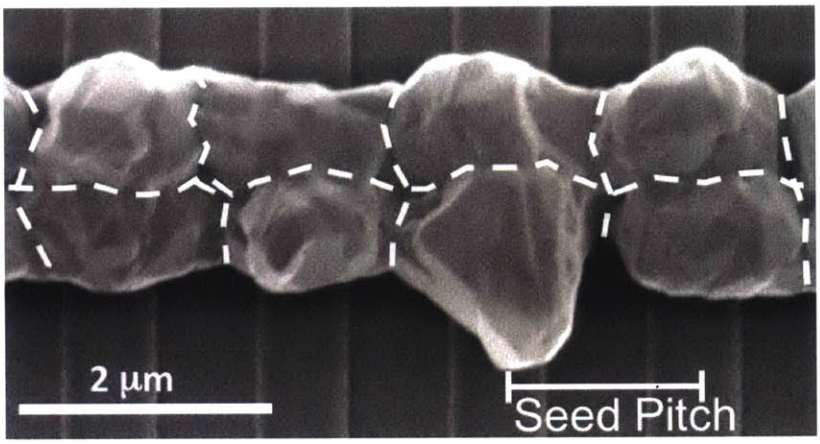


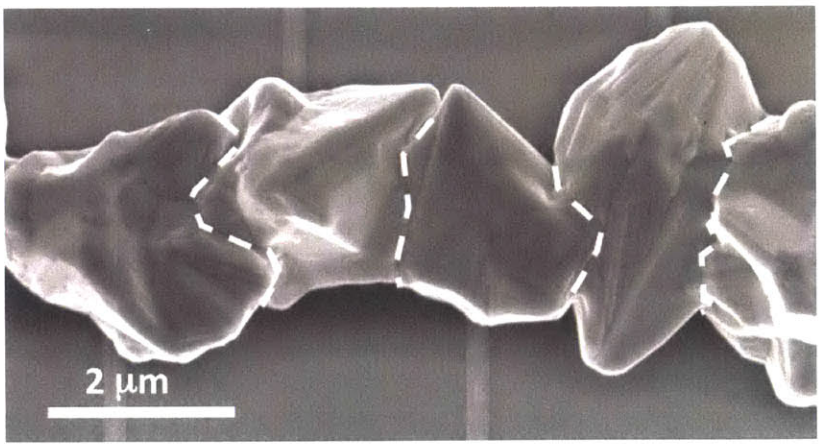
Figure 2-8: Plan-view SEM of a lithographically-defined trench that has been filled with Ge grains implementing the 2D GCLG process.

The Ge that has emerged from the trench is clearly non-planar. However, the Ge crystallites have coalesced with their neighboring grains, and therefore the trench has been successfully filled. An additional image of a filled trench is shown in Figure 2-9. The places at which the grains coalesced are marked with a dotted line, which indicates the approximate location of the grain boundaries. This shows that both the aligned seed design and the staggered seed design can be used to successfully fill

trenches. The aligned seed design has an additional grain boundary that runs down the middle of the trench, which the staggered seed design eliminates. Therefore, in order to maximize crystal quality in the active region of the detector, the staggered seed design is preferred. The zoomed-in images here show the clear coalescence of the grains, to completely fill the trenches.



(a) Coalesced Ge grains using the "Aligned Seed" design.



(b) Coalesced Ge grains using the "Staggered Seed" design.

Figure 2-9: Plan view SEM image of trenches filled using the geometrically confined growth technique. Approximate grain boundary lines have been drawn in. The dotted lines indicate the place at which the grains coalesced.

The top of the Ge is very non-planar. However, the topographical features of the Ge are located above the surface of the trench. If these devices are to be used in as

the active region in actual optoelectronic devices, then a CMP step would be required in order to planarize the Ge.

There is also significant vertical overgrowth of Ge out of the trench. This is because the pitch between seeds is 1.5 µm and the trench height is only 0.5 µm in this device. The growth process continues until the Ge grains coalesce with the neighboring grains, and therefore significant trench overgrowth occurs before the lateral growth is large enough for coalescence. The crystallographic orientation normal to the confined growth channel is randomized. With the random orientation, the lateral and vertical growth rates are, on average, equivalent. Therefore, the grains will grow the same amount in the vertical direction as they do in the lateral direction and the vertical overgrowth is approximately equal to the seed pitch (lateral growth distance).

The growth time can be calculated for different designs, based on a trench geometry and a growth rate. Growth rates for Ge in confined patterns at 450 °C was measured to be approximately 100 nm h^{-1} at a pressure of 1×10^{-2} mbar. A compact waveguide integrated photodetector is approximately 200 nm high and 500 nm wide. Therefore, the growth time to fill a trench is dependent on the seed pitch, as shown in Figure 2-10.

When the seed pitch is large, then the seeds are far away from each other and the limiting time step is for the grains to grow laterally and coalesce with the neighboring grains. When the seeds pitch is very small, then the growth time is limited by the time required to fill the width of the trench, since lateral growth distance required for coalescence is low. When the aligned seed design is used, then each grain has to grow large enough to fill the entire width of the trench (500 nm), however when the aligned seed is used, then the grain only has to grow half the width of the trench in order to coalesce with the grain on the opposite side of the trench. Therefore, the aligned seed design allows for faster growth time and higher manufacturing throughput, but at the expense of the addition of an additional grain boundary running down the middle of the trench. In order to choose a final device design, the trade off between throughput and material quality must be made.

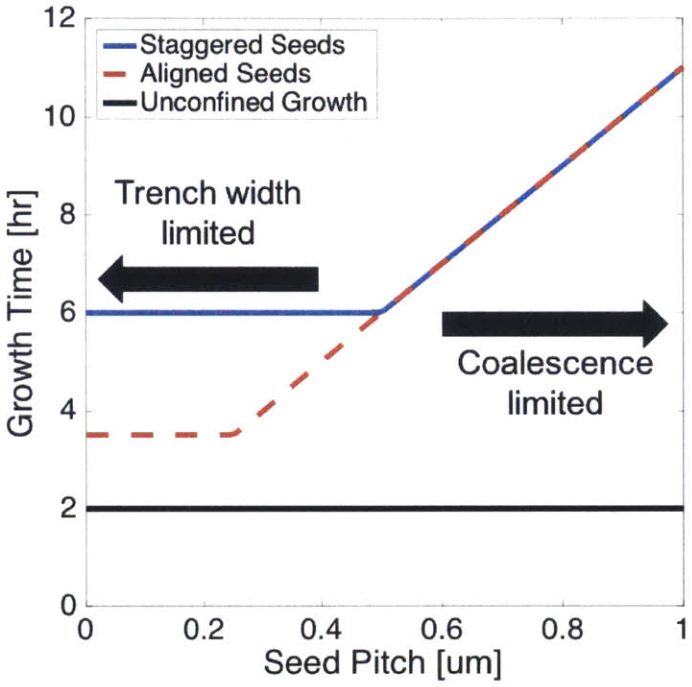


Figure 2-10: Growth time required to fill a trench that is 500 nm wide by 200 nm deep trench. The unconfined growth method (standard planar growth from substrate) does not have a seed and is therefore a constant. The growth time is determined by the assuming a growth rate of $100\,\mathrm{nm\,h^{-1}}$, as observed experimentally at 450 °C and a pressure of 1×10^{-2} mbar.

In order to compare the throughput of the confined growth technique with a standard unconfined planar growth technique, the growth time for these devices was also added to Figure 2-10. The growth time for an unconfined growth is always lower than a confined growth. This is in part due to the design in which the confined growth devices require the Ge to grow ~100 nm in the confined channel before the single crystal Ge emerges into the trench. This additional growth lowers the throughput. A conventional planar growth technique requires only 200 nm of growth to fill the trench from the bottom up, independent of pitch since there are no confinement channels for this growth mode.

2.3.3 Challenges

The staggered and aligned seed designs are a first iteration proof of concept, proving that it is possible to fill a lithographically defined trench with large grain Ge, on an amorphous substrate. However, there are still large problems with the design. The first problem is due to the misalignment of the trench and the seeds in the staggered seed design. This problem can be remedied with a trench mask level offset, or with the use of more modern equipment. The alignment in a stepper tool should be much less than 1 µm, and therefore this is not necessarily a design problem. However, one process step clearly limits the reproducibility of the design. That step is the TMAH undercut etch. The undercut etch is a timed wet etch. TMAH is selective, and will etch Si while leaving SiO_2 mainly un-etched. However, the only way to define the channel depth, is by timing the undercut etch such that the correct amount of Si is removed.

The problem of the TMAH undercut etch arises due to the geometrical limitations imposed by the small channel dimensions. The channel being etched has a cross-section that can be as small as 50 nm by 100 nm. At these small dimensions, mass transport of etchant can become a limiting factor when determining etch rates. In order to verify this hypothesis, the oxide overlay was removed in order to see the a-Si/Ge interface. This was done by selectively etching the SiO_2 overlay with a buffered oxide etch (BOE), which selectively etches SiO_2 and leaves Si and Ge intact. The result of this etch is shown in Figure 2-11. This etch was performed on a device that did not achieve coalescence, due to a growth sequence that was not optimized. In this plan view SEM image, the interface between the a-Si and the Ge is clearly shown, and occurs at the leading etch of the Si seed. This boundary shows the depth of the undercut etch that was achieved by the TMAH etch. The sidewalls of the trench have receded and are now bowed due to the SiO_2 being etched from the sidewalls within the trench, at the same time as it was etched from the top surface.

The problem with the TMAH undercut etch is due to the non-uniformity in

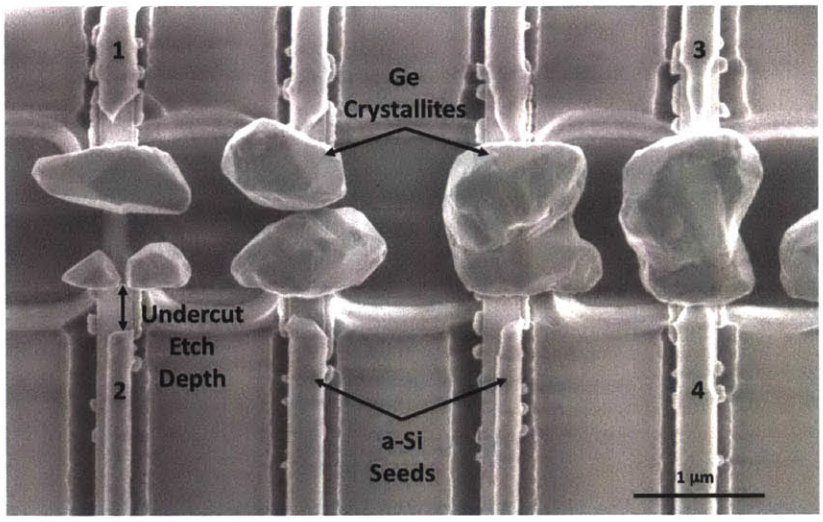


Figure 2-11: A plan view SEM image of a failed growth that has the top oxide removed by BOE. There is a clear non-uniformity in undercut etch of the a-Si.

undercut etch rates. From Figure 2-11, it is clearly seen that the total undercut etch depth is not constant for all of the seeds. For example, the two seeds on the left, labeled 1 and 2, have larger undercut etch depths than the two seeds on the right, labeled 3 and 4. It is difficult to quantify the absolute length of the undercut etch, due to the Ge overgrowth over the trench sidewalls. Therefore, the edge of the channel is hidden under the Ge overgrowth. The only way to measure undercut etch depth precisely, would be to use a focused ion beam (FIB) to mill a cross-section in each growth, and then measure each seed individually.

The variations in undercut etch depth leads to variations in the number of grains that will emerge from a given channel, N_G. Therefore, with a variable undercut etch, it is impossible to precisely control the geometry of the seed, and impossible to insure that the Ge crystallite that emerges from the channel will be single crystalline. For example, the grain that emerges from Seed 1 is highly faceted. The facet sizes are comparable to the size of the entire grain. This indicates that the entire growth is single crystalline. In addition, this seed has a large undercut etch depth, yielding a low N_G, since the height and width of the growth channels are fixed for all seeds.

Seed 2 also has a large undercut etch depth, however, two individual grains have emerged. This is likely because the amount of undercut etch leads to an N_G value of ~ 2. However, Seeds 3 and 4, have noticeably less undercut etch. This means that the channel depth is less, and therefore the N_G value is greater. This is confirmed by the facet sizes in the Ge grains that emerged from these channels. The facets are much smaller than the total grain, indicating that the growth is likely poly-crystalline and multiple grains emerged from the channel.

In addition to the lack of control of the total undercut etch depth, the remaining a-Si seed geometry after etching is also variable. Seed 2 shows a straight undercut etch that yielded an a-Si seed front parallel to the channel opening. This is exactly the geometry that was assumed in the model for predicting the number of grains that emerge from a 2D GCLG channel. However, the exposed front edge of Seed 1 and Seed 3 is clearly pointed. This means that the etch rate was not equal along the width of the seed, and therefore the undercut etch was not uniform, even within a single channel. This may be caused by capillary action, or mass transport limitations within such small channels. The front surface of the a-Si seed is the surface upon which Ge nucleates during growth. The area of this surface defines the number of seeds that are predicted to nucleate on the surface. The variation in seed geometry adds unpredictable variations to the model for N_G, therefore making it impossible to design channels that consistently yield single crystal Ge emergence. The TMAH undercut etch is the step, that limits the reproducibility and reliability of this design. Therefore, the process flow needs to be redesigned to eliminate the timed undercut etch step.

2.4 Improved Designs

The problem with the TMAH undercut etch step, is it relies on a timed etch in a small channel. This creates the potential for mass-transport limitations due to the

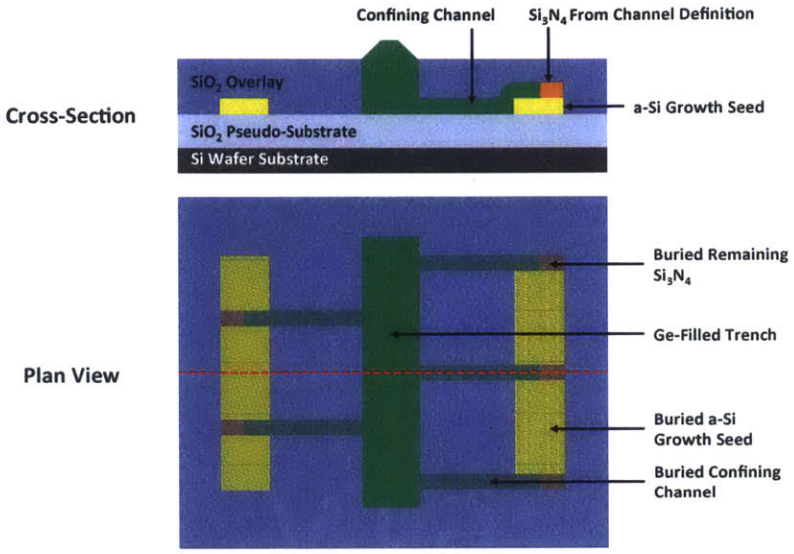


Figure 2-12: Schematic of the improved trench filling design utilizing silicon nitride for channel formation.

small cross-sectional dimensions of the channels. The only reliable way to control the channel depth is through either a gas-phase selective etch of Si at high vacuum, or by using lithography. Processing in high vacuum increases the mean free path of particles, and therefore reduces the potential for mass- transport limitations within small channels. However, high vacuum selective Si etches are not a standard processing step, so the lithography approach was utilized.

The enhanced design incorporates a new material, Si_3N_4. The nitride is used to define the channel cross-sectional dimensions. In order to define the channel depth, the a-Si seed is lithographically patterned such that it is a set distance from the edge of the trench. This distance defines and sets the channel depth. The final device design, after fabrication, is shown in Figure 2-12. The a-Si lines are now patterned such that they are parallel to the trench, with the gap between them determining the channel depth. The channels are made from patterned silicon nitride lines, instead of a-Si lines. Hot phosphoric acid selectively etches silicon nitride without etching a-Si or SiO_2 [49, 50], and therefore the Si_3N_4 can be over-etched. This eliminates the need for a timed etch for channel depth formation.

With the utilization of Si_3N_4 for channel formation, all critical channel dimensions are now controlled with either lithography or film thicknesses. Film thicknesses can be carefully controlled, and are reliable and repeatable. With the right equipment, patterning with lithography is very accurate and reproducible. Therefore, the yield of the new nitride design should be high, with reliable and reproducible trench filling.

A schematic of the process flow to fabricate the nitride-incorporated design is shown in Figure 2-13. The process for the enhanced design begins the same way as the original design. First, a SiO_2 film is deposited on a Si wafer using PECVD. This serves as the pseudo-substrate, emulating the wafer surface above the interconnect stack in a Si CMOS process flow. Next, an a-Si film is deposited using PECVD. The thickness of the a-Si film corresponds with the designed channel height. Next, the a-Si is patterned into two parallel lines. The width of the lines is not important, but they are approximately the same length as the trench. The critical dimension is the space between the lines. The space is equal to two times the channel depth, plus the width of the trench. This is because these lines define the channel depth. The process, up to this point is depicted in part (a) of Figure 2-13.

After the a-Si lines are patterned, a Si_3N_4 film is deposited using PECVD. The thickness of the Si_3N_4 film is equivalent to the thickness of the a-Si film, and is designed to be the height of the 2D GCLG channel. The Si_3N_4 film is then patterned into thin lines. The width of the lines is equal to the width of the of the growth channels. The nitride lines are patterned in a staggered design in order to maximize grain size. This will require accurate alignment between mask levels, but this is easily achievable with deep ultraviolet (DUV) lithography equipment. One edge of the staggered nitride lines will be aligned with the center of the trench. The other end overlaps the a-Si seed lines. If perfect alignment between mask levels could be achieved, then the overlap would be unnecessary. However, the nitride is designed to overlap the a-Si lines in order to reduce the alignment tolerances. The patterning of the nitride lines is shown in part (b) of Figure 2-13.

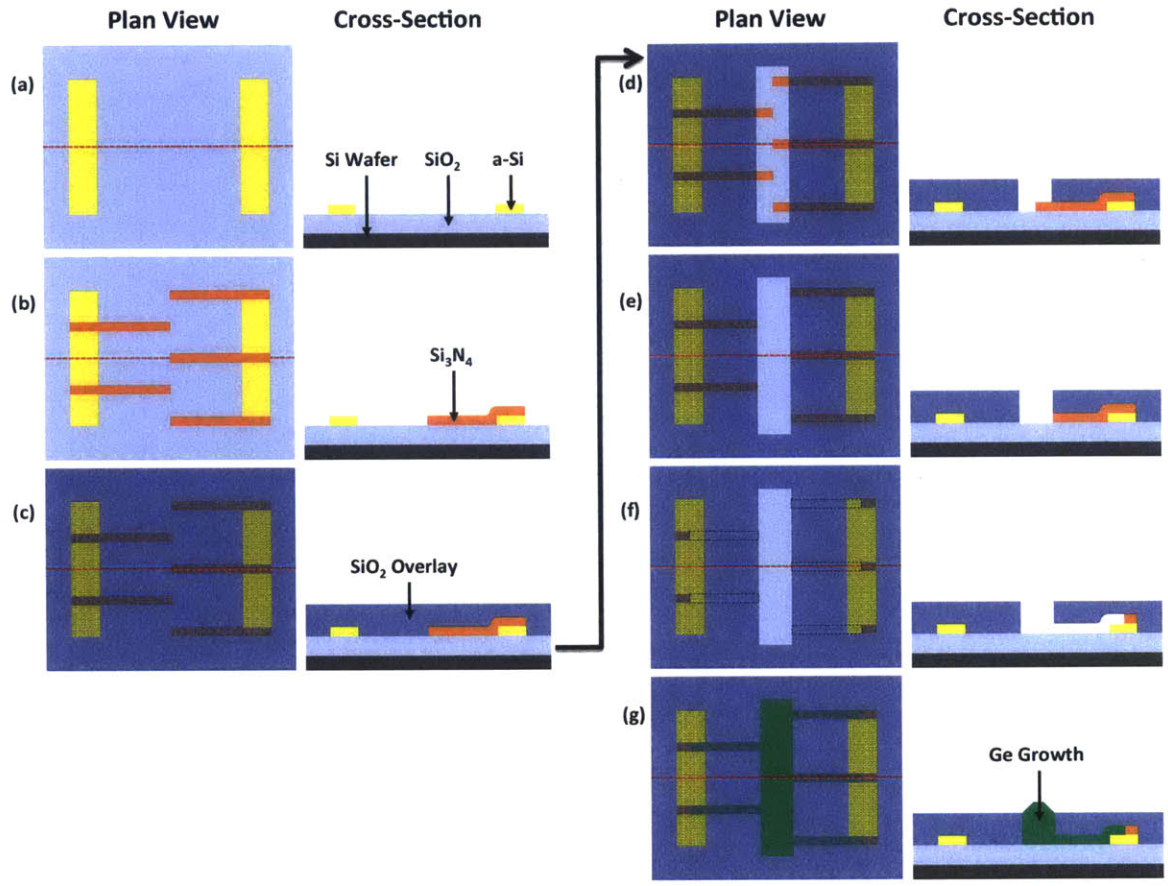


Figure 2-13: Process flow for fabricating the enhanced design with silicon nitride. The dotted red line in each plan view image represents the plane through which the cross-section view is shown.

A SiO_2 overlay film is deposited, over the nitride lines, using PECVD. The overlay thickness defines the trench height. The result of this step is shown in part (c). Next, the trench is patterned in the SiO_2. The SiO_2 is selectively dry etched in order to achieve vertical sidewalls. This exposes the ends of the nitride lines and is shown in part (d). Next, the exposed nitride lines are dry etched, as shown in (e). The nitride lines are then undercut etched until the a-Si seeds are exposed. The undercut etch is a wet etch in hot phosphoric acid, which selectively etches the Si_3N_4 without etching the SiO_2 or the a-Si. Due to the etch selectivity, the Si_3N_4 can be over- etched. This minimizes the effect of variable undercut etch rates. The purpose of the nitride lines

is to define the channel cross-sectional dimensions. The total depth of the channel is determined by the space between the a-Si seed lines and the trench, which has been defined lithographically. Therefore, the Si_3N_4 is over-etched, ensuring the a-Si seed is exposed to the open trench. This is shown in part (f). Finally, the Ge is deposited in a UHVCVD reactor at 450 °C. The Ge will still randomly nucleate on the a-Si seed at the end of the growth channel. With the correct channel design, a single crystal Ge crystallite will emerge from each channel, and therefore seed epitaxial growth within the channel. The crystallites will continue to grow epitaxially until the grains coalesce with the neighboring grains, effectively filling the trench, as shown in part (g).

The enhanced design for trench filling, which utilizes nitride to define the growth channels, eliminates the problems that were observed in the original design. It is an optimized design that uses the fundamentals of the 2D GCLG technique, and applies them to the goal of filling a trench with large grain Ge. This trench is lithographically defined, and all processing is compatible with Si CMOS back end integration. The design effectively creates a trench, filled with large grain Ge, which can be used as the active region in Ge-based optoelectronic devices.

2.5 Summary

In this chapter, a technique was developed in order to fabricate high quality germanium on an amorphous substrate, while adhering to low temperature processing constraints. Several properties of Ge were taken advantage of in order to achieve this. The properties that Ge will deposit selectively on Si and not SiO_2, polycrystalline Ge deposited on amorphous Si had a random grain orientation, some grain orientations grow faster than others, and the fact that fast growing grain orientations will overtake slow growing grain orientations were all used in the growth technique.

Ge was grown in two dimensional geometrically confined lateral growth (2D GCLG) channels in order to yield single crystal germanium. These grains were then arrayed

to open into a lithographically defined trench. The nucleation seeds and confinement channels were then arrayed to fill the trench in order to serve as the active material of a Ge photodetector. A staggered seed design was implemented in order to eliminate a grain boundary that runs down the middle of the trench.

The limitations in this growth technique were pointed out, namely the highly variable undercut etch of the amorphous Si. Then an improved design is presented in which all critical dimensions can be lithographically defined in order to maximize control and device yield.

Chapter 3

Optical Measurements of Strain in Germanium Trenches

The development of a technique to grow crystalline germanium on amorphous substrates, while adhering to low-temperature processing constraints was presented in Chapter 2. However, the only material characterization technique was SEM, essentially visual inspection. This material is intended to be the active material in a Ge photodetector, and therefore additional properties of the material must be understood in order to make a well designed photodetector. In this chapter, the strain state of the Ge is investigated.

3.1 Introduction

While strain may seem to be a mechanical property, and irrelevant to to the optoelectronic properties of a semiconductor photodetector, the presence of stress and strain in a material can dramatically affect a broad range of material properties. The presence of strain can change the direct band gap of germanium, with tensile strain reducing the band gap [51]. A shift in band gap will shift the absorption spectrum of a Ge photodetector. Strain can also affect the carrier mobility, with tensile strain

shown to increase the carrier mobility in Ge [52]. An increased carrier mobility can reduce the transit time limited bandwidth, and also increase the gain in an MSM detector.

Stress and strain are intimately coupled, and the presence of stress has been shown to affect material properties as well. The presence of shear stress can cause dislocations to glide and cause plastic deformation [53]. Dislocations can create defect states in the material which will reduce the responsivity and increase the dark current of a detector. Stress and strain have been shown to shift the phonon energy in Ge, with tensile stress and strain decreasing the phonon energy [54]. Therefore, determining the strain state of the Ge can also elucidate a range of other material properties which will affect device performance.

In order to fabricate high-performance germanium photodetectors, the active material should be of the highest crystalline quality possible. Specifically, this means that the grain size should be maximized, the concentration of point defects should be minimized, and the density of extended defects should be minimized. Grain boundaries, point defects, and extended defects all create trap states within the bandgap. These trap states can serve as generation sites which increase the dark current of a detector, or serve as recombination centers which reduce the carrier lifetime and therefore decrease the responsivity of the detector [55–59].

The size of the germanium grains in the photodetector is dependent on the growth conditions as well as the device structure, as outlined in Chapter 2. The concentration of point defects is dependent on the growth temperature and growth rate. The growth temperature determines the diffusivity of the adatoms during growth, and the growth rate determines the amount of time that the adatoms can diffuse before they are covered by the next monolayer of growth and are fixed into a stationary position. The time that the adatom has to diffuse to an appropriate lattice site τ is $\sim 1/r_g$ where r_g is the growth rate in monolayers per second [60]. The approximate distance that adatoms will diffuse in order to find a lattice site is $L = \sqrt{D_s \tau}$ where D_s is the

surface diffusivity of germanium adatoms, as measured in [61]. This distance must be large enough for the adatom to diffuse to the edge of an atomic step in order for the epitaxial process to continue without creating growth-induced point defects. Therefore the germanium growth conditions can be tuned in order to minimize the concentration of point defects. The surface diffusivity is a thermally activated process, and has an exponential dependence on temperature. Therefore, increasing the growth temperature drastically increases the surface diffusivity of adatoms which increases the surface diffusion length and can effectively reduce the concentration of point defects. Reducing the growth rate can have the same effect, but with a weaker sensitivity.

While the concentration of point defects is strongly a function of the growth temperature of the material, the generation of dislocations is dependent on the shear stresses in the material. The shear stress in the material is dependent on growth conditions, as well as the device structure and can be calculated from the strain state of the material, if the strain state is known. Therefore, by determining the strain state in the Ge, the resolved shear stress can be calculated, and the generation of dislocations can be inferred.

There are several standard methods for measuring the strain state of crystalline materials. One such method is to use x-ray diffraction (XRD) [62]. However, there are practical limitations to using this method. Typically the focused spot size is on the order of 1 mm in diameter, significantly larger than the 1 µm waveguides that are used for detectors in this application. Therefore the measurement is an average measurement of the entire probed area and the majority of the signal will be dominated by the surrounding SiO_2. It is possible to use XRD to perform strain measurements with sub-micron spatial resolution, but it requires the use of a synchrotron x-ray source [63].

The convergent beam electron diffraction technique of transmission electron microscopy (TEM) is another technique that can be used to measure strain [64, 65]. However, this is a destructive method and requires cleaving and polishing, or focused

ion beam (FIB) milling to reduce the sample thickness down to approximately 200 nm in order to transmit electrons through the sample for imaging. TEM has the benefit of being very spatially localized, but the imaging window is limited, and therefore it is very time consuming to acquire strain measurements from many samples in order to determine statistical averages.

The strain state of the material can also be determined using electron beam back scatter diffraction (EBSD) [66–69]. The EBSD method can have a strain sensitivity of $\sim$0.01 % and excellent spatial resolution, equivalent to the electron beam spot size (approximately 10 nm), but requires a planar sample which is electrically conductive. For the Ge waveguides surrounded by SiO_2, this requires chemical mechanical polishing (CMP) for planarization and sputtering of a thin gold layer to eliminate sample charging. Therefore, this technique also requires a destructive sample preparation technique.

Optical measurement approaches can provide the best combination of spatial resolution, strain sensitivity, and ease of sample preparation. Optical measurement techniques can be non-destructive as well as highly localized. The spatial resolution is approximately equivalent to the spot size of the laser source on the sample, $\sim$1 µm for high magnifications. There is no need to have an electrically conductive or perfectly planar sample. Ge that is faceted from growth can be analyzed directly without additional sample preparation. Therefore, optical techniques can provide a rapid method of acquiring localized strain measurements.

In this chapter, two different optical techniques are utilized to determine the strain state of selectively grown Ge in SiO_2 trenches. Raman spectroscopy and photoluminescence are both used to infer the existing strain in the Ge. Although the two methods are both optical techniques, they are probing very different physical properties of the crystal. Raman spectroscopy is used to probe the phonon energy in the crystal, while photoluminescence is used to probe the electronic band structure of the crystal, both of which are dependent on the strain state of the material. The

strain state is determined from these optical measurement techniques, and then used to calculate the resolved shear stress in the material. This shear stress is then compared to the critical resolved shear stress to determine whether or not dislocation generation can occur in the Ge, given the device structure and growth conditions.

3.2 Using Raman Spectroscopy to Measure Strain

Raman spectroscopy is a non-destructive optical measurement technique which can be used to determine the optical phonon frequency of a material. This frequency is dependent on the strain state of the material, and therefore can be used to calculate the strain of the material [70,71]. Raman spectroscopy can be performed through a microscope objective, and therefore can be localized down to a spot size of approximately 1 μm.

3.2.1 Theory

Raman spectroscopy is a technique in which the phonon energy is probed by analyzing the spectrum of light which is inelastically scattered by a material. A laser is used to excite electrons in the material to a virtual state. These electrons rapidly decay and release a new scattered photon which is of different energy from the original incident photon. The scattered photon is typically of lower energy than the incident photon, and the reduction in energy is correlated to the energy required to generate a phonon. It is also possible for the scattered photon to be of greater energy than the incident photon, with the difference in energy correlated to the absorption of a phonon. The generation of phonons is called the Stokes process, and the absorption of phonons is called the anti-Stokes process.

In these processes, both energy and crystal momentum must be conserved. Therefore, the phonon energy can be directly correlated to the difference in energy of the scattered photon and the incident photon. The conservation of energy can be

expressed by:

$$\hbar\omega_{\mathrm{L}} = \hbar\omega_{\mathrm{s}} \pm \hbar\omega_{\mathrm{ph}} \tag{3.1}$$

and the conservation of crystal momentum can be expressed by:

$$\hbar n\mathbf{k}_{\mathrm{L}} = \hbar n\mathbf{k}_{\mathrm{s}} \pm \hbar\mathbf{q} \tag{3.2}$$

where:

$\hbar$ = Reduced Plank's Constant
ω_{L} = Incident Laser Photon Frequency
ω_{s} = Scattered Photon Frequency
ω_{ph} = Phonon Frequency
n = Index of Refraction of Material
$\mathbf{k}_{\mathrm{L}}$ = Free Space Wave Vector of Incident Laser Photon
$\mathbf{k}_{\mathrm{s}}$ = Free Space Wave Vector of Scattered Photon
$\mathbf{q}$ = Phonon Wave Vector

In Equations (3.1) and (3.2), the upper sign relates to when a phonon is generated (Stokes scattering) and the lower sign relates to the when a phonon is absorbed (anti-Stokes scattering). With Equation (3.1), the phonon energy can be calculated from the difference in energy between the photons from the incident laser and the scattered photons as measured in the Raman spectrum. Equation (3.2) gives insight into which phonons are being observed. The photon wave vector is proportional to $1/\lambda$ which is on the order of $10^5\,\mathrm{cm}^{-1}$ while the Brillouin zone boundary is proportional to $1/a$ which is on the order of $10^8\,\mathrm{cm}^{-1}$, where λ is the photon wavelength and a is the lattice constant. Therefore, the photon wave vector can be considered to be negligible, and the phonon that is either generated or absorbed can be assumed to be an optical phonon at $\mathbf{q} = \mathbf{0}$ [72].

The phonon frequency in a given material is not a constant. The phonon frequency is a vibrational mode of the atoms within the crystal which changes as the crystal is physically deformed. Strain causes the phonon frequency to shift, which causes the

peak location in the Raman spectrum to shift accordingly. The strain in a crystal can be determined by the shift of the Raman spectrum according to the lattice dynamical theory, originally presented by Ganesan et al. in [73]:

$$\begin{vmatrix} p\varepsilon_{11} + q(\varepsilon_{22} + \varepsilon_{33}) - \lambda_1 & 2r\varepsilon_{12} & 2r\varepsilon_{13} \\ 2r\varepsilon_{12} & p\varepsilon_{22} + q(\varepsilon_{11} + \varepsilon_{33}) - \lambda_2 & 2r\varepsilon_{23} \\ 2r\varepsilon_{13} & 2r\varepsilon_{23} & p\varepsilon_{33} + q(\varepsilon_{11} + \varepsilon_{22}) - \lambda_3 \end{vmatrix} = 0 \tag{3.3}$$

where:

λ_i $= \omega_i^2 - \omega_0^2$
ω_0 = Unstrained Raman Frequency ($300.5\,\mathrm{cm}^{-1}$)
ω_i = Measured Raman Frequency
p = Longitudinal Phonon Deformation Potential ($-1.66 \cdot \omega_0^2$)
q = Transverse Phonon Deformation Potential ($-2.19 \cdot \omega_0^2$)
r = Shear Phonon Deformation Potential ($-10.87 \cdot \omega_0^2$)
ε_{ij} = Strain

The phonon deformation potentials p, q, and r, are phenomenological coefficients which describe how the phonon frequency changes with strain, and are experimentally determined in [54, 74]. They effectively describe the change in the "spring constant" of the optical phonons as a function of strain.

Assuming that the $\hat{x}_3$ direction is normal to the surface of the wafer being measured, then the only Raman signal viewable from a normally incident excitation source is λ_3. Equation (3.3) can be simplified by making two key assumptions. First, it can be assumed that the germanium is biaxially strained. Therefore, the strain in the two in-plane longitudinal directions ($\hat{x}_1, \hat{x}_2$) are equivalent. Also, it can be assumed that the Poisson's ratio in the material is a constant. These assumptions are as follows:

$$\varepsilon_{11} = \varepsilon_{22} = \varepsilon_{\parallel} \tag{3.4}$$

and

$$\nu = -\frac{\varepsilon_{33}}{\varepsilon_{\parallel}} \tag{3.5}$$

where:

$\varepsilon_{\parallel}$ = In-Plane Strain
ν = Poisson's Ratio (0.26)

For the growth of crystalline thin films on relatively thick substrates, the biaxial strain assumption is a standard assumption [75]. However, this assumption may not hold for Ge grown in narrow trenches. In addition, the assumption that the Poisson's ratio is a constant may also not always hold. The Poisson's ratio of a crystal is dependent on the crystallographic orientation, and therefore the grain orientation of a polycrystalline material can affect this assumption [76].

Ultimately, Equations (3.3) to (3.5) can be combined in order to solve for the in-plane strain as a function of measured Raman frequency. The result is:

$$\varepsilon_{\parallel} = \frac{\omega_3^2 - \omega_0^2}{2q - \nu p} \tag{3.6}$$

Therefore, Equation (3.6) is a simple equation which can be used to calculate the in-plane strain of a material from the measured Raman peak location, a reference Raman spectrum from unstrained material, the phonon deformation potentials, and the Poisson's ratio of the material.

3.2.2 Experimental Methods

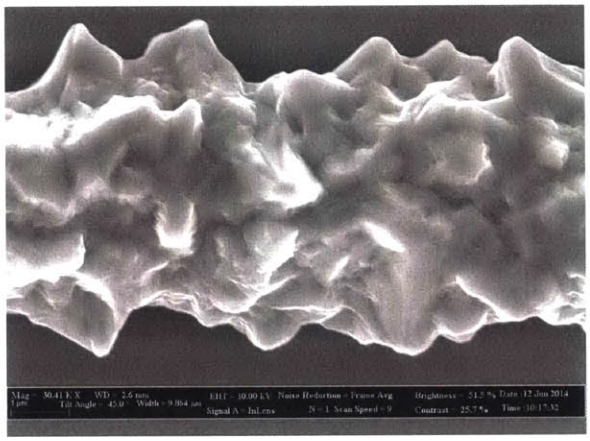
The strain state was measured in three different types of germanium trenches. Each sample consisted of Ge selectively grown in 1 µm wide trenches by UHVCVD at 450 °C. However, the three samples each had a different substrate at the base of the waveguide trench that the Ge nucleated from. In the first sample, the Ge was grown

directly on an amorphous silicon substrate. There was no geometric confinement structure to increase grain size. In the second sample, the Ge was grown on the 2-dimensional geometrically confined lateral growth (2D-GCLG) substrate, as described in Section 2.2. On the final sample, Ge was grown epitaxially on a crystalline silicon substrate.

Figure 3-1 shows plan-view SEM images of the three samples which were measured. From the images, it is clear that the grain size is the smallest in the sample grown on amorphous Si and the grain size is the largest in the Ge grown on crystalline Si. The grain size of the Ge grown on the SiO_2 geometrically confined substrate (2D-GCLG) is between the other two samples. The grain size was not measured directly, but it can be inferred from the faceting. Long range faceting is only possible across a single crystal grain. Therefore the extent of faceting is indicative of the grain size. The Ge grown on amorphous Si in Figure 3-1a exhibits minimal faceting, indicating the presence of small Ge grains. The Ge grown on confined structures in Figure 3-1b shows significant faceting, indicating that this sample is polycrystalline, but exhibits large grains. The Ge grown epitaxially on crystalline Si in Figure 3-1c is completely faceted, indicating that this sample is single crystalline.

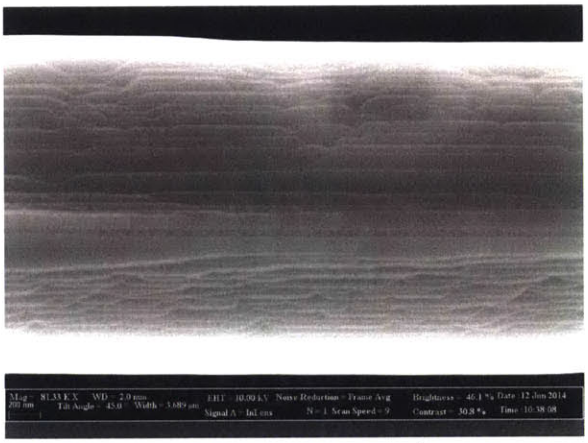
In order to accurately measure the in-plane strain in the three samples, a small Raman peak shift must be accurately measured. A HORIBA Jobin Yvon LabRAM HR bench-top system was used in order to measure Raman spectra from the three samples. The excitation source was a 532 nm laser which was magnified by a 100x confocal microscope objective, resulting in a laser spot size with a diameter of approximately 2 µm.

The spectrum of the scattered light was measured by a silicon CCD detector. However, the measured Raman peak was very narrow and the data in the vicinity of the peak was relatively sparse. Simply determining the peak location by the data point with the greatest signal intensity may not accurately determine the peak position, especially when small peak shifts are expected. In order to accurately determine



(a) Ge grown on on an amorphous Si substrate.

(b) Ge grown on SiO_2 2D-GCLG substrate.



(c) Epitaxially grown Ge on a crystalline Si substrate.

Figure 3-1: Plan-view SEM images of the three samples examined. All three samples were grown at 450 °C in 1 µm wide SiO_2 trenches.

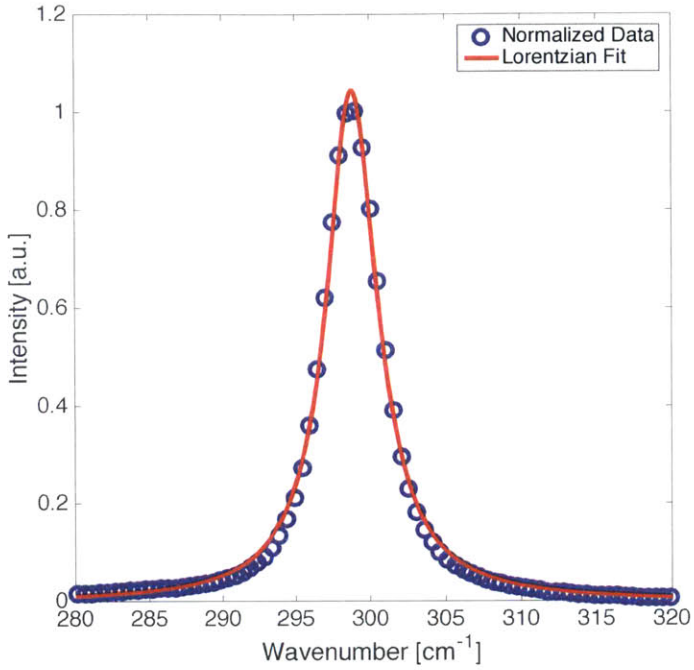


Figure 3-2: An example of fitting a normalized Raman spectrum to a Lorentzian function. This was done in order to precisely determine the peak location, despite sparse data in the vicinity of the peak.

the peak position, the Raman spectrum was normalized and then fit to a Lorentzian function. The Lorentzian function is an accurate fit to Raman spectra and the center of the fit can be used to precisely locate the peak position [77–79]. An example of the data fitting is shown in Figure 3-2. The Lorentzian function accurately fit the Raman spectrum and provided a technique to precisely determine the peak location, even if it exists between two data points.

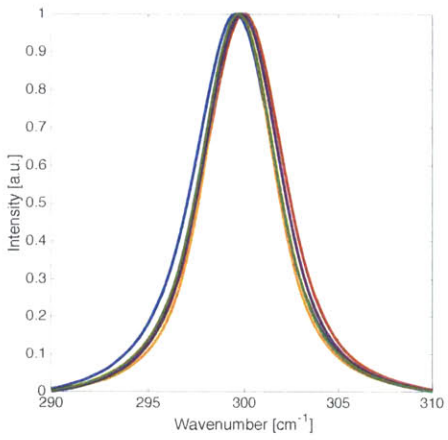
3.2.3 Raman Results

The strain was determined in all three samples indicated in Figure 3-1 by measuring the strain-shifted Raman spectrum. Raman spectra were measured from multiple

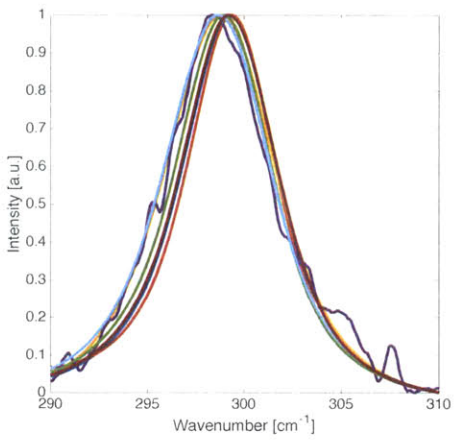
locations within a single waveguide, in multiple different waveguides, and at multiple laser powers. The spectra were normalized and plotted as shown in Figure 3-3. Each sample shows a peak shift towards lower wavenumbers, with respect to the unstrained peak position of $300.5\,\mathrm{cm}^{-1}$. The shift in the Raman peak location to lower wavenumbers indicates a reduction in phonon frequency and therefore the presence of tensile strain in the Ge.

The Raman spectra acquired from the epitaxially grown Ge on crystalline Si show the smallest shift from the unstrained location. Each measurement yielded repeatable and regular spectra with a small standard deviation, as shown in Figure 3-3a. The peak location was measured to be $299.75 \pm 0.18\,\mathrm{cm}^{-1}$. The uniformity in the measured spectra indicate that the phonon frequency is the same in all spatial locations along the waveguide, as well as in different locations on the wafer. This is to be expected as the epitaxially grown Ge is single crystalline with the same orientation and strain state in all locations.

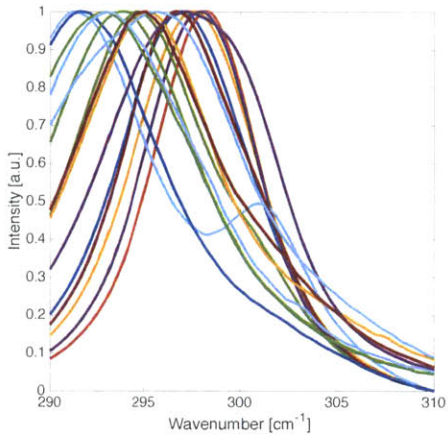
The Raman spectra acquired from the Ge grown on amorphous Si had a larger peak shift and more variability than the epitaxial Ge grown on crystalline Si. The peak location was measured to be $298.94 \pm 0.29\,\mathrm{cm}^{-1}$. The one noisy spectrum (plotted in purple in Figure 3-3b) was due to a low signal to noise ratio caused by a weak signal when the incident laser was at low power. This sample is polycrystalline with small Ge grains. The presence of multiple grains with different orientations will increase the variability of the phonon energies and their measured spectra. The incident laser spot size is approximately $2\,\mu\mathrm{m}$ in diameter, significantly larger than the Ge grain size. The measured spectrum is an average of all of the grains which are probed within the $2\,\mu\mathrm{m}$ spot. The presence of many grains with potentially different strain states broadens the Raman spectrum, however by measuring many different grains simultaneously, the variations are all averaged into a single spectrum. This reduces the variability from one measurement to another, since each spectrum is effectively an average spectrum from many different Ge grains.



(a) Normalized Raman spectra of Ge on crystalline Si. Peak position = 299.75 ± 0.18 cm^{-1}



(b) Normalized Raman spectra of Ge on amorphous Si. Peak position = 298.94 ± 0.29 cm^{-1}



(c) Normalized Raman spectra of Ge on amorphous SiO_2 2D GCLG substrate. Peak position = 295.14 ± 2.26 cm^{-1}

Figure 3-3: Normalized Raman spectra. All three samples were grown at 450 °C in a 1 µm wide SiO_2 trench.

The Raman spectra acquired from the Ge grown on SiO_2 in 2D GCLG substrates exhibited significant peak shifts towards lower wavenumbers, as well as significant variability. The standard deviation of the peak position was an order of magnitude larger than the other two samples. The peak location was measured to be $295.14 \pm 2.26\,\mathrm{cm}^{-1}$. In addition, some spectra had two distinct peaks, as shown in Figure 3-3c. The large standard deviation indicates that different grains have significantly phonon energies, and therefore significantly different strains. The existence of two peaks within one measurement is caused by two adjacent grains being sampled simultaneously during a single measurement. This is because the laser spot size is approximately $2\,\mu\mathrm{m}$ in diameter, while the individual Ge grains are approximately $1\,\mu\mathrm{m}$ in diameter. Therefore, two adjacent Ge grains can be measured simultaneously. If the two neighboring grains have significantly different strains, then they will exhibit different Raman peak shifts, causing two peaks in the measurement. This means that there exist multiple strain states even within the same waveguide. The strain can vary significantly from one grain to another, despite them being adjacent to one another.

Figure 3-4 overlays the experimentally measured Raman peak locations with the expected strain, as calculated from Equation (3.6). The straight line indicates the theoretical relationship between Raman peak location and the calculated in-plane strain. Each blue cross represents the peak location from an individual Raman spectrum measured from the Ge grown on a crystalline Si substrate. The strain from these devices was calculated to be $0.13 \pm 0.03\,\%$. The red crosses are the peak locations of individual Raman measurements of Ge grown on amorphous Si with a calculated strain of $0.26 \pm 0.05\,\%$.

The black data points are the peak locations from the Ge grown on 2D GCLG substrates, with a calculated strain of $0.89 \pm 0.37\,\%$. The data for the Ge grown on 2D GCLG substrates is further broken up into two distinct categories: "Aligned" and "Staggered". These are two different device designs, as outlined in Section 2.3. The aligned devices have amorphous silicon nucleation seeds aligned on both sides of the

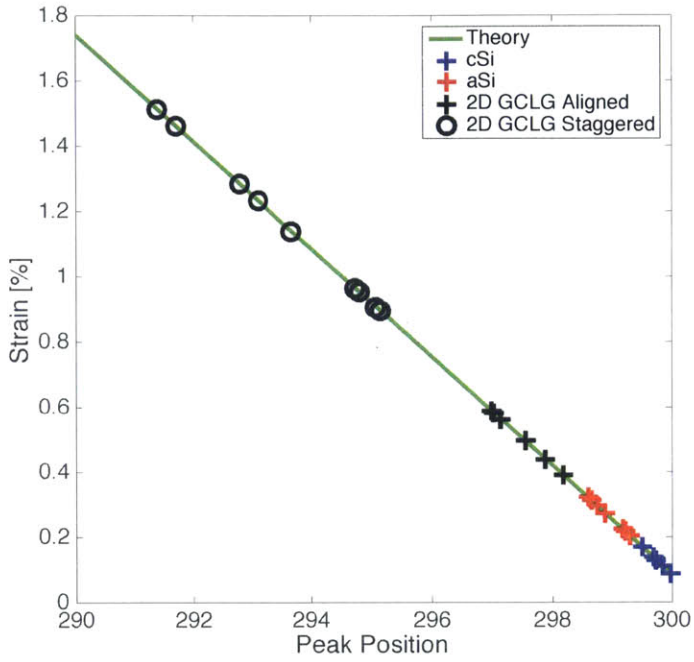


Figure 3-4: Summary of strain measurements from Raman spectra. Ge on 2D-GCLG substrates show largest peak shift and largest distribution of strains. The results have two distinct clusters. One is from the aligned seeds, which exhibit a relatively low tensile strain .The second cluster is from the staggered seeds, which exhibit very large tensile strains.

waveguide trench. Therefore, there must be a Ge grain boundary down the center of the entire trench, in addition to the grain boundary resulting from the coalescence of neighboring grains. The staggered devices have nucleation seeds that are staggered. The staggered devices eliminate the grain boundary down the center of the trench, and only have grain boundaries where the adjacent grains coalesce. From Figure 3-4, it is clear that the devices with aligned seeds have a less strain than the devices with a staggered seed design. In addition, the devices with the aligned seeds have a narrower distribution in strains when measuring different grains within the device. When only considering the devices with the aligned seeds, the measured strain is $0.51 \pm 0.08\,\%$.

In standard epitaxy processes, the lattice mismatch between the thin film and the substrate can be a significant source of strain [80,81]. However, it has been shown that the strain in Ge from epitaxy on Si is largely dominated by the thermal expansion mismatch between Ge and the substrate that it is grown on [3]. The in-plane biaxial strain created from thermal expansion mismatch can be predicted by:

$$\varepsilon_{\parallel} = \Delta\alpha\Delta T \tag{3.7}$$

where:

$\varepsilon_{\parallel}$ = In-Plane Strain
$\Delta\alpha$ = $\alpha_{\mathrm{Ge}} - \alpha_{\mathrm{sub}}$
α_{Ge} = Coefficient of Thermal Expansion of Germanium (5.6 ppm/°C)
α_{sub} = Coefficient of Thermal Expansion of Substrate
ΔT = $T_{\mathrm{g}} - T_{\mathrm{r}}$
T_{g} = Growth Temperature (450 °C)
T_{r} = Room Temperature (20 °C)

In the specific case of Ge on Si epitaxy, the resulting strain in the Ge is tensile. This is because Ge is nearly relaxed at the elevated growth temperature. When the Ge cools from the growth temperature down to room temperature, the Ge tries to contract significantly, due to the large thermal expansion coefficient. However, the coefficient of thermal expansion of Si is much smaller, and the Si contracts much less than the Ge as it cools. Since the Ge and Si are well bonded and the Si substrate is much thicker than the Ge film, the displacement of the substrate dominates the displacement of the entire structure. This means that the Ge film cannot contract as much as it would naturally, which results in a tensile strained Ge film. The resulting strain in the Ge is dependent on the growth temperature, as well as the coefficient of thermal expansion of the substrate that the Ge is grown on. A summary of the biaxial tensile strains is shown in Table 3.1.

From Table 3.1 it is clear that crystalline Si, amorphous Si, and SiO_2, the three substrates that Ge was grown on, all have a lower coefficient of thermal expansion than

Table 3.1: Summary of strain measurements using Raman spectroscopy.

Substrate	**c-Si**	**a-Si**	**2D GCLG (Aligned)**
α_{sub} [ppm/°C]	2.6	1.0	0.56
$\varepsilon_{\parallel}$ [%] (Predicted)	0.14	0.21	0.23
$\varepsilon_{\parallel}$ [%] (Measured)	0.13 ± 0.03	0.26 ± 0.05	0.51 ± 0.08

Ge. Therefore, the expected strain in the Ge is always tensile. The predicted strain listed in the table is calculated from Equation (3.7). The measured strain is from the Raman measurements. The devices with crystalline Si and amorphous Si substrates both have a measured strain that is within one standard deviation of the predicted strain. Therefore, the thermal expansion mismatch model is an accurate predictor of strain for these samples. However, the Ge grown on the 2D GCLG substrates has a measured strain that is approximately twice as large as the model predicts. This discrepancy creates uncertainty that either the Raman technique is yielding incorrect strain (breakdown of the assumptions made in Equations (3.4) and (3.5)), or that there is another mechanism that is creating significantly greater strain in the Ge than thermal expansion mismatch alone. Therefore, an additional measurement technique is vital in order to verify the strain measurements obtained from Raman spectroscopy.

3.3 Using Photoluminescence to Measure Strain

In order to understand whether there is an inaccuracy in the strain measured from the Raman, or if there is an additional source of strain in the Ge on 2D GCLG substrates, an additional technique must be employed in order to verify that the measured strain is accurate. As mentioned in Section 3.1, optical techniques provide the best trade-off between spatial resolution, strain sensitivity, and ease of sample preparation.

Photoluminescence (PL) was utilized as an additional optical measurement method in order to verify the magnitude of strain measured from Raman spectroscopy. Like

Raman spectroscopy, PL can be performed though a microscope objective, and therefore can be localized to a spot size of approximately 1 µm. It is a non-destructive technique that measures the luminescence spectrum of a sample, which can be correlated to the band gap of the material, which is dependent on the strain state of the material.

3.3.1 Theory

Photoluminescence is the re-emission of a photon after a material absorbs a photon of higher energy. If the incident photon has an energy greater than the band gap of the material, then an electron can be excited from the valence band to the conduction band, creating an electron-hole pair. The excited electron rapidly thermalizes to the bottom of the conduction band, before it is eventually re-emitted. The time that it takes for the electron to recombine and emit light is dependent on the carrier lifetime, which is a material property. The spectrum of the emitted light is dependent on the band gap, the density of states of the valence and conduction bands, as well as the temperature of the material. The PL spectrum can be approximated by [82]:

$$I\left(E_{\mathrm{ph}}\right) = C \cdot \sqrt{E_{\mathrm{ph}} - E_{\mathrm{g}}} \exp\left(-\frac{E_{\mathrm{ph}} - E_{\mathrm{g}}}{k_{\mathrm{B}}T}\right) \tag{3.8}$$

where:

I = Photoluminescence Intensity
E_{ph} = Emitted Photon Energy
C = Constant
E_{g} = Band Gap
k_{B} = Boltzmann Constant
T = Temperature

The constant C is a function of the effective masses of the electrons and holes. The constant therefore takes into account the curvature of the conduction and valence bands for the density of states term. The square root part of the spectrum originates

from the density of states, while the exponential portion of the equation arises from the Boltzmann approximation of the Fermi-Dirac distribution, which determines the occupancy of states. The intensity of the spectrum has a sharp rise at E_g from the density of states term, and then exponentially decays due to the Boltzmann term. The width of the spectrum is approximately $k_B T$. Therefore, the leading edge of the PL spectrum can be used to determine the band gap of the material [83–85].

Germanium is an indirect band gap material, and therefore the PL spectrum will be a convolution of emission from recombination from the indirect band gap (0.66 eV) and the direct band gap (0.8 eV). Recombination from an indirect band gap is a phonon mediated transition, meaning that a phonon is required in order to preserve the conservation of momentum. This process requires three particles: an electron, hole, and a phonon. Recombination from a direct band gap, requires only two particles, an electron and hole. Therefore, the probability of the two particle process occurring is significantly greater than the probability of the three particle process occurring. This means the emission rate from the direct transition is significantly greater than the emission rate from the indirect transition. Consequently, the PL intensity from the direct band gap will be significantly greater than the intensity from the indirect band gap. This has been experimentally observed especially in Ge grown on Si, which is both tensile strained and posesses growth induced defects [86]. Therefore, the PL spectrum is dominated by recombination from the $\mathbf{k} = \mathbf{0}$ direct band gap of the material.

The band gap of a material is not a fixed property, but it changes as a function of strain. Deformation potential theory can be used to calculate how the band gap changes with strain, as developed by [87]:

$$E_g^{\Gamma}(lh, \varepsilon_{\parallel}) = E_g^{\Gamma}(0) + a(\varepsilon_{\perp} + 2\varepsilon_{\parallel}) + \frac{\Delta_0}{2} - \frac{1}{4}\delta E_{100} - \frac{1}{2}\sqrt{\Delta_0^2 + \Delta_0 \delta E_{100} + \frac{9}{4}(\delta E_{100})^2} \quad (3.9)$$

$$E_g^{\Gamma}(hh, \varepsilon_{\parallel}) = E_g^{\Gamma}(0) + a(\varepsilon_{\perp} + 2\varepsilon_{\parallel}) + \frac{1}{2}\delta E_{100} \tag{3.10}$$

where:

$E_g^{\Gamma}(lh, \varepsilon_{\parallel})$	= Band Gap at Γ Valley ($\mathbf{k} = \mathbf{0}$) from Light Hole Valence Band
$E_g^{\Gamma}(hh, \varepsilon_{\parallel})$	= Band Gap at Γ Valley ($\mathbf{k} = \mathbf{0}$) from Heavy Hole Valence Band
$\varepsilon_{\parallel}$	= In-Plane Strain
$\varepsilon_{\perp}$	= Strain Perpendicular to Film Surface
$E_g^{\Gamma}(0)$	= Direct Band Gap ($\mathbf{k} = \mathbf{0}$) of Unstrained Ge (0.8 eV)
a	= Dilational Deformation Potential (−8.97 eV)
b	= Devitorial Deformation Potential (−1.88 eV)
Δ_0	= Split-Off Energy (0.29 eV)
δE_{100}	= $2b(\varepsilon_{\perp} - \varepsilon_{\parallel})$

Equations (3.9) and (3.10) show that the direct band gap changes as a function of strain. Further, it shows that the degeneracy of the light hole and heavy hole valence bands is eliminated as the material becomes biaxially strained. With the presence of strain, the ($\mathbf{k} = \mathbf{0}$) transition breaks its degeneracy and the electrons can relax from the conduction band to either the heavy hole or the light hole valence band. Since the lowest energy states are always preferentially occupied, the conduction band electrons will preferentially recombine into whichever valence band provides a smaller band gap for a given strain state. These equations again assume that the Ge is biaxially strained. Once the band gap is determined from the onset of the PL spectrum, the band gap can be correlated with the expected strain, and therefore the strain state of the material can be determined from the PL spectrum.

3.3.2 Experimental Methods

The photoluminescence technique was used to determine the strain state of the same three samples as shown in Figure 3-1. The same HORIBA Jobin Yvon LabRAM HR bench-top system that was used to measure Raman was used to measure PL. A 1064 nm laser was used as the excitation source, magnified by a 100x microscope

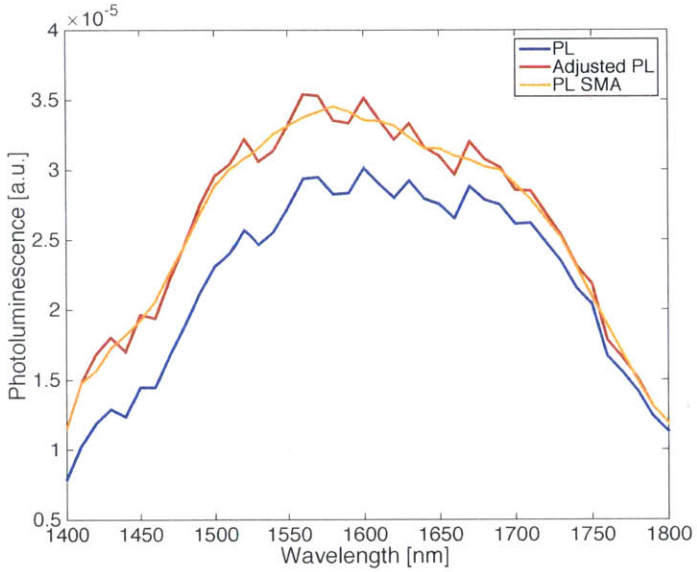
objective, to achieve an illumination spot size of approximately 2 µm. The intensity of the incident laser was reduced in power by a neutral density filter with an optical density (OD) of 1. A chopper was used, in sync with a lock-in amplifier in order to increase the signal-to-noise ratio of the acquired PL spectrum. An obscure frequency of 187.27 Hz was used for the chopper and lock-in amplifier in order to eliminate any potential noise from other alternating signals in the vicinity. Since the emission spectrum from Ge is not absorbed in a Si CCD, an InGaAs PMT detector was used in order to acquire the spectrum.

An example of the raw photoluminescence data is shown in the blue line in Figure 3-5a. The InGaAs detector does not have a constant responsivity across the broad spectrum, so the responsivity of the PMT was taken into account to adjust the PL to it's actual emitted spectrum, as shown in the red line. Since undoped Ge is not a strong light emitter, the PL spectrum had a relatively low signal to noise ratio. Therefore, the data was smoothed by using a simple moving average (SMA) in order to clean up the spectrum. This smoothed spectrum is shown in the orange line.

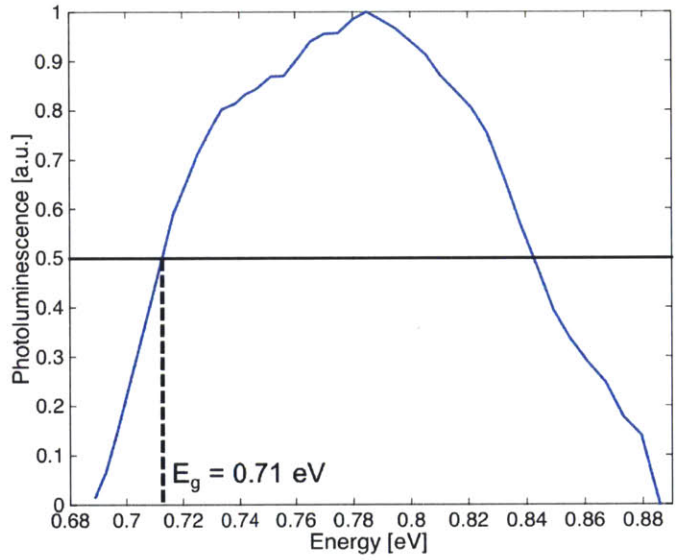
In order to determine the band gap from the PL spectrum, the units were converted from wavelength to energy by using $E = hc/\lambda$ which can be simplified to $E[\text{eV}] = 1240/\lambda[\text{nm}]$. Since the absolute intensity of the spectrum is not important, the spectrum was normalized. This final spectrum is plotted in Figure 3-5b. When the PL spectrum is plotted on the energy scale, the sharp rise in intensity on the low energy side of the spectrum is caused by the rapid increase in density of states above the band gap of the material, as explained in Equation (3.8). Therefore, the band gap was approximated by determining the energy at which the PL intensity reaches 50 % of its maximum intensity.

3.3.3 Photoluminescence Results

Photoluminescence spectra were acquired from the Ge waveguides grown selectively on crystalline silicon, amorphous silicon, and 2D GCLG substrates. The PL spectra



(a) Photoluminescence spectrum as aquired (blue), then adjusted for detector responsivity (red), then filtered using a simple moving average (SMA, in orange).



(b) Normalized photoluminescence spectrum, converted to energy scale. Band gap is determined from where spectrum rises above 50 % of the maximum signal.

Figure 3-5: Technique for determining band gap from photoluminescence spectrum.

from Ge on crystalline Si was repeatable and regular, just as the Raman spectra from the same samples were. The band gap from Ge on crystalline Si was determined to be $0.78 \pm 0.003\,\text{eV}$.

Unfortunately, the emission intensity from the Ge on amorphous Si was too weak to be able to collect reliable PL spectra. The Ge on amorphous Si was small grain polycrystalline material. Since grain boundaries can serve as recombination centers, the non-radiative recombination rate dominated the recombination process, and there was not enough radiative recombination to measure a reliable spectrum. Therefore, the band gap of the Ge on amorphous Si was not determined.

The Ge grown on 2D GCLG substrates emitted strongly enough to acquire PL spectra from the sample. Similar to the Raman spectra acquisition technique, the measurements were made in different grains within the same waveguide trench, as well as in different waveguides. The emission spectra occasionally contained multiple peaks within the same spectrum. The reason for this is the same as the reason there were multiple peaks in the Raman spectra, as explained in Section 3.2.3. The incident spot size was large enough to simultaneously probe multiple Ge grains. The adjacent grains may have different strain states, therefore different band gaps, which results in different PL peaks. A band gap of $0.73 \pm 0.02\,\text{eV}$ was measured on the aligned seed devices from the Ge grown on 2D GCLG substrates. The band gap was shifted to significantly lower energies than the Ge on crystalline Si. The standard deviation of the band gap is also an order of magnitude greater, signifying that the Ge on 2D GCLG substrates exhibits a range of different strain states.

The band gap measured from the PL spectra was then used to determine the in-plane strain of the Ge. In Figure 3-6, the band gap of Ge is plotted as a function of in-plane strain. With the addition of tensile strain, the light hole valence band moves towards the conduction band more quickly than the heavy hole valence band. Therefore the transition from the conduction band to the light hole valence band is more probable, since holes will preferentially occupy the light hole valence band. There

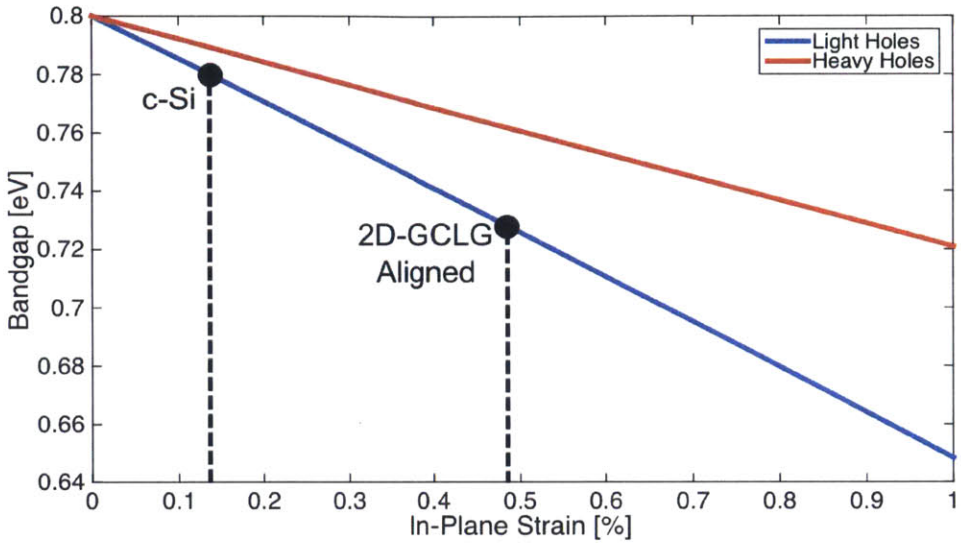


Figure 3-6: Using Equations (3.9) and (3.10), the band gap can be plotted as a function of strain. Assuming the photoluminescence signal is from the smallest energy gap, the strain can be determined by correlating the measured band gap to the band gap of the light hole valence band.

may be radiative emission from both transitions, which broadens the PL spectrum. It may also give the appearance of multiple peaks within the same spectrum. However, the rise of the PL spectrum at low energies is due to the emission from the low energy transition, which is due to the transition from the light hole valence band. Therefore, the band gap measured from the PL spectra can be correlated to the in-plane strain by determining at what strain the light hole valence band gap is equivalent to the measured band gap.

The resulting in-plane strain was calculated to be $0.12 \pm 0.02\,\%$ for the Ge on crystalline Si, and $0.49 \pm 0.14\,\%$ for the Ge on 2D GCLG substrates with aligned seeds. Figure 3-7 summarizes the in-plane strain measured from the two different optical methods, and compares them with the strain predicted from the thermal strain model. For the Ge gown on crystalline Si, the predicted strain is within one standard deviation of the strain measured from both optical techniques. This is a strong indication that the source is strain in the Ge is the mismatch between the coefficients

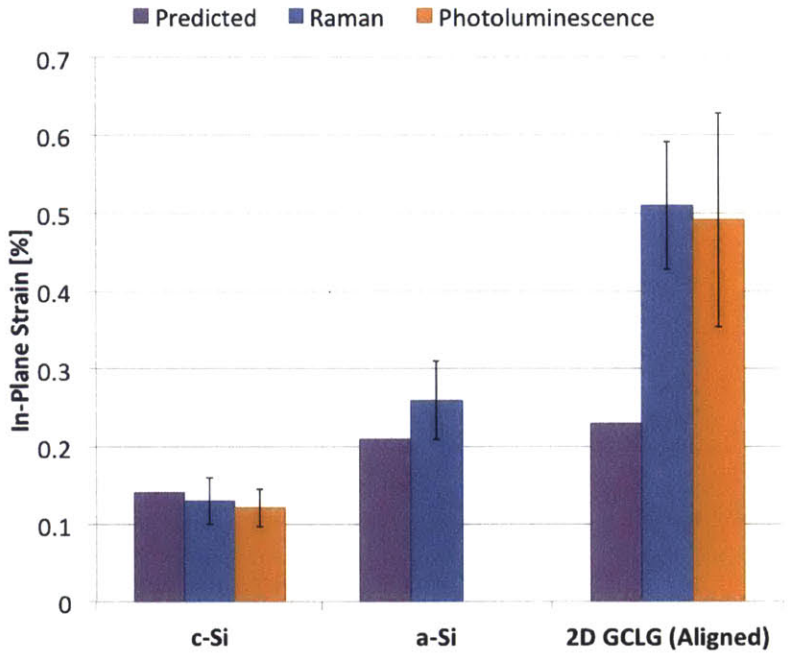


Figure 3-7: Summary of the strain measured from Raman and photoluminescence. The measured strain aligns with the strain predicted from theory for the samples on crystalline Si (c-Si) and amorphous Si (a-Si). However the strain measured in the Ge on 2D GCLG samples is approximately double the predicted strain.

of thermal expansion of the Ge and the substrate. The PL method was ineffective for the Ge grown on amorphous Si, so the strain was only measured by Raman. For this sample, the predicted strain is within one standard deviation of the measured strain, indicating that the thermal strain model holds for both substrates. However, the model is ineffective in accurately predicting the in-plane strain for the Ge grown on 2D GCLG substrates. The strain measured from the PL method correlate well with the strain measured from Raman, which verifies the measured results to be accurate, yet, the measured strain is approximately twice as large as the model predicts. The two measurement techniques verify that the actual in-plane strain is known to be 0.5 %, however source of the high in-plane tensile strain is not understood.

3.4 Determining the Source of High Tensile-Strain

Raman spectroscopy and photoluminescence were used in order to measure the in-plane tensile strain of Ge grown on crystalline Si, amorphous Si, and 2D GCLG substrates. The thermal strain model presented in Equation (3.7) accurately predicts the strain present in the Ge on crystalline Si and amorphous Si, but the Ge grown on 2D GCLG substrates has a strain that is approximately twice as large as the predicted strain. Therefore, there is a physical mechanism that is magnifying the strain in the Ge on 2D GCLG samples. Understanding the source of the strain is critical for determining the expected strain for different Ge growth conditions and device designs. The strain state effectively determines the dislocation density, which affects the device performance. Therefore, the source of strain must be understood in order to effectively design high performance photodetectors.

3.4.1 Void Formation from Grain Coalescence

In order to determine the source of strain present in the Ge grown on 2D GCLG substrates, the physical structure of the Ge filled trench was examined. The SEM image in Figure 3-8 shows a bird's eye perspective of a Ge on 2D GCLG device with aligned seeds. In this device the Ge grains have coalesced to fill the waveguide trench, and have overgrown the trench. For the final photodetector device, the Ge will be planarized, but this image is taken before planarization. The ridges adjacent to the Ge-filled trench are caused by the amorphous Si nucleation seeds. The amorphous Si seeds are buried by a blanket SiO_2 film which adopts the physical shape of the amorphous Si lines below it. This image shows that the Ge grains have fully coalesced to fill the trench.

Plan-view SEM images are not capable of fully showing what is happening to the plane where neighboring Ge grains coalesce. Cross-sectional images of the Ge waveguide trench can show whether or not the neighboring grains have fully coalesced.

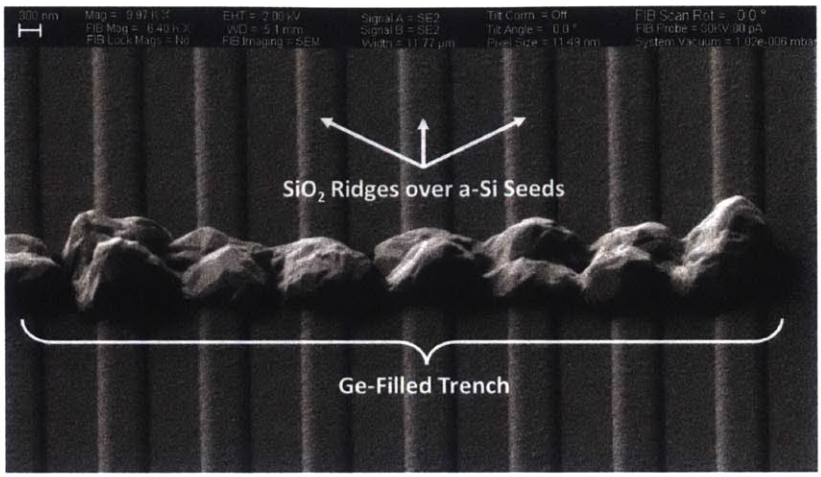


Figure 3-8: SEM image of a Ge-filled trench from a bird's eye perspective. The Ge has been grown on a 2D-GCLG substrate. The ridges in the surrounding area are from the SiO_2 overlaying the patterned amorphous Si nucleation seeds.

With a trench width of 1 µm, it is not possible to accurately cleave the sample down the middle of the trench in order to image the Ge coalescing fronts. Therefore, a focused ion beam (FIB) was used to selectively mill away material in order to view the cross-section of the trench.

By selectively milling away material and imaging the sample from an angle, it is possible to see the cross section of the device, as shown in Figure 3-9. The silicon wafer is seen at the bottom, which was used as a substrate. Above that, the SiO_2 can be seem, which was used as a pseudo-substrate in order to simulate the dielectric material within the metal interconnect stack of an integrated circuit. There are undulations in the SiO_2 thickness, which are a product of fabrication errors. When the SiO_2 trench was defined and etched, the amorphous Si seed lines were still present. The SiO_2 was over-etched, which etched into the SiO_2 pseudo-substrate. Some of the SiO_2 was protected by the a-Si seeds, and did not get etched. Therefore the undulations in thickness of the SiO_2 pseudo-substrate was caused by the over-etch of the oxide trench, while some of the material was protected by the a-Si seeds. The coalesced Ge grains are seen above the oxide layer. The top surface of the Ge has been roughened from the exposure to the ion beam while focusing.

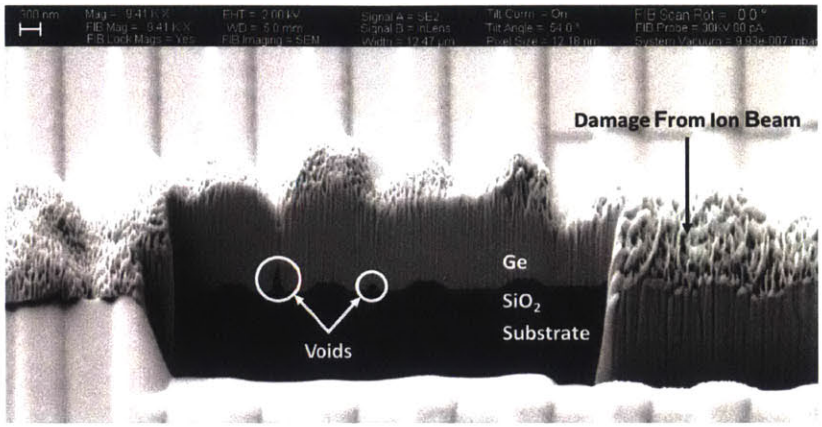


Figure 3-9: SEM image of the cross-section of Ge-filled trench. The cross section was obtained by FIB milling. Voids are seen at some of the regions where the coalescence of neighboring Ge grains was incomplete.

In the cross-section image, it is evident that the Ge has not perfectly coalesced at all locations. Small voids are seen at the interface between coalescing Ge grains. The voids are present at the bottom of the SiO_2 pseudo-substrate undulations, indicating that the fabrication problems may have enhanced the probability of void formation. The presence of voids in a strained material can act as stress/strain concentrators, increasing the local stress and strain in the material [88]. The voids in the Ge may be providing the same effect, and increasing the local strain. This can be the source of the increased strain, as measured by the optical techniques.

3.4.2 Modeling Strain With the Presence of Voids

In order to determine whether or not the voids are the source of the high tensile strain measured, their effect was quantified. When the cross section of the Ge on 2D GCLG substrates is examined closely, several voids are observed. The typical voids are approximately triangular with a width of 100 nm and a height of 100 nm and are located at the interface of the Ge and the SiO_2 pseudo-substrate. The voids are formed from the lack of complete coalescence from adjacent Ge grains.

COMSOL Multiphysics was used in order to quantify the effect of voids on the

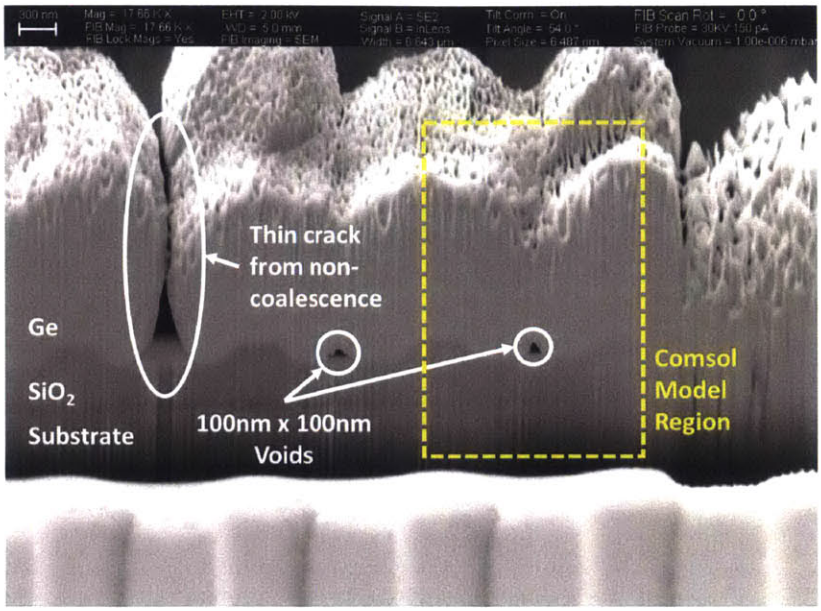


Figure 3-10: SEM image of the cross-section of Ge-filled trench. The cross section was obtained by FIB milling. Small voids are seen with dimensions of approximately 100 nm by 100 nm at the interface between adjacent Ge coalescing grains, and the SiO_2 pseudo-substrate. COMSOL was used to determine how the presence of voids affects the strain state with the modeled region indicated by the yellow box.

strain state of the Ge. A 1 µm layer of Ge on 0.5 µm SiO_2 on 500 µm thick crystalline Si substrate was the device structure which was modeled. This model region is represented in Figure 3-10.

The COMSOL Multiphysics model is a finite element solver in which the 3D geometry is initially designed and the material properties are defined. The simulation is based on defining the geometry at 450 °C and then cooling the model to 20 °C. The thermal strain is then calculated and the two-dimensional cross section of the device is displayed in the top row of Figure 3-11. In addition to the in-plane strain, the resolved shear stress was also calculated, and displayed in the bottom row of Figure 3-11. As a reference, the strain was calculated in a sample without any voids. This sample is indicated in the first column and serves as a baseline strain. Then, triangular voids with different geometries are added to the interface between the Ge and the SiO_2 to determine their effect on the in-plane strain. The multiplier in the top of of each

figure is an indication of how much larger the maximum strain is in the device with a void as compared to the baseline device without voids. The multiplier is a function of void geometry, but it is evident that the presence of a void significantly increases the maximum in-plane strain in the Ge. The void geometry observed in the cross section image showed a void with dimensions of 100 nm by 100 nm. This geometry increases the maximum in-plane strain by 1.9x, nearly double the strain calculated for the baseline Ge without voids. Wider void geometries increase the maximum in-plane strain by a factor of 2.9x, nearly tripling the strain compared to the baseline. In addition to the increase of in-plane strain, the resolved shear stress also increases with respect to the baseline by a factor of 1.4x.

The strain measured by in the Ge on 2D GCLG substrates by Raman spectroscopy and photoluminescence was approximately twice as large as the thermal strain model predicted. This factor of two increase can be accounted for by the stress and strain concentration around the voids formed from coalescing adjacent Ge grains. Therefore, the source of the strain is still based on the difference in coefficients of thermal expansion between the Ge and the substrate it is grown on, but it is also magnified by the presence of voids. The void geometry affects the magnitude of the maximum in-plane strain, as summarized by the plots in Figure 3-12. The magnitude of the maximum in-plane strain is shown to be a strong function of geometry, with cases with a short wide void maximizing the strain. The maximum strain is shown to increase to above 1 %, which is significantly greater than the strain predicted by the thermal strain model. However, the Ge grown on 2D GCLG substrates have in-plane strains measured to be in excess of 1 % when using a staggered seed device design, as shown in Figure 3-4. Therefore, the magnitude of measured strain can also be used to gather insight to the geometry of the underlying voids.

When Ge is grown epitaxially on crystalline Si, there is no reason to expect the formation of voids. The Ge nucleates uniformly on the Si substrate, and then grows vertically by extension of atomic steps, and grows monolayer by monolayer. This

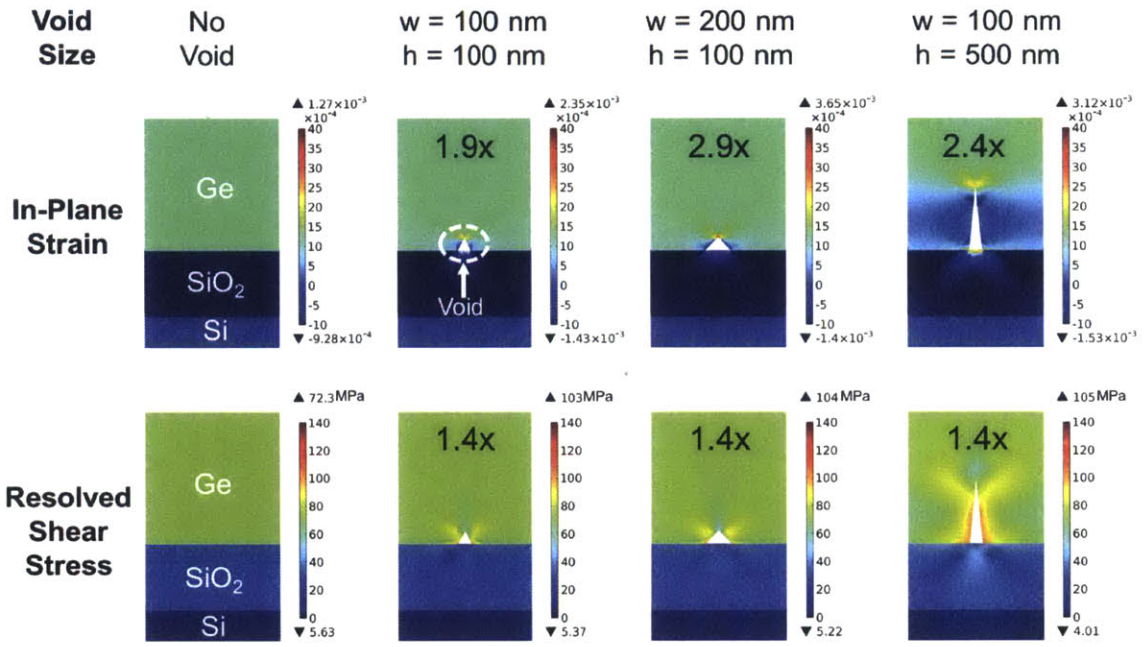
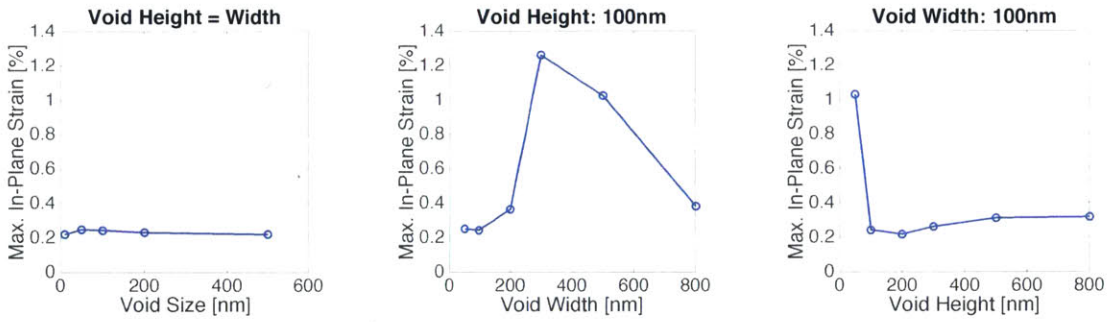


Figure 3-11: Calculated in-plane strain on the top row, and resolved shear stress in the bottom row. The results were calculated using COMSOL. The multiplier in each image indicates how much larger the maximum strain/shear is in the sample with a void, as compared to the baseline without voids.



(a) Maximum in-plane strain assuming a triangular shaped void with equal height and width dimensions.

(b) Maximum in-plane strain assuming a triangular shaped void with a fixed height of 100 nm and a varying width.

(c) Maximum in-plane strain assuming a triangular shaped void with a fixed width of 100 nm and a varying height.

Figure 3-12: Summary of the maximum in-plane strain as a function of void geometry. The results were calculated using COMSOL Multiphysics.

type of epitaxial growth does not lead to void formation since there are no grains to coalesce. The Ge grown on amorphous Si is similar to the Ge grown on crystalline Si. The Ge nucleates on the Si at the bottom of the trench and grows in the normal direction. There is minimal lateral growth of grain boundaries, which is the source of void formation in Ge on 2D GCLG substrates. Without the presence of voids, there is no strain concentration and the in-plane strain is expected to directly follow the thermal strain model for these samples.

3.5 Dislocation Generation in Strained Germanium

The Ge on 2D GCLG substrates was measured to be significantly tensile strained. However, the nucleation of dislocations is dependent on the magnitude of shear stress. Therefore, the shear stress of the Ge must be determined from the strain state. The resolved shear stress can be calculated from the in-plane stress with the following equation:

$$\tau = \sigma \cos\phi \cos\lambda \tag{3.11}$$

where:

τ = Resolved Shear Stress
σ = In-Plane Stress
ϕ = Angle Between Slip Plane Normal and Tensile Axis
σ = Angle Between Slip Direction and Tensile Axis

In Equation (3.11) the product $\cos\phi\cos\lambda$ is called the Schmid Factor, and is maximized when $\phi = \lambda = 45°$. For the case of Ge grown on 2D GCLG substrates, the exact orientation of the Ge grains is unknown. Therefore, it is impossible to know the orientation of the dislocation slip planes and directions with respect to the in-plane strains. A worst case scenario can be explored, in which the Schmid Factor is at a maximum, in order to determine the maximum possible shear stress.

In addition, the in-plane stress was not directly measured, the in-plane strain was measured. Therefore, the maximum possible shear stress in can be calculated from the in-plane strain by the following:

$$\tau_{\max} = \frac{\sigma}{2} = \frac{E\varepsilon_{\parallel}}{2} \tag{3.12}$$

where:

τ = Maximum Resolved Shear Stress
σ = In-Plane Stress
E = Young's Modulus
$\varepsilon_{\parallel}$ = In-Plane Strain

This maximum shear stress is not expected to be the actual shear stress present in the Ge. This is only the worst case scenario in which the angles between the slip plane, slip direction, and in-plane strain are 45°, and therefore the Schmid Factor is maximized. Since the Ge grains nucleate randomly on the amorphous Si, their precise grain orientation is randomized. Therefore the orientation of slip direction and slip plane with the in-plane stress is not known. The maximized Schmid Factor is only considered in order to examine the worst case scenario. If the worst case scenario does not generate dislocations, then dislocations are not expected to form given realistic conditions.

If the resolved shear stress in the Ge is greater than the critical resolved shear stress (CRSS) then the strain energy becomes large enough to induce plastic deformation. The nucleation of dislocations requires the motion of atoms in the crystal, and is therefore a thermally activated process. This means that the CRSS is a function of temperature, as plotted in Figure 3-13. The red circle plots the maximum resolved shear stress in the Ge grown on SiO_2, as calculated from Equation (3.12). Since the source of strain is thermal expansion mismatch between the Ge and the substrate, magnified by the presence of voids, the strain and the stress can be assumed to be linear with temperature and fully relaxed at the growth temperature of 450 °C.

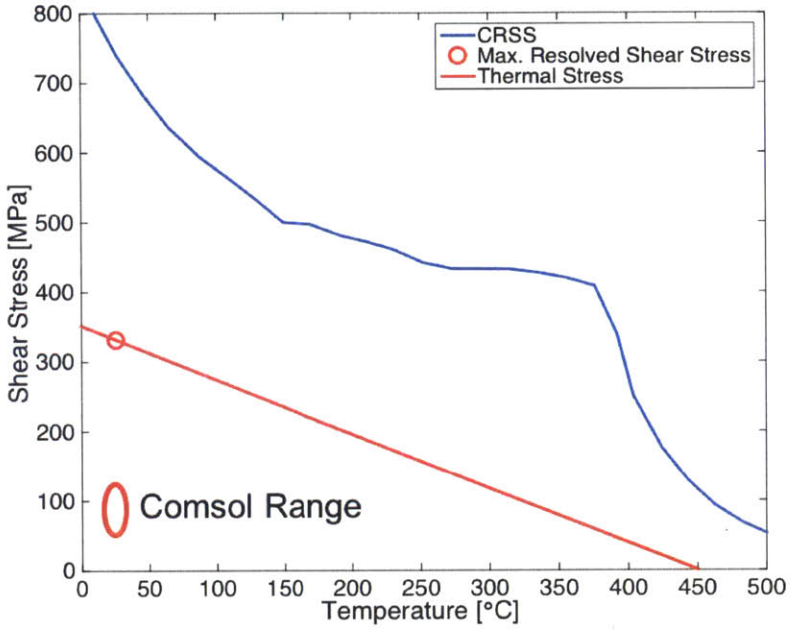


Figure 3-13: Maximum shear stress as a function of temperature. The blue line indicates the critical resolved shear stress (CRSS). The red circle indicates the maximum possible resolved shear stress present in the Ge on SiO_2. The red line indicates the maximum resolved shear stress as a function of temperature, as the samples cools from growth temperature. The red oval indicates the resolved shear stress that is actually expected, from the COMSOL results. The resolved shear stress is always less than the CRSS, indicating that no dislocation generation occurs.

Therefore, the red line plots the shear stress as a function of temperature as it cools to room temperature after growth. This line assumes a maximized Schmid factor, which is a worst case scenario. The actual shear stress is expected to be below the red line and the shear stress calculated by COMSOL is indicated in the red oval.

From Figure 3-13 it is evident that the shear stress in the Ge is always lower than the critical resolved shear stress. This means that the shear stress is never large enough to initiate plastic deformation. Therefore, dislocations are not expected to form in the Ge grown on SiO_2 despite the large in-plane strain measured in these devices. The defect states in this material are not dominated by dislocations, but by the concentration of point defects and grain boundaries, which can be designed around, as discussed in Chapter 2.

3.6 Effect on Absorption Spectrum

The presence of tensile strain can reduce the band gap of Ge, as shown in Section 3.3. The photoluminescence spectra from strained Ge on SiO_2 was used in order to show the reduction in band gap energy which correlates to a shift in the luminescence spectrum towards lower energies, or longer wavelengths. While photoluminescence is based on a spontaneous emission process, optical absorption is a similar process, but in reverse. Therefore, the shift in the photoluminescence spectrum towards longer wavelengths also corresponds with a shift in the absorption spectrum towards longer wavelengths, as can be seen in Figure 3-14.

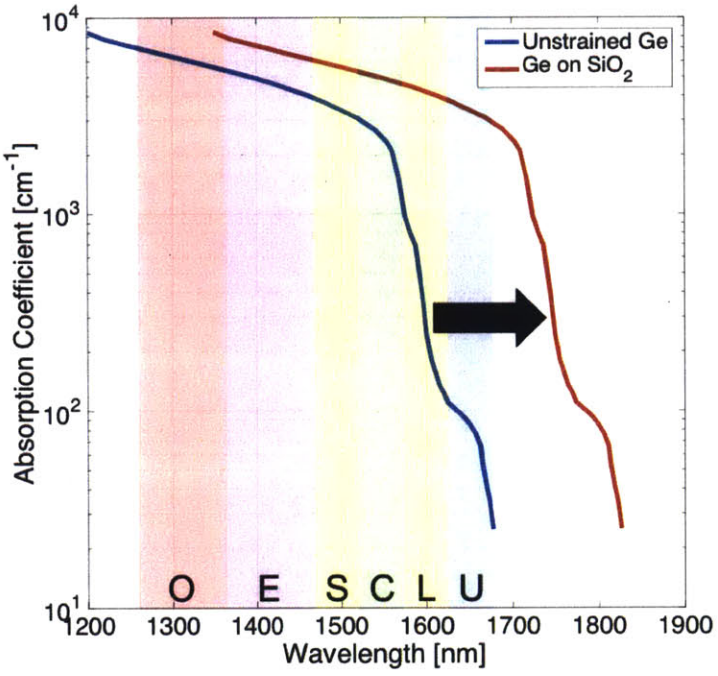


Figure 3-14: Absorption coefficient of unstrained Ge plotted with the simulated absorption spectrum of tensile strained Ge. The colored segments correspond with different telecom bands.

In Figure 3-14, the blue line plots the measured absorption coefficient on unstrained

Ge. The red line plots the simulated absorption coefficient of the tensile strained Ge on SiO_2. From photoluminescence, the band gap was measured to be shifted from 0.8 eV to 0.73 eV. Therefore, the absorption spectrum can be assumed to shift towards lower energies by 0.07 eV. In reality, the splitting of the light hole and heavy hole valence bands would cause a kink in the spectrum, but the general trend holds true.

While unstrained Ge is an excellent absorber at 1550 nm and across the C band, it is a relatively weak absorber in the L and U bands. However, the strained Ge has an absorption spectrum that is shifted towards longer wavelengths and therefore is an effective absorber across the entire telecom window. Therefore the strained Ge can be used as the sole photodetector for all telecom applications. In addition, at 1550 nm, the absorption length is reduced from 4 µm to 2 µm. This means that very small compact photodetectors can be utilized while still absorbing all of the light. Smaller photodetectors have a lower capacitance and are therefore suited for higher speed operation. Therefore, the presence of tensile strain in the Ge does not generate deleterious dislocations, but instead increases the absorption coefficient and allows for the design of compact high-speed detectors.

3.7 Summary

In this chapter the strain state of selectively grown germanium was determined experimentally. Optical measurement techniques were utilized in order to obtain the high spatial resolution required to analyze Ge grown in 1 µm wide trenches, as well as maintaining a simple sample preparation procedure.

Three separate samples were investigated. Each sample consisted of Ge that was selectively grown at 450 °C. Crystalline Ge was grown epitaxially on crystalline Si, small grain polycrystalline Ge was grown on amorphous Si, and large grain Ge was grown on geometrically confined SiO_2 substrates.

Raman spectroscopy was utilized in order to measure the phonon energy in the

Ge. A biaxial strain state was assumed in order to determine the in-plane strain from the phonon energy. The strain measured in Ge on crystalline Si was 0.13 ± 0.03%, the strain in Ge on amorphous Si was 0.26 ± 0.05%, and the strain in the Ge on geometrically confined SiO_2 substrates was 0.89 ± 0.37%. The orientation of the nucleation seeds was shown to be a predictor of strain, with a wide range of in-plane tensile strains measured on the devices with staggered seeds. A narrower distribution of strains at 0.51 ± 0.08% was measured for the devices with aligned seeds.

The measured in-plane tensile strain was compared to a model in which the difference in coefficient of thermal expansions between the Ge and the substrate is the cause of the strain in the Ge. The model accurately predicts the strain for Ge grown on crystalline Si and amorphous Si, but the strain measured in the Ge on geometrically confined SiO_2 substrates with aligned seeds had a measured strain approximately twice as large as predicted.

A secondary optical strain technique was employed in order to verify the large strain measured in the Ge on SiO_2. Photoluminescence was measured in order to determine the band gap of the Ge. The light emission was assumed to be from recombination from excited carriers in the conduction band to the light hole valence band at the $\mathbf{k} = \mathbf{0}$ point. The in-plane tensile strain was determined from the reduction in band gap energy. The strain measured from photoluminescence was equivalent to the strain measured by Raman spectroscopy for Ge on crystalline Si and on SiO_2. The PL emission from Ge on amorphous Si was too low in intensity to obtain reliable measurements. The equivalent strain state measured from the two techniques verified the measured strain state and determined that the strain in the Ge on SiO_2 was twice as large as predicted by the coefficient of thermal expansion mismatch model.

In order to determine the source of the large tensile strain measured in the Ge on SiO_2, the physical structure of the coalesced grains was examined. A focused ion beam was used to mill the Ge trench in half and image the center of the waveguides. Small voids were observed with an approximately triangular shape and dimensions

of approximately 100 nm by 100 nm. COMSOL Multiphysics was used to model the strain with the presence of voids. The voids were shown to act as stress concentrators, increasing the maximum in-plane strain by a factor of two or larger. Therefore, the voids were determined to be the source of the large strain.

The maximum possible resolved shear stress was calculated from the in-plane strain by assuming a maximized Schmid Factor. This resolved shear stress was compared to the critical resolved shear stress of Ge, above which dislocations become mobile. The shear stress was shown to be significantly lower than the critical resolved shear stress, and therefore it was shown that the high tensile strain is not large enough to nucleate dislocations in Ge grown using the 2D GCLG technique at 450 °C. Therefore, dislocations are not expected to be present in this material, and will not limit the final photodetector device performance.

Chapter 4

Developing Schottky Contacts to Germanium

4.1 Introduction

A metal contact is the way that a semiconductor device is typically connected to a larger circuit. The metal contact is critical for any semiconductor device. There are two main types of metal contacts, Ohmic and Schottky contacts. In an Ohmic contact, the current voltage relationship follows Ohm's Law, and is linear. In practice, an Ohmic contact has a negligible resistance with respect to the total resistance of the semiconductor device. Therefore an Ohmic contact is used to supply current to a semiconductor device without requiring an appreciable voltage drop across the contact. On the other hand, a Schottky contact is rectifying and results in the formation of a diode.

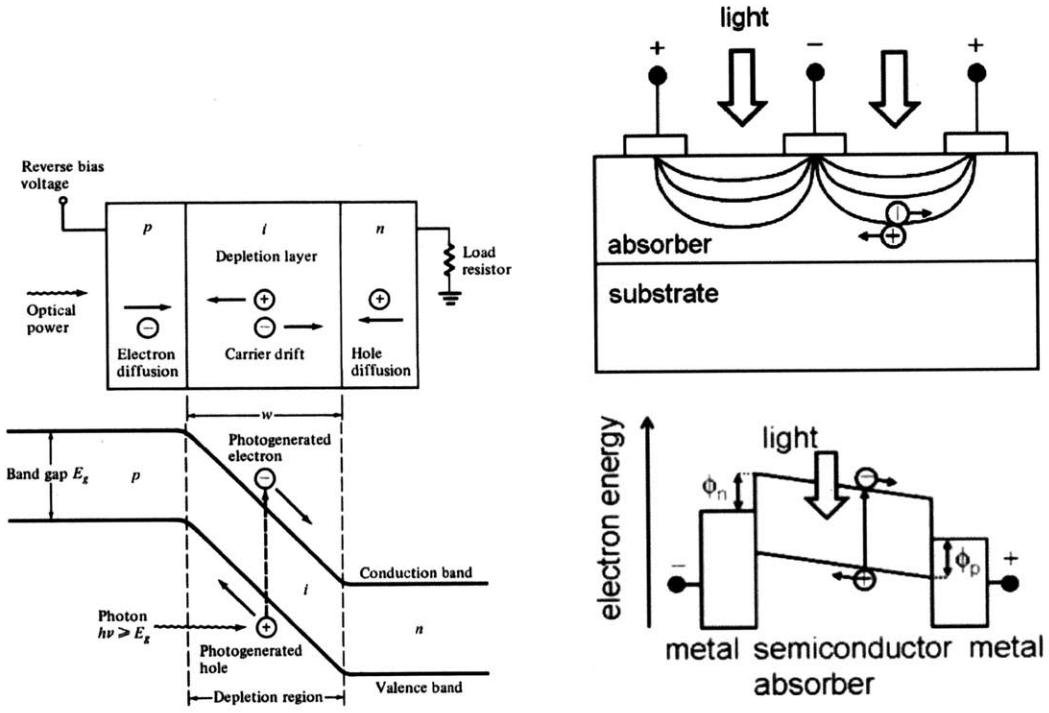
In order to determine the appropriate metal contact, the specific application must be considered. In this case, the goal is to make a photodetector and connect it to an external circuit. Two typical photodetector devices are *pin* diodes and metal-semiconductor-metal (MSM) photodetectors.

4.2 Photodetector Device Selection

Typical *pin* diode devices are similar to a standard *pn* diode, but have an added intrinsic region in the middle in order to increase the width of the depletion region. Charge separation comes from from the built-in electric field in the depletion region, and therefore a wider depletion region increases the volume of material that can contribute to current collection. This device can provide charge separation even without an externally applied bias due to the built-in electric field. Ohmic contacts are required at both the *n*-type and *p*-type regions in order to efficiently extract the photogenerated carriers. A schematic of this device is shown in Figure 4-1a.

The drawback of this device is that it requires a specific doping profile. There are two main ways to add a specific doping profile: *in situ* doping and dopant implantation. Typical *in situ* doping involves adding a specific dopant during the epitaxy process. For example, making *n*-type Ge requires the addition of phosphine gas (PH_3) in addition to germane gas (GeH_4) during the deposition process. This induces the deposition of some phosphorous on substitutional Ge sites, and therefore dopes the Ge *n*-type. However, the 2D GCLG technique utilized here (described in Chapter 2) is not a standard bottom-up growth technique, and therefore a sharp doping profile can not be realized. The alternative doping approach involves implantation of ionized dopants. After implantation, the Ge becomes significantly damaged, and therefore an annealing process must take place in order to anneal out the implantation induced defects, as well as electrically activate the dopants. However, this is a high temperature process, and therefore is not compatible with back-end-of-line processing. Therefore, a *pin* detector is not easily realized as a device structure for the BEOL photodetector.

A metal-semiconductor-metal (MSM) photodetector is a simple device which consists of a semiconductor absorber region and two metal contacts, as shown in Figure 4-1b. There is no specific doping profile required for this device, which is an advantage for back end of line integration. The metal contacts can be either Ohmic or Schottky



(a) Device schematic (top) and band structure (bottom) of a typical *pin* diode photodetector.

(b) Device schematic (top) and band structure (bottom) of a typical metal-semiconductor-metal (MSM) photodetector.

Figure 4-1: Typical photodetector device structures. From [89].

contacts. In the case of Ohmic contacts, the device becomes a photoconductor and is effectively a resistor with a resistance that is a function of optical absorption. While this device can act as a photodetector, it can have a very high leakage power in the dark, and therefore have a high power consumption. On the other hand, if Schottky contacts are used, then the dark current can be suppressed by the diode-like behavior of the contact, as described in Section 4.3. With Schottky contacts, the device is symmetric and one Schottky contact will always be in reverse bias. The reverse biased metal contact will always limit the current and therefore the MSM detector can have a significantly reduced dark current when compared to a standard photoconductor. In addition, an MSM detector can exhibit gain and have an internal quantum efficiency in excess of 100 %, as explained in detail in Chapter 5.

Due to the ease of fabrication, the back-end-of-line compatibility, gain, and dark current suppression, an MSM device structure is chosen as the ideal BEOL photodetector device structure.

4.3 Theory

In order to fabricate a metal-semiconductor-metal (MSM) photodetector, it is critical to determine the ideal metallization scheme. The entails determining an ideal pre-metallization clean, as well selecting an appropriate metal to use for the contact. In the case of a MSM photodetector, a Schottky contact is preferred to an Ohmic contact in order to suppress dark current.

When a semiconductor is brought into direct contact with a metal, their Fermi levels will align, resulting in band bending in the semiconductor. This can result in the formation of an energetic barrier that electrons must overcome while conducting from the Fermi level of the metal into the conduction band of a semiconductor. A band structure schematic of a Schottky contact is shown in Figure 4-2. The energetic barrier is called the Schottky Barrier. The presence of this barrier is what creates the rectifying properties of the contact, since carriers need to overcome the barrier by a process of thermionic emission in order to conduct from the metal to the semiconductor.

The edge of the semiconductor can have a high concentration of defect states which can become electrically charged. If the concentration of these defect states is high enough, the Fermi level can become pinned at their charge neutrality level, as discussed in Section 4.4. In addition, there can be a thin oxide layer between the semiconductor which can physically separate the metal from the semiconductor. If this is thin enough, carriers can easily tunnel though it without blocking current, as discussed in Section 4.5.

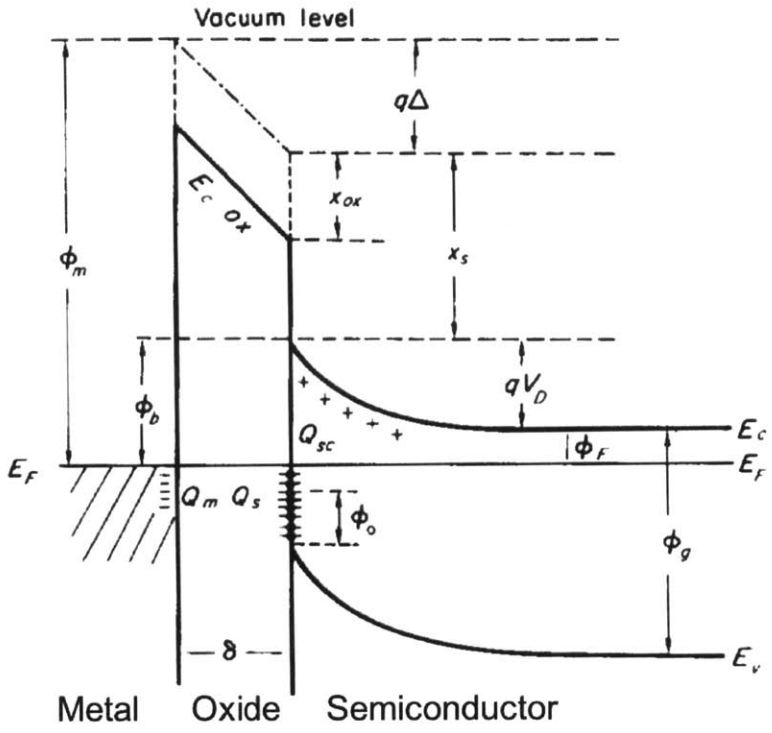


Figure 4-2: Band structure schematic of a Schottky Barrier. An n-type semiconductor is represented in this case. From [90].

where:

ϕ_{m} = Metal Work Function

ϕ_{b} = Schottky Barrier Height

ϕ_0 = Charge Neutral Level for Surface States

ϕ_{g} = Band gap of Semiconductor

E_{F} = Fermi Level

E_{c} = Conduction Band in Semiconductor

E_{v} = Valence Band in Semiconductor

χ_{ox} = Electron Affinity of Oxide or Interlayer

χ_{s} = Electron Affinity of Semiconductor

δ = Oxide or Interlayer Thickness

V_{D} = Diffusion or Built-In Potential

The basic current-voltage relationship in a Schottky diode follows the same equation as the current-voltage relationship in a standard p-n junction diode, and is represented by the Shockley equation, also known as the ideal diode law [91]:

$$I = I_s \left[\exp\left(\frac{qV}{kT}\right) - 1 \right] \tag{4.1}$$

where:

I = Current Through Schottky Diode
I_s = Reverse Bias Saturation Current
q = Elementary Charge
V = Applied Bias
k = Boltzmann Constant
T = Absolute Temperature

While the basic current-voltage relationship between a p-n junction diode and a Schottky diode is the same, the I_s reverse bias saturation prefactor is based on very different phenomenon in p-n junction diodes and Schottky diodes. In a p-n junction, the reverse bias saturation current is physically based on the thermal generation of electrons and holes in the quasi-neutral p and n-type regions. The excess carriers then diffuse to the space charge region are are swept across the depletion region due to the built-in electric field, and therefore contribute to the current flow through the diode in the dark. The dark current is a function of temperature, which is embedded in the intrinsic carrier concentration term. Increasing the temperature increases the thermal generation rate and therefore increases the intrinsic carrier concentration and the reverse bias saturation current. It can be calculated by:

$$I_s = qA\sqrt{\frac{D_p}{\tau_p}}\frac{n_i^2}{N_D} + \sqrt{\frac{D_n}{\tau_n}}\frac{n_i^2}{N_A} \tag{4.2}$$

where:

I_s = Reverse Bias Saturation Current (p-n Junction Diode)
q = Elementary Charge
A = Diode area
$D_{p,n}$ = Diffusion Coefficient for Holes and Electrons, Respectively
$\tau_{p,n}$ = Carrier Lifetime for Holes and Electrons, Respectively
n_i = Intrinsic Carrier Concentration in Semiconductor
$N_{D,A}$ = Donor and Acceptor Concentrations in n and p Side, Respectively

The fundamental source of dark current or reverse bias saturation current in a Schottky diode is very different. Physically, it is caused by thermionic emission of carriers from the metal, over the Schottky barrier, and into the semiconductor material. This thermionic emission relies is exponentially dependent on the Schottky barrier height, which is not an inherent material property, but a device property that can be modified, as discussed in this chapter. This thermionic emission has a strong dependence on temperature and on the Schottky barrier height, as shown here:

$$I_s = A\mathscr{A}^* T^2 \exp\left(-\frac{q\phi_B}{kT}\right) \tag{4.3}$$

where:

I_s = Reverse Bias Saturation Current (Schottky Diode)
A = Diode area
$\mathscr{A}^*$ = Effective Richardson's constant
ϕ_B = Schottky Barrier

In the context of a MSM photodetector, a Schottky contact is preferred over an Ohmic contact. An MSM photodetector is a symmetric device with two metal contacts and a volume of semiconductor material between them. If Ohmic contacts are used, then each individual contact responds linearly with bias and the total device effectively becomes a resistor. This is called a photoconductor. The problem with standard photoconductor devices is that they have large leakage currents when the device is in the dark. Therefore they consume a lot of power. In addition, the signal to noise ratio (SNR) is determined by the ratio of the photocurrent and the dark

current. With a very high dark current, the SNR is reduced.

If the metal contacts are changed from Ohmic to Schottky contacts, then each contact becomes a diode. Since the device is symmetric, either way the device is biased, one contact will always be in reverse bias and the other contact will be in forward bias. The total current through the device will always be limited by the reverse biased Schottky contact, and therefore the dark current of the detector will be reduced.

The metal contact should ideally form a Schottky contact in order to suppress photodetector leakage current in the dark.

4.3.1 Measuring Schottky Barrier Height

The linear relationship between current and voltage makes it trivial to determine whether or not a metal contact is Ohmic. However, when a contact shows rectifying behavior, a technique is required to quantify its properties, namely the Schottky barrier height.

It is possible to use the expression for reverse bias saturation current in Equation (4.3) to experimentally measure the Schottky barrier height. If the equation is rearranged and the logarithm is taken of each side, then the following relationship is obtained:

$$\ln\left(\frac{I_s}{T^2}\right) = -\frac{q\phi_B}{kT} + \ln(A\mathscr{A}^*) \tag{4.4}$$

where:

I_s = Reverse Bias Saturation Current
A = Diode area
$\mathscr{A}^*$ = Effective Richardson's constant
ϕ_B = Schottky Barrier

Experimentally, an I-V measurement must be performed on the diode at a series of known temperatures. I_s is directly measured from the I-V measurement in the

reverse bias condition. If Equation (4.4) is plotted with $\ln(I_s/T^2)$ on the y-axis and $1/T$ on the x-axis, then the y-intercept of the plot is equal to $\ln(A\mathscr{A}^*)$. The slope of the line is given by $-(q\phi_B)/k$. Since q and k are known constants, the slope of the line can be used to extract ϕ_B. The reverse bias saturation current is typically not a constant with bias as the idealized equation indicates. This is because the Schottky barrier height can be a function of bias. Therefore, this measurement can be done at a range of different reverse bias conditions to determine how the Schottky barrier changes with bias.

4.4 Direct Metallization to Germanium

The simplest metallization approach is to deposit a metal contact directly onto the germanium surface. This approach requires the optimization of both the pre-metallization clean, as well as the choice of metal. Initially, the effect of pre-metallization clean was explored. In order to keep all else constant, the metal was chosen to be aluminum which was directly sputtered onto a polished polycrystalline germanium film. The metal was patterned by depositing though a shadow mask, for direct patterning.

The material used was a polycrystalline germanium blanket film. The sample preparation involved the plasma-enhanced CVD (PECVD) deposition of a 300 nm thick SiO_2 film. This is to ensure that the Ge nucleation surface will remain amorphous. Since Ge does not grow on SiO_2, 50 nm of amorphous Si was deposited via PECVD to serve as a nucleation site. Polycrystalline germanium was then grown on this structure in a UHVCVD at 450 °C. The resulting material is a very rough polycrystalline germanium film. This film was then planarized using chemical mechanical polishing (CMP) in order to obtain a flat smooth surface with a thickness of 650 nm. A Hall-Effect measurement was utilized in order to measure the active doping concentration and carrier mobility of the deposited germanium. The film was measured to be p-type with a carrier concentration of $1.1 \times 10^{18}\,\mathrm{cm}^{-3}$ and a mobility of $78\,\mathrm{cm}^2\,\mathrm{V}^{-1}\,\mathrm{s}^{-1}$. The

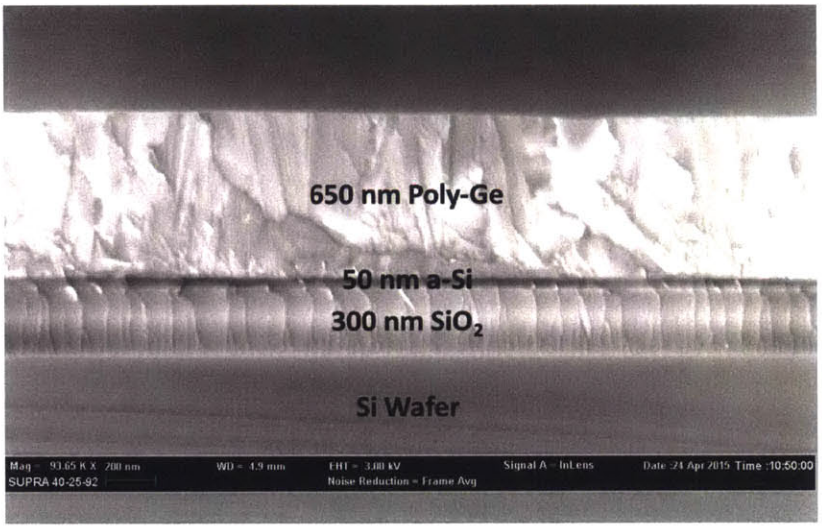


Figure 4-3: Cross section of polycrystalline germanium used for pre-metallization clean tests.

resulting sample before metal deposition is shown in cross-section SEM in Figure 4-3.

4.4.1 Effect of Metal Selection

With aluminum fixed as the contact metal, the pre-metallization cleaning step did not significantly alter the *I-V* performance of the metal contact. Independent of the cleaning approach, the contacts were always Ohmic. Therefore, the effect of metal choice was examined.

Ideally, the Schottky barrier height can be determined by the Schottky-Mott relationship, which enables the barrier height to be calculated from the metal work function and the electron affinity in the semiconductor. It is given by the following:

$$\phi_B = \phi_M - \chi \tag{4.5}$$

where:

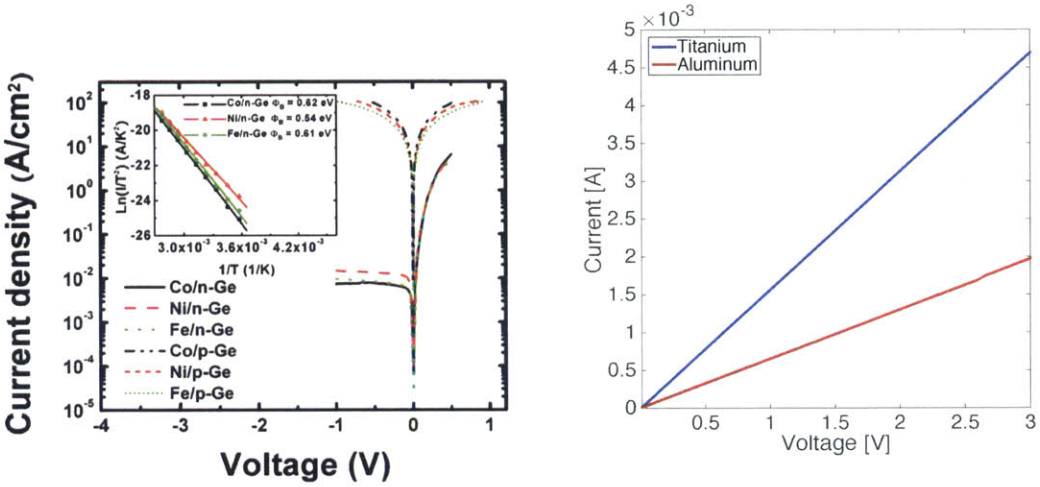
ϕ_B = Schottky Barrier
ϕ_M = Work Function in Metal
χ = Electron Affinity in Semiconductor

While the Schottky-Mott relationship can ideally predict the Schottky barrier height from known material parameters, it is too idealized and is often inaccurate. In actual metal-semiconductor contacts, the interface can become dominated by interface states. The atoms at the surface of the Ge have unsatisfied covalent bonds, called dangling bonds. These dangling bond can form states within the band gap of the material. These states can either accept or donate electrons, depending on the Fermi level. Therefore, these surface states can accumulate charges, and the position of the Fermi level in which the surface becomes electrically neutral is called the charge neutrality level. If the density of these surface or interface states is large enough, the Fermi level will become pinned at the charge neutrality level within the band gap of the semiconductor, which is associated with the defect state energy level. Therefore the Schottky barrier height becomes independent of metal work function, and solely defined by the position of the interface defect states.

In germanium, the charge neutrality level for interface states between the Ge and the metal is located approximately 0.1 eV above the valence band [90, 92, 93]. For direct metallization to Ge, the Fermi-level is almost always pinned at this charge neutrality level. This means that direct metal contacts to n-type Ge always form Schottky barriers with barrier heights of approximately 0.5 eV, while contacts to p-type Ge always form barriers of approximately 0.1 eV, which is effectively an Ohmic contact. This phenomenon is observed experimentally by Zhou et al. in [94].

In Ge, structural defects form acceptor states, and therefore cause the Ge to be p-type, even without the addition of dopants [35, 95]. Structural defects arise from grain boundaries, dislocations, and point defects. In this case, the grain boundaries and the point defects from low temperature epitaxy cause the Ge to always be p-type with a doping level of approximately $10^{18}\,\mathrm{cm}^{-3}$. Therefore, Schottky contacts must be developed onto p-type Ge.

In Figure 4-4a, several different metals are utilized to form direct contacts to n-type and p-type Ge. Independent of the metal selection, all direct contacts to p-type



(a) Direct metallization to both n-type and p-type germanium. The contacts to n-type Ge are always rectifying with Schottky barriers, while the contacts to p-type Ge always have high current and Ohmic behavior From [94].

(b) Ti and Al direct metallization to p-type Ge.

Figure 4-4: Current-voltage measurements from direct metallization to Ge.

Ge are Ohmic and have a very high current density. On the other hand, all contacts to n-type Ge are rectifying and have Schottky barriers greater than 0.5 eV. The specific metals selected in this study are not standard metals available in a CMOS compatible process. Therefore direct metallization was attempted with Al and Ti, which are CMOS compatible metals. These contacts were made to the same p-type Ge as described in Figure 4-3. The metals were deposited via sputtering after removing the native oxide in a HF dip. The resulting I-V measurement is shown in Figure 4-4b. The same results were shown in which any metal directly in contact with p-type Ge yields Ohmic contacts. After experimental results from direct metallization using Al, Co, Fe, Ni, and Ti, with metal work functions ranging from 4.06 eV to 5.01 eV, all of which produce Ohmic contacts, it can be concluded that the idealized equation in Equation (4.5) is not sufficient to determine the Schottky barrier height. Simply changing the metal selection and metal work function for direct metallization is not an appropriate method to fabricate Schottky contacts to p-type Ge. A different

approach must be taken in order to alleviate the Fermi-level pinning, and create Schottky contacts to p-type Ge.

4.4.2 Effect of Pre-Metallization Cleaning

Without any treatment, a germanium surface that is exposed to ambient conditions will form a native oxide. This oxidized surface has been shown to be contaminated by the adventitious adsorption water vapor, hydrocarbons and carbon [96]. This contaminated native oxide arises from an uncontrolled process, and therefore is spatially non-uniform, as well as inconsistent from wafer to wafer. The inconsistencies in native oxide and contaminant composition yield inconsistent and variable device performance results [97]. Therefore, in order to develop a controllable and repeatable process, the surface of the Ge must be cleaned in order to form a pristine interface between the Ge and the metal contact.

In addition to removing the native oxide, a chemical treatment can also alter the electronic properties of the surface. For example, exposing a Ge surface to HF has been shown to passify the dangling bonds of the surface Ge atoms, and significantly reduce the surface recombination velocity [98].

The first step was to test various surface cleans before depositing the metal contact. In each case, the metal contact consisted of 100 nm film of sputtered aluminum. Aluminum was chosen because of its compatibility with standard CMOS processing. It has already been introduced as an interconnection metal, and therefore there is no concern with respect to implementing it into a standard CMOS process. The base pressure in the sputtering tool was approximately 1×10^{-6} Torr, while the metal deposition occurred at 3 mTorr. The contact pattern was defined by direct patterning through a shadow mask with contact circles ranging in diameter from 0.5 mm to 5 mm in diameter. Therefore, both contacts were on the top Ge surface. In order to clean the germanium surface, several different approaches were tried. The native oxide was allowed to remain on the surface, it was removed chemically, it was removed

mechanically, and it was regrown chemically. The specific tests, their purpose and the specific process is listed below:

No Clean – Leave native oxide

1. No wafer treatment before Al deposition

Plasma Etch-Back – Mechanically remove native oxide

1. 30 seconds plasma etch-back at 25 W in sputtering tool

HF – Chemically remove native oxide

1. 30 seconds in 1:10 ($HF:H_2O$)
2. Rinse in DI water
3. Blow dry with N_2 gun

NH_4OH – Chemically remove particles and strip oxide (BAE approach)

1. 120 seconds seconds in 1:1 ($NH_4OH:H_2O$)
2. Rinse in DI water
3. 10 seconds in 1:50 ($HF:H_2O$)
4. Rinse in DI water
5. 120 seconds seconds in 1:1 ($NH_4OH:H_2O$)
6. Rinse in DI water
7. Blow dry with N_2 gun

Ge RCA + HNO_3 – Chemically remove native oxide, then reform oxide

1. 60 seconds in 3:1 ($NH_4OH:H_2O$)
2. Rinse in DI water
3. 15 seconds in 1:6 ($H_2O_2:H_2O$)

4. Rinse in DI water
5. 15 seconds in pure (49%) HF
6. Rinse in DI water
7. 30 seconds in 1:4 ($HCl:H_2O$)
8. Rinse in DI water
9. 15 seconds in pure HNO_3
10. Rinse in DI water
11. Blow dry with N_2 gun

The five different pre-metallization cleans all create a different surface before the metallization step occurred. The "No Clean" process left the native oxide on the surface and directly contacted the native oxide. The "Plasma Etch-Back" process uses argon ion bombardment in the plasma state to mechanically remove the native oxide from the surface of the germanium. This process takes place inside the sputtering chamber, immediately before Al deposition. However, this physical bombardment process may cause structural damage to the germanium surface. The power in this step is kept low in order to minimize the structural damage to the Ge surface. The "HF" process will chemically remove the native oxide. It has also been shown to temporarily passivate the dangling bonds on the surface, as shown by [98]. The "NH_4OH" process utilizes NH_4OH to remove particles and strip organics from the surface. This process is similar to the SC1 step in a standard RCA clean. The following HF step is used to strip the oxide from the surface and expose the bare Ge below. BAE Systems uses a similar NH_4OH chemical clean after a germanium CMP step in their Ge *p-i-n* photodiode fabrication process flow. The "Ge RCA + HNO_3" process utilizes a modified RCA chemical clean to clean the surface of the germanium. A standard RCA clean was shown to be too aggressive for Ge, and fully removed all of the Ge. Therefore this Ge RCA process was developed as an alternative. The NH_4OH

step is for removing organics and rejecting particles, the H_2O_2 oxidizes the Ge surface, the HF strips that oxide, the HCl removes ions, then the HNO_3 chemically forms an oxide on the germanium surface. The chemical formation of an oxide could aid in passivating the dangling bonds on the surface of the Ge, and is a more controllable process than the formation of a native oxide from ambient exposure.

After the samples were cleaned, they were immediately loaded into the sputtering tool and pumped down to vacuum in order to minimize the spontaneous formation of a native oxide. 100 nm of aluminum was sputtered onto the germanium surface. The metal was directly patterned with a shadow mask such that circular contacts were formed on the surface with a diameter of several millimeters. A current-voltage measurement was performed through two adjacent top contacts, and the results are shown in Figure 4-5.

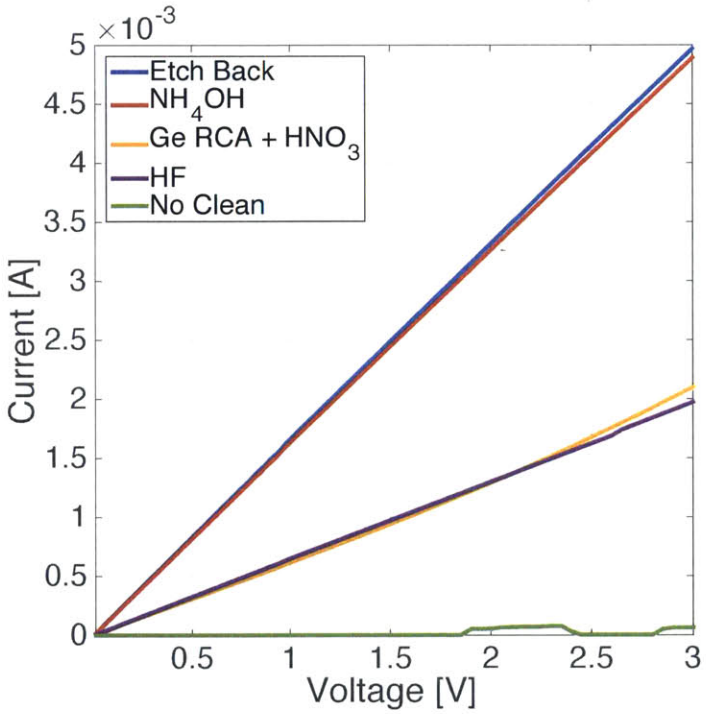


Figure 4-5: Current-Voltage measurement of aluminum contacts to polycrystalline germanium with different pre-metallization cleaning procedures.

From the linear I-V relationship, it is immediately evident that all of the sample preparation techniques yield Ohmic contacts. Each of the different cleaning procedures led to Ohmic contacts and are therefore unsuitable for low dark current MSM photodetectors. The results also indicate that the I-V behavior is not significantly dependent on the cleaning procedure. The only sample that showed significantly different results from the others is the sample that was not cleaned. The sample that was not cleaned shows very low current, but the signal is noisy, irregular, and unstable. Therefore, it is not a suitable candidate for obtaining repeatable results. Altering the pre-metallization preparation alone is not enough to passivate the interface trap states and relieve the Fermi level pinning in order to create Schottky contacts to Ge.

4.5 Contacting Germanium Through an Interlayer

In Section 4.4.1 it was shown that independent of metal selection, direct metallization to p-type Ge results in Fermi-level pinning near the valence band, and therefore yields Ohmic contacts. Even with extensive pre-metallization cleaning procedures, Section 4.4.2 showed that the surface states cannot fully be passivated enough to relieve the Fermi-level pinning and create Schottky contacts. Therefore, a different approach must be made to relieve the Fermi level pinning.

States within the band gap of a semiconductor are caused by a disruption in the perfect crystalline lattice structure. This is why point defects, dislocations, grain boundaries, free surfaces, and interfaces can create defect states within the band gap. In this case, the interface between the Ge and the metal is a disruption in the crystal lattice and forms enough defect states to pin the Fermi level. The defect states have been shown to be metal-induced gap states [93]. In order to reduce the density of metal-induced gap states, different materials can be added between the Ge and the metal. The purpose of these interlayer materials is to separate the metal from direct contact with the Ge, and to passivate as many of the dangling bonds on the Ge

surface as possible. Different materials have been utilized as an interlayer including amorphous Ge [99], silicon-carbon (Si:C) [100], Ge_3N_4 [101], GeO_x [102], sulfur and NiGe [103], and thin Al films allowed to oxidize to form Al_2O_3 [94].

The addition of these interlayers has shown various levels of success. Dark current suppression is observed, but these techniques typically suffer from additional problems. For example, non-standard CMOS materials (Ni and S) are required in [103], the contact relies on unstable oxides (GeO_x) in [102], imprecise processing steps such as spontaneous oxidation in an ambient conditions is implemented in [94], photocurrent is also suppressed reducing device responsivity in [99], non-standard (111) wafer orientations are required in [101], or sometimes even generate their own defect states which generate leakage current from trap-assisted thermal generation [58, 103].

While the addition of a thin interlayer between the Ge and the metal has shown promise in its ability to create Schottky barriers to p-type Ge, many of the proposed techniques have limitations that do not allow for repeatable, reliable integration with a standard CMOS process. Therefore a robust process must be developed in order to obtain the benefits observed from previous studies, while maintaining the standard compatibility with CMOS processing in order to facilitate monolithic electronic-photonic integration.

4.5.1 Amorphous Si and HfO_2 Interlayers

The addition of an interlayer between the metal and the Ge is implemented in order to minimize the metal induced gap states and relieve the Fermi level pinning. In order to reduce the density of interface states between the metal and the Ge, the dangling bonds on the Ge surface must be passivated. An initial approach of using a thin amorphous Si layer as an interlayer was attempted. Amorphous Si was chosen due to its obvious compatibility with standard CMOS processing, the ease of depositing thin layers at low temperatures, as well as its similarities with Ge. The purpose of the amorphous Si is to passivate the dangling bonds on the surface of the Ge.

Then, a thin HfO_2 layer is added to passivate the surface of the Si. HfO_2 was chosen because it is CMOS compatible, since it is used as a high-κ gate dielectric, and can be deposited with an atomic layer deposition (ALD) technique. From a materials perspective, the use of HfO_2 as a standard gate dielectric indicates that it already exists in mass-produced transistors and does not create interface states in Si between the Si and the gate metal. From a processing perspective, the ability to be deposited with ALD means that very thin films can be deposited at low temperatures with excellent uniformity and atomic precision on film thickness.

The material used for this contact was blanket Ge grown epitaxially on Si substrates. The Ge was grown in a UHVCVD reactor to grow a thin buffer layer at 360 °C, then 1.4 µm thick layer at 730 °C. The film was then annealed at ~850 °C in order to reduce the threading dislocation density [104]. The film was not intentionally doped, but structural defects in Ge always result in a p-type material, as discussed in Chapter 2. After growth, the Ge was chemically cleaned before amorphous Si deposition. The clean consisted of 10 min in 1:1 NH_4OH:H_2O, followed by 10 sec in 1:50 HF:H_2O, with the whole process repeated twice. After the clean, 20 nm amorphous Si was deposited using PECVD. The wafer was then immediately loaded into the ALD to deposit 2 nm HfO_2. After the ALD step, the wafer was immediately loaded into a sputtering tool and 200 nm Al was deposited. The specific contacts were designed by photolithography and then the Al was dry etched with end point detection used to stop the etch. Finally, an oxygen plasma was used to remove the resist in an ashing process. The resulting device structure is shown schematically in Figure 4-6.

After fabrication, the Schottky barrier height was measured, as outlined in Section 4.3.1. In order to do this, current-voltage measurements were taken in the dark at a series of temperatures ranging from 30 °C to 160 °C. The results of these measurements are plotted in Figure 4-7. The initial measurements at 30 °C show promising results. The magnitude of the current is very low, at below 1 nA for biases up to 2 V. The low current and approximate linearity on the logarithmic scale indicate that

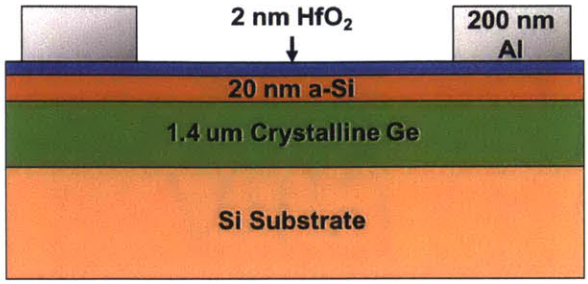


Figure 4-6: Cross-sectional schematic of metal contact to Ge with a HfO_2 interlayer. Ge was grown epitaxially in a UHVCVD, then amorphous Si was deposited via PECVD, then the HfO_2 was deposited with ALD, then the Al was deposited by sputtering. The metal contact was etched into a blanket Al film. (Figure is not drawn to scale.)

the metal contact is rectifying and shows diode-like behavior. However, the leakage current rapidly increases at elevated biases. In addition, the dark current rises rapidly with increasing temperature. This is to be expected, to some extent, since thermionic emission over the Schottky barrier is a thermally activated process. However, it seems that the dark current saturates at slightly elevated temperatures and then no longer increases.

In order to extract the Schottky barrier height from the I-V data, the reverse bias saturation current was extracted and Equation (4.4) plotted in an Arrhenius plot. This extracted data is shown in Figure 4-8. One data point immediately stands out, and that is the data point measured at 30 °C. This data point has significantly lower dark current than the rest of the measurements and does not fit the linear approximation of the rest of the data. This indicates a fundamental shift in the results at temperatures above 30 °C. The rest of the data is fit to a linear approximation in order to determine the slope of the line and extract the Schottky barrier height. The Schottky barrier was measured to be 0.08 eV. Therefore, the contact was a rectifying Schottky contact as fabricated, but rapidly degraded to an Ohmic contact once the temperature was raised above 30 °C. The Schottky barrier height of 0.08 eV is also consistent with the pinned Fermi level results as reported from direct metallization techniques, as

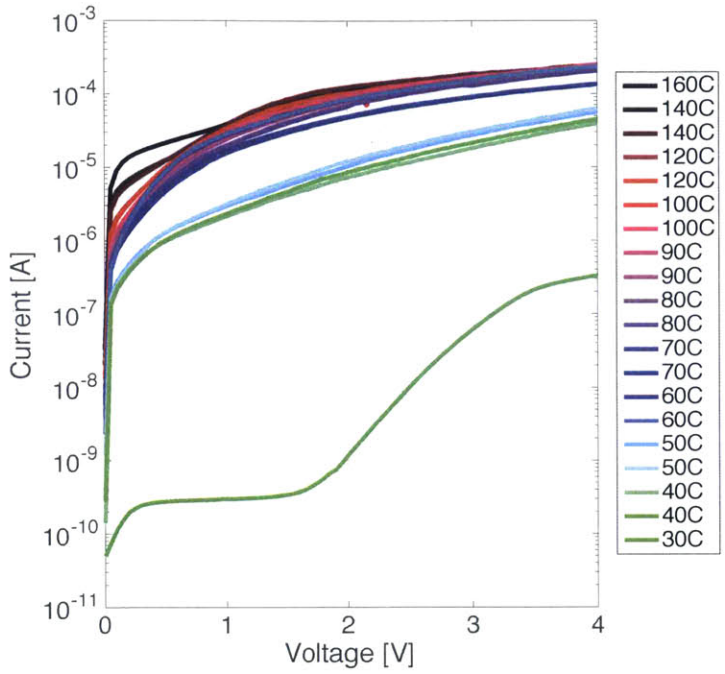


Figure 4-7: Dark *I-V* measurements at a variety of different temperatures ranging from 30 °C to 160 °C. The device structure consists of Al on 2 nm of ALD HfO_2 on 20 nm amorphous Si on 1.4 µm crystalline Ge epitaxially grown on a crystalline Si substrate.

described in Section 4.4. Therefore, the Ge surface states were intitally passivated by these interlayers, which relieved the Fermi-level pinning. However, this passivation was unstable at elevated temperatures.

In order to understand the breakdown of the Al-HfO_2-Si-Ge metallization, the material selection must be revisited. HfO_2 is used as a thin tunneling oxide immediately between the Al and the amorphous Si. In this material the oxygen is bonded to Hf in order to form the HfO_2 barrier. As the temperature of the device is raised, diffusion and intermixing processes become more active. Therefore, the oxygen will only remain bonded to the Hf if this is the most stable state. The Gibbs free energy of formation of HfO_2, SiO_2, and Al_2O_3 is $-1088\,\mathrm{kJ\,mol^{-1}}$, $-856\,\mathrm{kJ\,mol^{-1}}$ and $-1562\,\mathrm{kJ\,mol^{-1}}$ re-

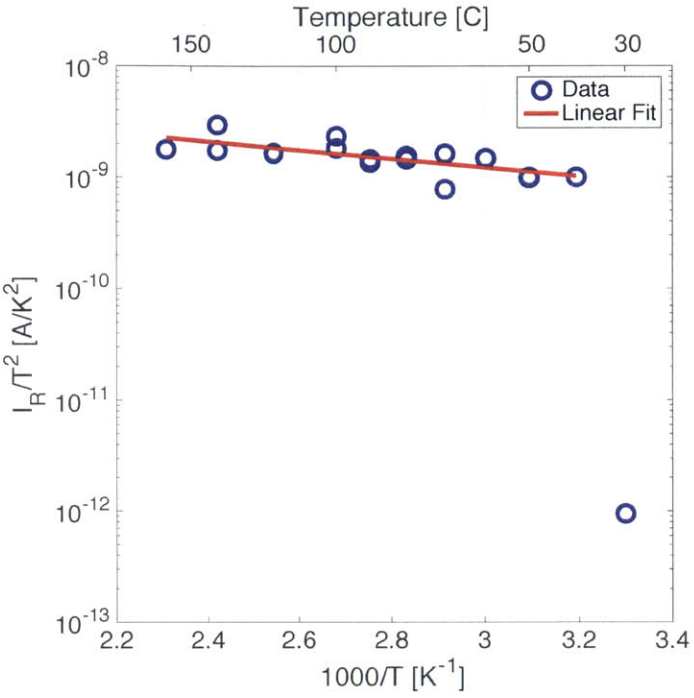


Figure 4-8: Arrhenius plot of the dark I-V measurements taken in Figure 4-7. Fitting for the slope of the line, the Schottky barrier height is calculated to be 0.08 eV.

spectively. Here, it is obvious that the oxygen is most stable when bonded with Al to form Al_2O_3. Since the HfO_2 interlayer is only 2 nm thick, the oxygen does not have to diffuse very far to decompose the HfO_2 layer into a thin Hf metal layer and form an Al_2O_3 layer. Therefore, this process is thermodynamically unstable and slightly elevated temperatures are enough to cause this initially Schottky metallization design to decompose into an Ohmic contact.

Evidence of this decomposition is presented in Figure 4-9. Both lines in this figure represent I-V measurements made on the same device at the same temperature, both at 30 °C. The black line was measured from the device immediately after fabrication. The blue line is the same measurement at the same temperature, however it was performed after the the device temperature was raised to 160 °C in order to extract

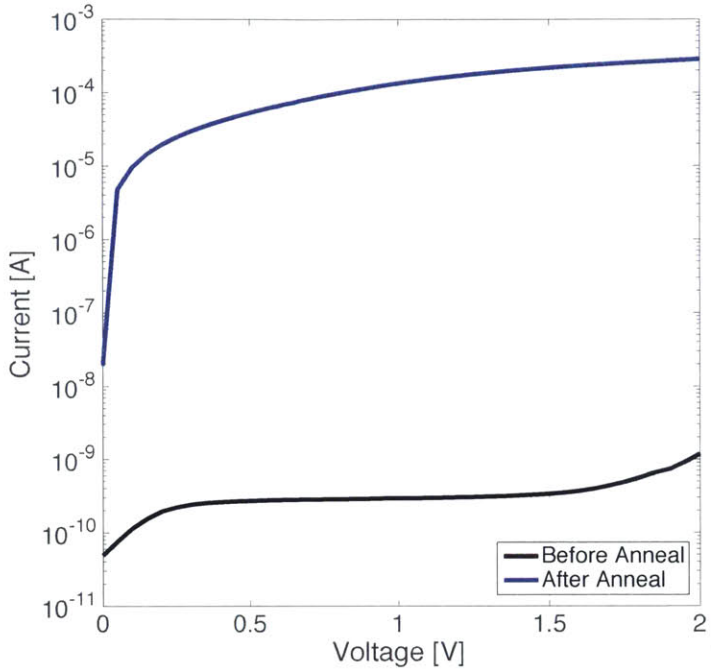


Figure 4-9: Dark I-V before and after annealing. The annealing temperature was raised up to 160 °C. There is a clear degradation of the metal contact, with the dark current increasing by a factor of more than 10^5.

the barrier heights from Figure 4-7. The current in the device after the anneal was five orders of magnitude larger than the device as fabricated. Therefore, the increase in current was from an irreversible decomposition of the device.

4.5.2 Al_2O_3 Interlayers

The use of a thin interlayer between the Ge and the metal contact proves to be an affective method of alleviating Fermi-level pinning and forming Schottky contacts. However, using HfO_2 in direct contact with Al results in a thermodynamically unstable metallization. The HfO_2 was shown to degrade since the oxygen is more stable when bonded to Al. Therefore, the HfO_2 layer was removed and replaced with a Al_2O_3

since Al_2O_3 is a much more stable oxide. In addition, the amorphous silicon layer was removed. Amorphous semiconductors typically suffer from reduced carrier lifetimes, mobilities, diffusion lengths, all of which will reduce the responsivity in a photodetector as well as increase dark current through defect mediated generation. It is advantageous to have a metal contact that does not require any amorphous semiconductor regions.

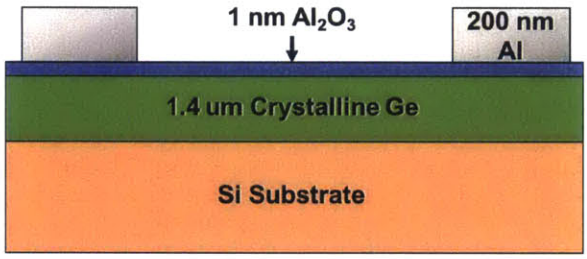


Figure 4-10: Cross-sectional schematic of metal contact to Ge with a Al_2O_3 interlayer. Ge was grown epitaxially in a UHVCVD, then the Al_2O_3 was deposited with ALD, then the Al was sputtered. The metal contact was etched into a blanket Al film. (Figure is not drawn to scale.)

The same epitaxial blanket Ge from Section 4.5.1 was utilized to test an Al_2O_3 interlayer design. However, a different pre-metallization cleaning procedure was implemented. The cleaning process included 5 min in 1:5 H_2SO_4:H_2O, then 2 min in 1:4 H_2O_2:H_2O, then 15 sec in 1:50 HF:H_2O. The purpose of the sulfuric acid step is to clean the organics from the surface. The peroxide chemically oxidizes the Ge surface, then the HF step etches away that oxide leaving a pristine Ge surface. After cleaning, 1 nm of Al_2O_3 was deposited in a plasma-enhanced ALD process at 300 °C. Immediately after ALD, the wafers were loaded into a sputtering tool and 200 nm Al was deposited. The contacts were then defined by photolithography and dry etching the Al with end point detection. Finally, the photoresist was removed with an ashing process. The device was not heat treated after formation. The resulting device structure is shown schematically in Figure 4-10. The Al_2O_3 interlayer is very thin at 1 nm in order to allow carriers to effectively tunnel through the dielectric. If the interlayer is thin enough, then carriers can tunnel through it without restricting current flow,

while still physically separating the Al from the Ge, and eliminating the Fermi-level pinning from metal induced gap states.

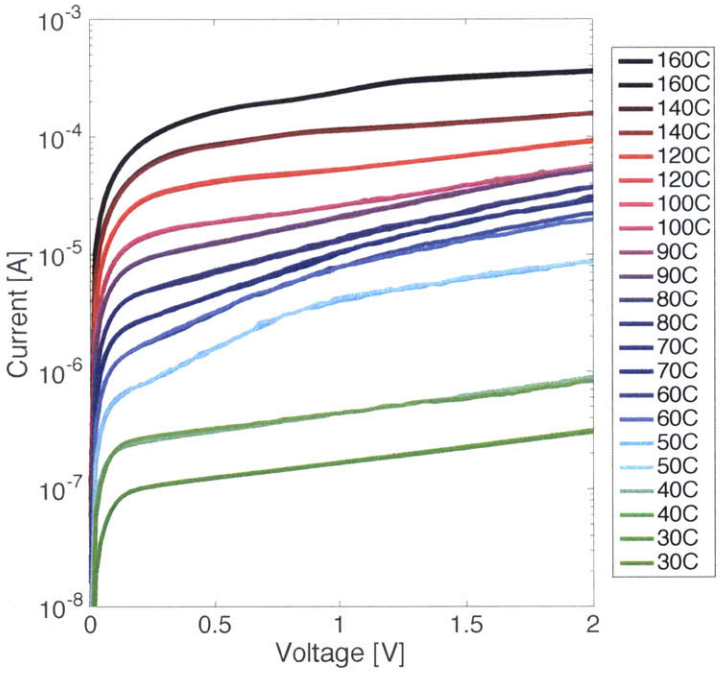


Figure 4-11: Dark I-V measurements at a variety of different temperatures ranging from 30 °C to 160 °C. The device structure consists of Al on 1 nm of ALD Al_2O_3 on 1.4 µm crystalline Ge epitaxially grown on a crystalline Si substrate.

Current-voltage measurements were taken in the dark, and shown in Figure 4-11. The measurements taken at 30 °C show a dark current below 200 nA at biases up to 2 V. In addition, the relationship is linear when plotted on the logarithmic scale, indicating that these devices follow the I-V relationship indicated in Equation (4.1) and are characteristic of Schottky diodes. The reverse bias leakage current is measured at a series of temperatures from 30 °C to 160 °C. The current increases as the temperature increases, as expected from Equation (4.3).

When the dark current is extracted from the temperature dependent I-V data, it can be plotted on an Arrhenius plot, as indicated in Figure 4-12. With a linear fit to

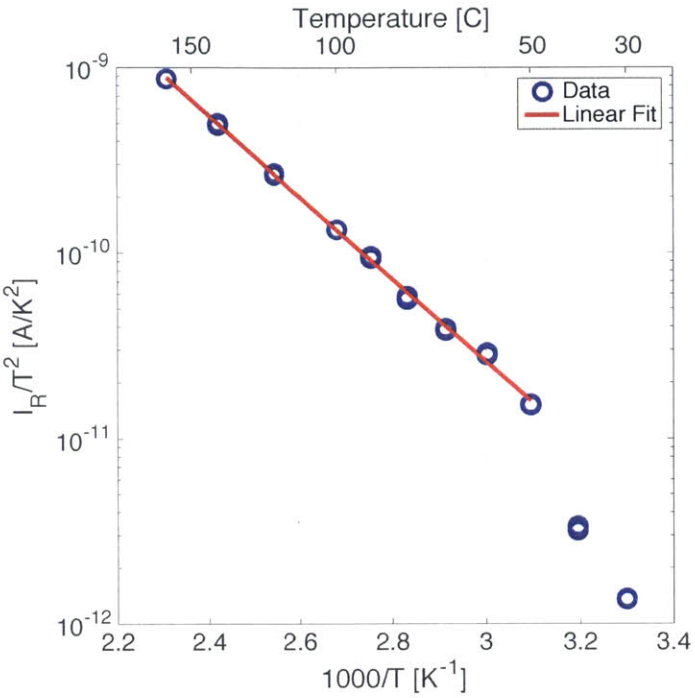


Figure 4-12: Arrhenius plot of the dark I-V measurements taken in Figure 4-11 at a bias of 0.5 V. Fitting for the slope of the line, the Schottky barrier height is calculated to be 0.44 eV.

the reverse bias current, the Schottky barrier height can be extracted. However, the reverse bias current does not saturate to a fixed value, but increases with increasing bias. Therefore extracting a reverse bias saturation current is dependent on the bias condition. For this specific example, the reverse bias of 0.5 V is considered. The linear fit to the reverse bias current yields a Schottky barrier height of 0.44 eV.

While the Figure 4-12 utilizes a reverse bias of 0.5 V to calculate the Schottky Barrier height, this can be performed at each bias. Figure 4-13 plots the calculated Schottky Barrier height as a function of bias. The Schottky barrier is maximized at 0.46 eV at a small reverse bias of 0.25 V and decreases with increasing bias. The reduction in barrier height at low bias is likely an artifact since the Schottky diode is not expected to have reached a saturation current at very low biases. The reduction

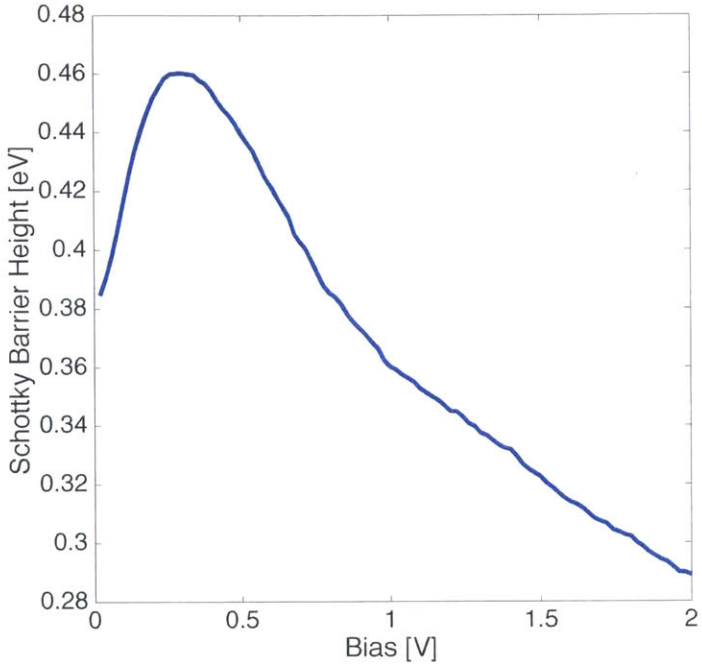


Figure 4-13: Plot of the Schottky barrier height as a function of bias. A maximum Schottky barrier of 0.46 eV is observed at a bias of 0.25 V and decreases as the bias increases.

of barrier height with increasing bias is caused by image-force forces, and is known as Schottky-barrier lowering, or the Schottky effect [105]. It has been documented in other Schottky barriers to Ge [39]. Schottky barrier lowering can be theoretically calculated from:

$$\Delta\phi_{\mathrm{B}} = \sqrt{\frac{q\mathscr{E}_{\mathrm{m}}}{4\pi\varepsilon_{\mathrm{s}}}} \tag{4.6}$$

where:

$\Delta\phi_{\mathrm{B}}$ = Change in Schottky Barrier Height
q = Elementary Charge
$\mathscr{E}_{\mathrm{m}}$ = Maximum Electric Field at Surface of Semiconductor
ε_{s} = Permittivity of Semiconductor

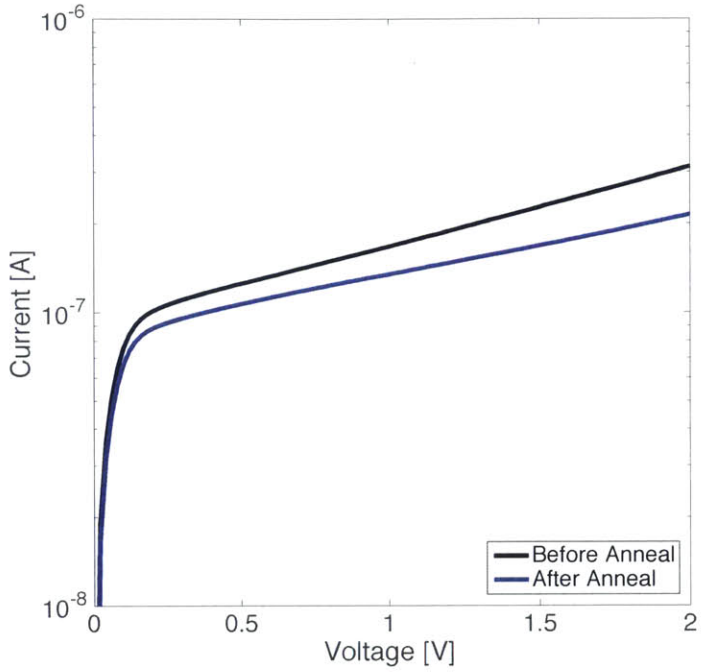


Figure 4-14: Dark I-V before and after annealing. The annealing temperature was raised up to 160 °C. The metal contact clearly remains rectifying without a significant difference in dark I-V characteristics before and after annealing.

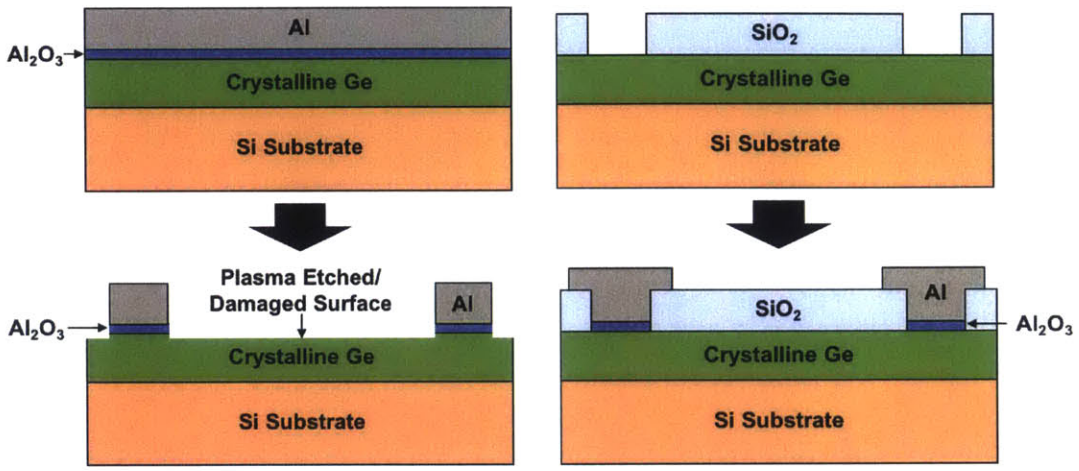
The Schottky barrier height was measured by measuring I-V at a series of temperatures ranging from room temperature to 160 °C. Therefore, the sample was effectively annealed at 160 °C. This caused an irreversible breakdown of the device implementing a HfO_2 interlayer. However, when the device with an Al_2O_3 interlayer was measured before and after heat treatment, the dark current remained constant. Figure 4-14 plots the current-voltage relationship measured at 30 °C, before and after heat treatment up to 160 °C. The metal contact remains rectifying after exposure to elevated temperatures without a significant change in dark current. This verifies the thermal stability of this contact design, as 160 °C is higher temperature than the devices are expected to experience while integrated into a microprocessor.

4.6 Improving Device Performance with Process Design

The metal contact design which utilizes a thin Al_2O_3 prove to alleviate Fermi level pinning and effectively suppress dark current. The dark current is dominated by thermionic emission over the Schottky barrier. Therefore, in this device, it requires thermal emission over a barrier of 0.46 eV at low bias. An additional source of dark current results trap-assisted thermal generation from defect states within the band gap. If this generation occurs within the space charge region of the Schottky diode, the charges will be separated and this will contribute to the dark current.

Trap states within the band gap arise from disruptions of the crystallinity of a semiconductor. Therefore, surfaces and structural defects can cause defect states, which can lead to increase Shockley-Read-Hall recombination, which would reduce the responsivity of a photodetector, or trap assisted thermal generation, which increases the dark current of a photodetector, as discussed in Chapter 3. While defects in the semiconductor can arise from the growth process or from significant strain in the material, they can also be introduced from processing.

The process for producing Schottky barriers to Ge includes a plasma etch step to etch the Al and define the metal contacts. This etch step ends with an endpoint detection. Therefore, at the end of the Al plasma etch, the Al_2O_3 is exposed to the etching plasma. While the etch chemistry is selective to Al, it is not perfectly elective. With the Al_2O_3 layer being only 1 nm thick, it is likely that it was etched away entirely where it was exposed to the plasma. Therefore, it is likely that the Ge surface was exposed to the etching plasma. The plasma contains ionized particles which are accelerated towards the wafer surface in order to yield an anisotropic etch. These ionized particles can cause structural damage on the Ge surface, as indicated in Figure 4-15a. This plasma-induced surface damage introduces trap states along the Ge surface, thereby reducing device performance.



(a) Process flow used to fabricate metal contacts as measured.

(b) Improved process flow to reduce surface damage on Ge from metal etch.

Figure 4-15: Current metal contact process flow compared to a proposed improved process flow.

An improved process is indicated in Figure 4-15b. Before metallization, a protective SiO_2 film is deposited. Then contact vias are etched in the SiO_2 using HF, which is gentle on the Ge surface. Then the device can be fabricated as discussed in Section 4.5.2. When the metal is etched, the end-point will end on the protective SiO_2 and the Ge will remain buried and protected. This improved metallization process can reduce the creation of trap states near the Ge surface, thereby further decreasing dark current and increasing photocurrent. The addition of a SiO_2 passivating layer on the germanium surface has been shown to reduce dark current of Ge MSM photodetectors by two orders of magnitude [106].

4.7 Summary

In this chapter Schottky contacts to p-type Ge were developed. Structural defects in undoped Ge create p-type Ge. Literature review has shown that directly contacting p-type Ge always yields Ohmic contacts. The high concentration of surface states at the interface between the Ge and the metal pins the Fermi level at the charge neutral

level, which is approximately 0.1 eV above the conduction band edge. The Fermi level is pinned at this point independent of metal work function.

Different pre-metallization cleaning procedures were tested in order to passivate these surface states and alleviate the Fermi level penning. A range of different cleaning procedures all resulted in the same final condition with the Fermi level still pinned resulting in an Ohmic contact.

Thin interlayers were added to separate the Ge from direct contact with the metal. This approach showed promise in literature, but most previous approaches suffered from a range of problems including lack of CMOS compatibility, requirement of non-standard wafers, or photocurrent suppression. Initial attempts of using a 20 nm amorphous Si layer in addition to a 2 nm HfO_2 layer proved effective in creating Schottky barriers with dark current suppression. However, they were unstable and the HfO_2 decomposes at slightly elevated temperatures. This resulted in the contact changing irreversibly into an Ohmic contact. This design proved to be thermodynamically unstable with the oxygen preferentially bonding to the Al to form Al_2O_3, since it has a lower Gibbs free energy of formation.

An improved metallization was developed which consists of a thin 1 nm Al_2O_3 interlayer between the Ge and the Al contact. The Al_2O_3 was kept thin enough to efficiently allow tunneling through the layer, however it was thick enough to physically separate the Al from the Ge surface. Therefore, the Fermi-level pinning was alleviated and Schottky barriers were observed. A barrier height of up to 4.6 eV was measured. The barrier height as a function of bias was determined. The metallization approach was proven to remain stable at temperatures up to at least 160 °C, which verifies that they will not degrade with the elevated temperatures present in integrated circuits.

Finally, an improved device fabrication process was proposed. The improved fabrication process involves burying the Ge under a protective SiO_2 layer, and contacting through chemically etched vias. This eliminates the exposure of the Ge to harsh plasma etch processes, therefore eliminating the process induced defects in the Ge.

Chapter 5

Ge MSM Photodetectors

5.1 Introduction

In Chapter 2, high quality germanium was grown on amorphous substrates while adhering to back-end-of-line processing constraints. In Chapter 4, Schottky contacts were developed to p-type Ge in order to enable MSM photodetectors with low dark currents. In this chapter, these individual components are all combined in order to fabricate and test germanium MSM photodetectors.

5.2 Quantifying Device Performance

There are three key factors that determine the performance of a photodetector, including dark current, responsivity, and bandwidth. The first two metrics can be determined with steady state measurements, while the bandwidth of the detector is determined from its frequency response.

The dark current determines the magnitude of current that passes through the device while there is no light incident upon the detector. This factor effectively determines the noise level of the detector, as the photocurrent will have to be measured above this dark current level. Therefore it plays a significant role in the signal to

noise ratio (SNR). In addition, the dark current plays a role in the power consumption for the device. Power consumption can be determined from the simple relationship $P = IV$ where P is the power consumed by the device, I is the current flowing through the device and V is the applied bias. Therefore, the dark current should be minimized for a given bias. This is why Schottky contacts were implemented for these MSM photodetectors, as discussed in detail in Chapter 4. The Schottky contacts reduce the dark current, thereby increasing the SNR and decreasing the power consumption of the detector.

The responsivity of the detector is a metric at how efficient it is at converting incident photons into current. It is reported in units of amps per watt, where amps refer to the output photocurrent, and watt refers to the incident optical power. This term should be maximized in order to produce the largest response possible per unit of incident optical power. A large responsivity enables the SNR to be maximized and allows the detector to operate at low optical powers. This saves power for the entire system since it allows the light source to operate at lower powers. Both the dark current and the responsivity can be measured under steady state conditions, and therefore will be the focus of this chapter.

The bandwidth is a measure of the detectors frequency response. It is also called the $-3\,\mathrm{dB}$ cutoff frequency. This is the frequency at which the detector photocurrent output is reduced by a factor of $3\,\mathrm{dB}$ from it steady state output. This is typically considered the maximum frequency at which the detector can be operated. The bandwidth of the detectors was not explicitly measured in this thesis. Theoretically, the bandwidth of the device is either limited by RC delay or by the carrier transit time. RC delay is dependent on the device design, and especially on the contact design. The RC limited bandwidth is the limit how how fast the capacitance within the detector can be charged and discharged, and can be calculated by:

$$f_{\mathrm{RC}} = \frac{1}{2\pi \left(R_{\mathrm{L}} + R_{\mathrm{s}}\right) C} \tag{5.1}$$

where:

f_{RC} = RC Limited Bandwidth
R_L = Load Resistance (50 Ω)
R_s = Series Resistance
C = Detector Capacitance

The carrier transit time limited bandwidth is limited by the time that it takes for a photogenerated carrier to reach a contact and be collected. This term is dependent on the carrier velocity within the semiconductor, which is a function of the electric field within the semiconductor. This internal electric field can be altered by the applied bias of the detector. However, under the assumption that the carriers are traveling at their saturation velocity, the transit time limited bandwidth can be calculated from [105]:

$$f_{tr} = \frac{0.44}{\sqrt{2}} \left(\frac{v_s}{s} \right) \tag{5.2}$$

where:

f_{tr} = Transit Time Limited Bandwidth
v_s = Carrier Saturation Velocity
s = Separation Between Contacts

The final −3 dB cutoff frequency can be estimated by combining the RC limited bandwidth and the carrier transit time limited bandwidth by the following:

$$f_{3dB} = \sqrt{\frac{1}{1/f_{RC}^2 + 1/f_{tr}^2}} \tag{5.3}$$

Therefore, in order to maximize the bandwidth of the detector, the capacitance should be minimized and the carrier transit time should be maximized. In order to minimize the noise and the power consumption of the device, the dark current should be minimized. This can be performed by maximizing the Schottky barrier height in the metal contact, as discussed in Chapter 4. Finally, the responsivity of the device

should be maximized, which is achieved by maximizing the measured photocurrent per watt of incident light. Maximizing the responsivity of the detector is the focus of this chapter.

5.2.1 Measuring Responsivity

The ultimate goal of a photodetector is to convert an optical signal into an electrical signal that can be measured by an external circuit. The metric that is used to quantify this conversion is called responsivity and is defined by the ratio of measured photocurrent per unit incident optical power:

$$\mathscr{R} = \frac{I_{\text{meas}}}{P_{\text{opt}}} \tag{5.4}$$

where:

$\mathscr{R}$ = Responsivity
I_{meas} = Measured Photocurrent
P_{opt} = Optical Power

In order to accurately determine the responsivity of an actual photodetector, both the measured photocurrent and the optical power must be quantified. The photocurrent is measured directly by connecting the device to an external circuit and using a semiconductor parameter analyzer. However, determining the incident optical power is more involved.

The devices fabricated here were not waveguide integrated. Therefore, the light was coupled into the device from the top surface. A fiber coupled laser was used in order to illuminate a spot on the wafer surface which included the photodetector. A schematic of this normal illumination scheme is shown in Figure 5-1.

In order to quantify the optical power incident on the detector, all loss mechanisms must be considered. The total optical power is based on the average intensity of the light on the wafer surface. This is then scaled by the actual area of the detector, since

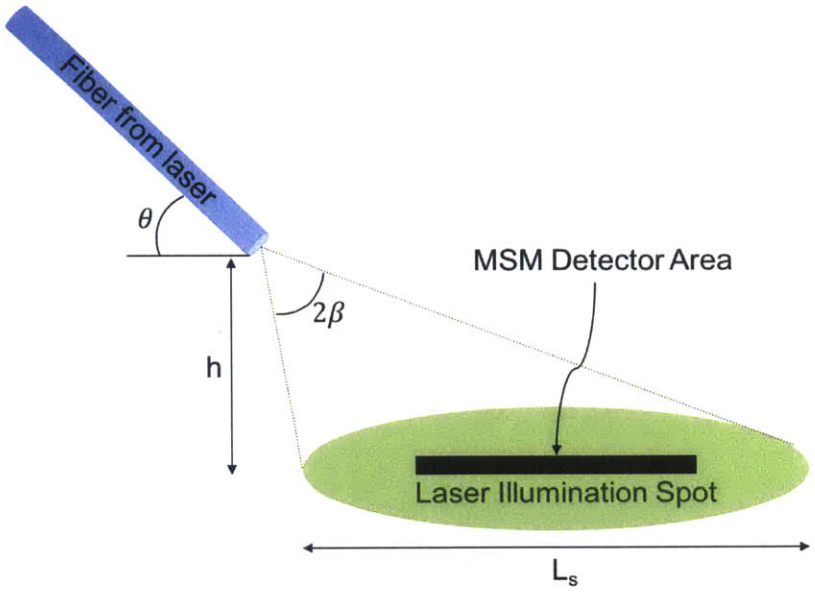


Figure 5-1: Schematic of the approach used to measure the responsivity of Ge photodetectors. The detectors were illuminated from the top-down using a fiber coupled laser.

the illumination spot is larger than the detector areas. Then all of the optical loss mechanisms are accounted for. The optical power is adjusted for the fraction of light lost to shadowing from the metal contacts, the fraction of light lost from reflection off the Ge surface, and adjusted for the amount of light absorbed in the material since the Ge layer was too thin to absorb all of the light in the normal incidence configuration. The total optical power is calculated by:

$$P_{\text{opt}} = I_{\text{laser}} A_{\text{det}} (1 - f_{\text{shadow}})(1 - f_{\text{ref}}) f_{\text{abs}} \tag{5.5}$$

where:

P_{opt} = Optical Power Incident Upon Detector
I_{laser} = Average Optical Intensity From Laser
A_{det} = Detector Area
f_{shadow} = Fraction of Detector Area that is Shadowed
f_{ref} = Fraction of Light that is Reflected from Detector Surface
f_{abs} = Fraction of Light that is Absorbed

First, the initial optical laser power was quantified using an optical power meter. The laser power was directly measured for a range of laser driver input currents in order to directly measure P_{laser}. Then the average optical intensity was scaled by the area of the elliptical illumination spot on the wafer surface, as indicated by:

$$I_{\text{laser}} = \frac{P_{\text{laser}}}{\frac{1}{4}\pi L_{\text{s}} W_{\text{s}}} \tag{5.6}$$

where:

I_{laser} = Average Optical Intensity From Laser
P_{laser} = Laser Optical Power
L_{s} = Laser Spot Length
W_{s} = Laser Spot Width

Calculating the laser spot length and width is simply a geometry exercise. The divergence angle of the light from the end of the fiber is determined by the numerical aperture of the fiber. Then, the length and width of the spot can be calculated by the geometry of the measurement setup and is calculated explicitly by:

$$L_{\text{s}} = \frac{d_{\text{core}}}{\sin\theta} + h\left[\tan(90-\theta+\beta) - \tan(90-\theta-\beta)\right] \tag{5.7}$$

$$W_{\text{s}} = d_{\text{core}} + \frac{2h\tan\beta}{\sin\theta} \tag{5.8}$$

where:

L_{s} = Laser Spot Length
W_{s} = Laser Spot Width
d_{core} = Fiber Core Diameter
h = Height of Fiber Above Detector
θ = Angle Between Fiber and Wafer Surface
β = Divergence Angle of Light From Fiber = arcsin(NA)
NA = Numerical Aperture of Fiber

Once the average optical intensity is determined, then the additional losses must

be considered. The metal contacts on the top of the detector shadow the active area below. Therefore the fraction of the detector that is shadowed by the metal contacts is calculated by:

$$f_{\text{shadow}} = \frac{W_{\text{finger}}}{p} \tag{5.9}$$

where:

f_{shadow} = Fraction of Detector Area that is Shadowed
W_{finger} = Width of Contact Finger
p = Metal Contact Pitch

Germanium has a very high refractive index, and therefore coupling light directly from air into Ge results in large reflection losses from the surface. Therefore, to fully account for the optical power of light that is absorbed in the Ge, the reflected light must be taken into account. The fraction of light reflected from the Ge surface is calculated by:

$$f_{\text{ref}} = \left(\frac{n_{\text{Ge}} - n_{\text{air}}}{n_{\text{Ge}} + n_{\text{air}}}\right)^2 \tag{5.10}$$

where:

f_{ref} = Fraction of Light Reflected off Surface
n_{Ge} = Refractive Index of Germanium
n_{air} = Refractive Index of Air

When the final Ge photodetector is integrated into a system, the light will be absorbed down the length of the device, ensuring that all of the optical power is absorbed. However, these test devices have light illuminated from the surface and therefore the path length of light is limited by the thickness if the Ge layer, and therefore not all of the light is absorbed. In order to have a fair comparison of the expected responsivity of a waveguide coupled device, the fraction of light absorbed

in the Ge must be taken into account. That fraction is simply calculated by the Beer-Lambert law:

$$f_{\text{abs}} = 1 - \exp(-\alpha L_{\text{p}}) \tag{5.11}$$

where:

f_{abs} = Fraction of Light Absorbed in Germanium
α = Optical Absorption Coefficient of Germanium
L_{p} = Optical Path Length in Germanium

5.2.2 Gain

The fundamental photocurrent can be defined based on the assumption that a single photon creates a single electron hole pair with a given collection efficiency, and can be defined as follows:

$$I_{\text{photo}} = q\left(\eta\frac{P_{\text{opt}}}{h\nu}\right) \tag{5.12}$$

where:

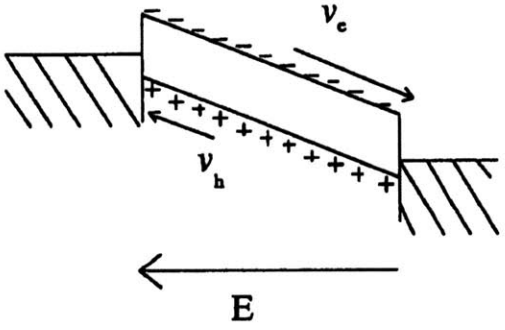
I_{photo} = Directly Generated Photocurrent
q = Elementary Charge
η = Collection Efficiency
h = Plank's Constant
ν = Photon Frequency

The photocurrent that is directly generated from the absorption of light can also be magnified by the presence of gain. As the light is absorbed in the semiconductor, electrons and holes are generated, as indicated in Figure 5-2a. If the device is being biased, then an electric field is present within the semiconductor, and this will cause the charges to be separated towards opposite contacts, as shown in Figure 5-2b. Some carriers may be directly collected by the metal contacts, while some carriers may become trapped in the semiconductor at or near the interface of the metal contact.

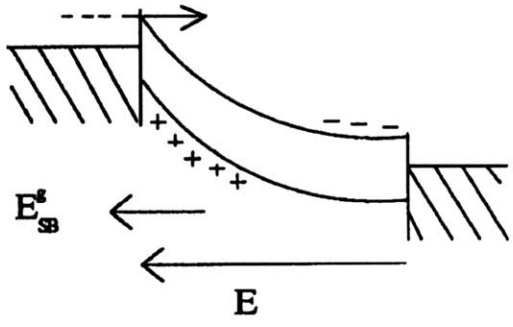
The mechanism for gain in an MSM is often attributed to two different effects. One mechanism is photoconductive gain, and the other is attributed to enhanced carrier conduction through the Schottky barrier in the presence of trapped carriers. The photoconductive gain mechanism assumes that the conductivity of the semiconductor will be enhanced for the duration of time that a photogenerated carrier exists (the carrier lifetime). When a single carrier is collected by the metal contact, an additional carrier is injected at the opposite contact in order to maintain charge neutrality. If the the transit time is lower than the lifetime, then multiple carriers can travel from one contact to the other. This can continue to occur for the duration of time that the semiconductor conductivity remains high, equivalent to the carrier lifetime. This mechanism is observed in photoconductors with ohmic contacts [107], but not in MSM detectors with Schottky contacts. This is because the the conductivity of the semiconductor is what limits current flow in a photoconductor, since the ohmic contacts do not block current. However, in an MSM with Schottky contacts, the reverse biased Schottky is the component with the highest resistance in the device, and therefor the Schottky barrier limits the carrier conduction in the detector. Therefore, photoconductivity is not the source of gain in these devices.

The other gain mechanism is based on enhanced carrier conduction through Schottky contacts due to photogenerated image forces, as demonstrated in [108, 109]. This mechanism assumes that carriers collect at the semiconductor surfaces. This can either be due to carriers getting trapped in surface trap states, or piling up at a thin insulating interlayer between the semiconductor and the metal contact. The accumulation of charges results in image charges in the metal and the generation of an additional electric field across the interface of the metal contact. As reported in Section 4.5.2, the addition of an electric field can cause Schottky barrier lowering, and therefore increase the current flow across the contact by enhanced thermionic emission over the barrier, as indicated in Figure 5-2d. In addition, if holes are trapped at a thin enough insulating layer, they can promote excess electron tunneling across the contact

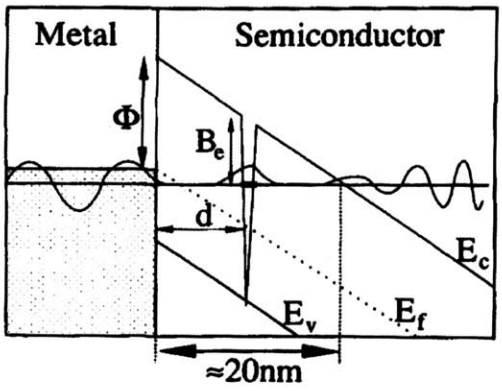
into the semiconductor, as shown schematically in Figure 5-2c. This mechanism relies on the presence of Schottky barriers for the metal contacts and a way to trap carriers at the semiconductor surface.



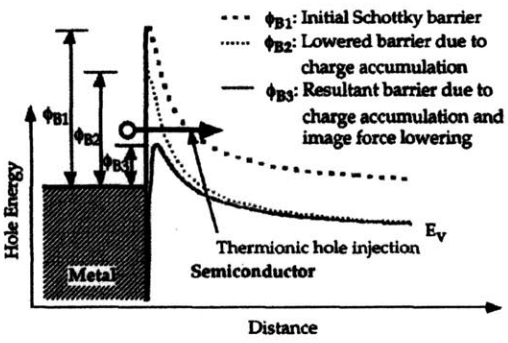
(a) Electron-hole pair generation from photon absorption. From [109].



(b) Charge separation from internal electric field externally applied bias. From [109].



(c) Charges can get trapped at interface states and promote excess tunneling. From [110].



(d) Excess charge at contact can create en electric field a lower the Schottky barrier. From [108].

Figure 5-2: Gain mechanism. Electron hole pairs are generated from photon absorption. The external electric field separates carriers. Some carriers can get stuck in traps and promote excess tunneling through the barrier. The pile-up of charges at the contact create image forces which generates an electric field which lowers the Schottky barrier. The reduced barrier allows excess thermionic emission current.

Independent of the gain mechanism, it can be quantified in a similar way. The photogenerated carriers get trapped for a certain amount of time τ. During this time, an extra carrier will be injected into the semiconductor, either by tunneling or

thermionic emission, and it will transit the distance from one contact to the other. If the original carrier is still trapped, then another carrier can be injected and transit from one contact to the other. This can continue to happen for the duration of time that the photogenerated carrier exists in the excited state. Therefore, the gain can be quantified by te ratio of the carrier lifetime and the transit time and is given by the following expression [111]:

$$G = \frac{I_{\text{meas}}}{I_{\text{photo}}} = \frac{\tau}{t_{\text{tr}}} \tag{5.13}$$

where:

G = Photoconductive Gain
I_{photo} = Directly Generated Photocurrent
I_{photo} = Measured Photocurrent
τ = Carrier Lifetime
t_{tr} = Carrier Transit Time

The carrier lifetime is a material property and can be affected by dislocations in the material, surface passivation, and the presence of recombination centers. However, the transit time is dependent on device design, applied bias, as well as material properties. The transit time can be expressed by the following expression:

$$t_{\text{tr}} = \frac{s}{v} \tag{5.14}$$

where:

s = Separation Between Metal Contacts in Photodetector
v = Carrier Velocity

The distance between contacts is a device design parameter, but the carrier velocity is a function of both the carrier mobility, which is a material property, and the electric field, which is a design parameter. The carrier velocity can be approximated by:

$$v = \mu\mathscr{E} \approx \mu\frac{V}{s} \tag{5.15}$$

where:

μ = Carrier Mobility
$\mathscr{E}$ = Electric Field
V = Applied Bias

If Equations (5.13) to (5.15) are combined, then the photoconductive gain can be expressed by the following:

$$G = \frac{\mu \tau V}{s^2} \tag{5.16}$$

Combining everything, the detector responsivity has the following expression:

$$\mathscr{R} = \eta \left(\frac{q}{h\nu} \right) \left(\frac{\mu \tau V}{s^2} \right) \tag{5.17}$$

The first term represents the carrier collection efficiency, the second term is purely dependent on the energy of the incident photon, and the third term represents the gain within the detector. The responsivity of the detector should increase as the gain increases, and therefore linearly increase with applied bias, as well as be a strong function of the contact separation.

5.3 Device Structure

The design of the metallization contact pattern plays a large role in determining final device performance. The smaller the separation between metal contacts, the shorter the transit time. This increases the grain factor, as indicated in Equation (5.13). It also increases transit time limited bandwidth, as indicated in Equation (5.2). However, as the spacing between metal contacts is reduced, the capacitance per unit length of the detector is increased. Therefore the RC delay for the device increases and the total bandwidth becomes limited. Therefore, a standard metallization strip running down each side of the waveguide trench has a trade-off in the spacing between contacts.

In order to de-couple the device capacitance from the metal contact spacing is to implement an interdigitated contact design. Large metal lines are used to ensure low series resistance for the device. However, these large metal lines have high capacitance, so they are kept 5 µm from the Ge trench, and therefore the anode and cathode lines are separated by 10 µm in order to keep capacitance low. The direct contact to the Ge is achieved with narrow interdigitated contacts. The contact fingers width was 1 µm, the smallest feature size that the available i-line stepper is able to reliable resolve. The contact pitch was varied from 1.5 µm to 3 µm, meaning that the spacing between contacts ranged from 0.5 µm to 2 µm. An image of the contact design is seen in Figure 5-3.

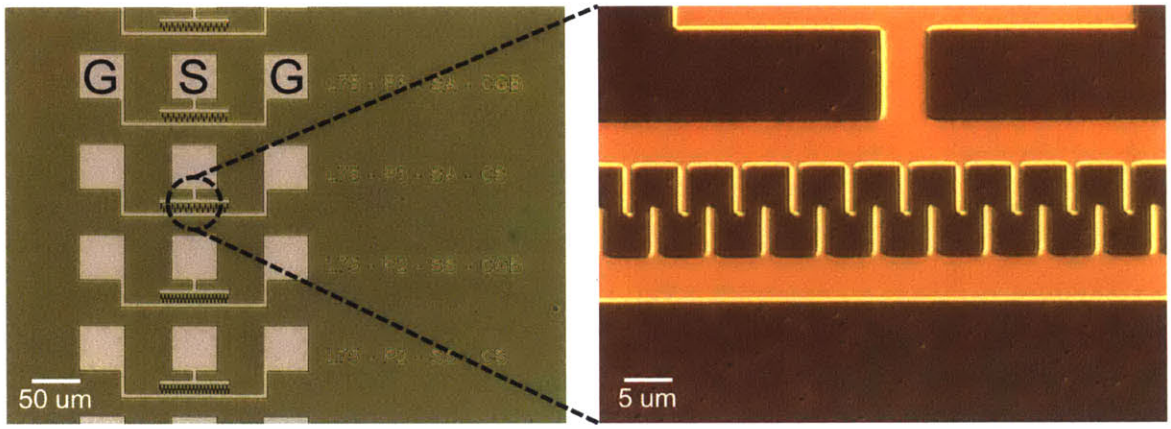


Figure 5-3: Plan view of the metallization device structure used for MSM photodetectors. The probe pads are 50 µm by 50 µm with a pitch of 100 µm. They have a ground-signal-ground (GSG) setup for high-speed measurements. The individual contact fingers are interdigitated with a pitch ranging from 1.5 µm to 3 µm.

In order to make the contact design suitable for high-speed measurements, a standard ground-signal-ground (GSG) probe pad design was implemented. The probe pads were 50 µm squares with a pitch of 100 µm. This probe pad design is compatible with standard RF probes in order to measure the bandwidth of the detectors.

5.4 MSM Photodetectors on Blanket Ge

In Chapter 4, the metal contact design was optimized with the intent of maximizing the Schottky barrier height. Maximizing the Schottky barrier height suppressed leakage current in the dark, ensuring a low power devices, and enabling the possibility of having high SNR photodetectors. However, the low leakage Schottky contacts are useless unless photocurrent is capable of passing through the contacts without also being suppressed. Therefore, the photoresponse must be tested.

The device structure tested consisted of a 1 nm Al_2O_3 interlayer between a blanket epitaxial Ge film and a sputtered aluminum metal contact. The fabrication process and device structure is the same one discussed in detail in Section 4.5.2. The same contact metallization pattern is used as shown in Figure 5-3 with interdigitated contacts.

When testing the photoresponse, a fiber coupled laser with a wavelength of 980 nm was used to illuminate the devices from the surface, as outlined specifically in Section 5.2.1. A 980 nm laser was used in order to ensure significant optical absorption within the thin Ge film in addition to practical constraints, such as the availability of a high power fiber coupled laser.

The *I-V* response of the detector was first measured in the dark, and then again under illumination. The illumination intensity was increased by increasing the drive current to the laser. In Figure 5-4, both the dark and light *I-V* lines are plotted. The immediately obvious characteristic of this plot is the significant difference in current with the presence of light as compared to the dark measurement. Therefore, the detector is working as a photodetector. This also indicates that while the Schottky barriers are effective at suppressing dark current, photocurrent is not suppressed.

At any specific bias voltage, as the magnitude of the optical intensity increases, the magnitude of the device current also increases. This can be observed more explicitly in Figure 5-5. In order to generate this figure, the total optical power incident upon the detector was calculated from the laser drive current by the method outlined in

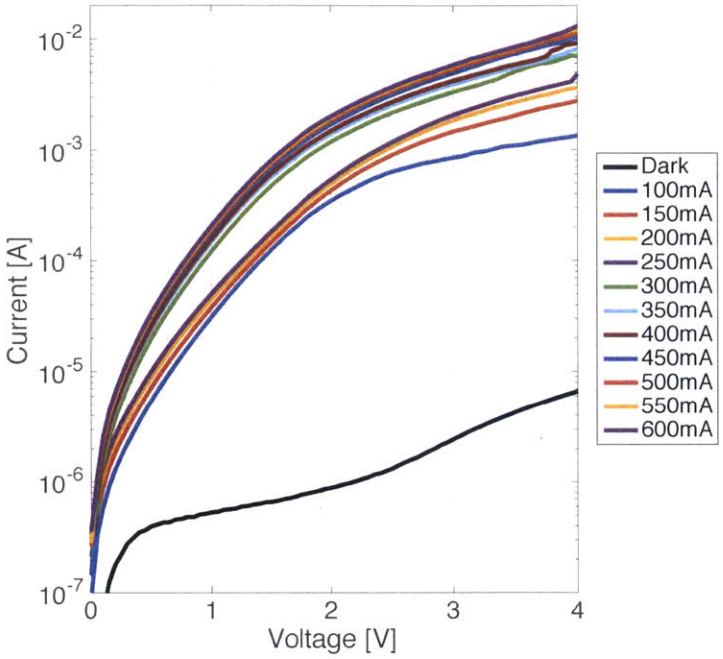


Figure 5-4: Light and dark I-V measurements in the dark and with various laser powers. Illumination is at 980 nm and the legend denotes the current used to drive the laser. The significant increase in current is due to the generation of a photocurrent, and therefore the MSM structure is acting as an effective photodetector.

Section 5.2.1. As a given bias voltage is kept constant, the measured photocurrent increases with increasing optical power. The measured photocurrent was shown to increase linearly with optical power. The slope of the linear relationship between photocurrent and optical power is the responsivity of the detector. Therefore, the data was fit to a linear model and the slope of the linear fit represents the responsivity of the detector at that given bias. Several different biases are plotted in Figure 5-5, from 1 V to 4 V. The slope of the line increases with increasing bias, indicating that the responsivity of the detector also increases with increasing bias. When the responsivity is plotted as a function of bias, then Figure 5-6 can be extracted.

Figure 5-6 shows the responsivity of the blanket MSM photodetectors as a function

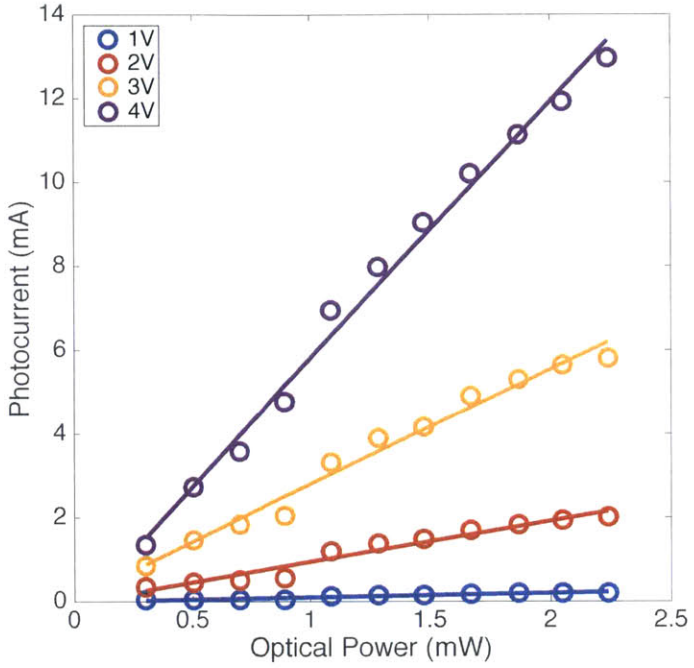
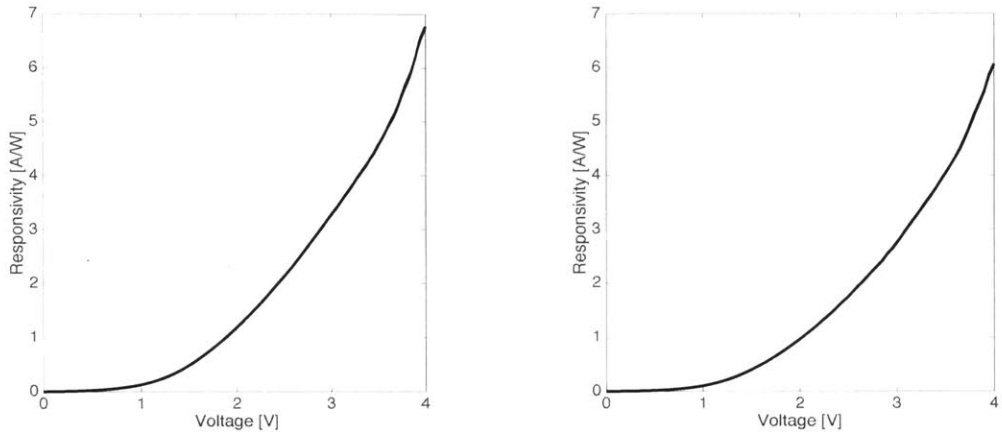


Figure 5-5: Measured photoresponse from at 980 nm laser source. The photoresponse is plotted for different detector biases. The slope of the linear fit of the photocurrent vs. optical power plot gives the detector responsivity at that bias. This particular detector has a contact pitch of 3 µm and a spacing of 2 µm.

of bias. The plot in Figure 5-6a shows the responsivity of a detector with a 1 µm spacing between contacts, while Figure 5-6b shows the responsivity of a detector with a 2 µm spacing between contacts. The magnitude of the responsivity is very high, at 6 A W^{-1} to 7 A W^{-1}. Assuming that each incident photon generates a single electron-hole pair, and each carrier is collected with 100 % efficiency, then the maximum responsivity is 0.79 A W^{-1}. Since the measures responsivity is much higher than this, there must be gain in the detector. The Schottky barriers which suppress the dark current are clearly not suppressing the photocurrent, thereby selectively reducing dark current to enhance the SNR of the detector.

While the responsivity curves indicate that the MSM device structure operates as



(a) Responsivity of a blanket Ge photodetector with a contact separation of 1 µm.

(b) Responsivity of a blanket Ge photodetector with a contact separation of 2 µm.

Figure 5-6: Responsivity of Ge MSM photodetectors on blanket epitaxially grown Ge films. Notice that the responsivity is not linear as expected, and does not scale with contact spacing. However the measured responsivity is high enough to indicate the presence of gain.

an effective photodetector, it also raises additional questions. The responsivity is not linear with bias as expected and it is not a strong function of contact separation as expected. This is because the active area of the detector is not clear for these blanket devices. In calculating the incident optical power on these devices, it was assumed that the active area was limited to the 1 µm wide region where the interdigitated fingers overlap. This assumption was made since this region will have the highest electric field within the Ge, and therefore be the most efficient at collection photogenerated carriers. The surrounding regions with low electric field would not have carriers efficiently swept out by a drift process since the electric field is low, instead they would rely on a diffusion process to diffuse into the high field regions before they are collected. However, the lack of dependence on contact separation and the non-linear responsivity plot indicate that this assumption may not be appropriate.

The photodetectors on blanket Ge have shown that the Schottky barriers developed

for dark current suppression do not limit the collection of photocurrent. The contacts selectively suppress dark current and not photocurrent. They also show that the responsivity of the detectors is much higher than possible from collecting a single electron-hole pair per incident photon, and therefore the detector must exhibit gain.

5.5 MSM Photodetectors on Selectively Grown Ge

While the photodetectors made on blanket Ge verify the high performance capabilities of the MSM device structure, accurate responsivities could not be determined. In order to accurately quantify the responsivity of these detectors, the detector area must be clearly defined. Therefore, the device was modified to implement Ge which was selectively grown in SiO_2 trenches.

In order to fabricate the devices, the wafer was first thermally oxidized to form a 500 nm thick SiO_2 film. Then 1 µm wide trenches were lithographically defined and etched into the SiO_2, exposing the crystalline Si below. Ge was selectively grown in the exposed Si regions in the trenches, and not on the SiO_2. During the growth process, the Ge was thermally cycled between 650 °C to 850 °C in order to minimize the dislocation density and achieve the highest material quality possible, as outlined in [16, 104]. After growth, the Ge had overgrown the trench sidewalls and formed angled facets, as seen in [112, 113] . In order to remove the facets and clearly define the active detector volume, the Ge was planarized in a CMP process, then cleaned. The metal contacts were then deposited exactly as they were for the blanket devices in Section 5.4 and in the development of the Schottky contacts as outlined in Section 4.5.2. The detailed fabrication process flow can be found in Appendix A. In these devices, the majority of the surface is SiO_2 and only a small 1 µm wide trench contains Ge. Therefore, the detector area is well known since it is lithographically defined. There is no charge transfer from the surrounding SiO_2 since the 980 nm light is not absorbed there. A plan view SEM image of device is shown in Figure 5-7.

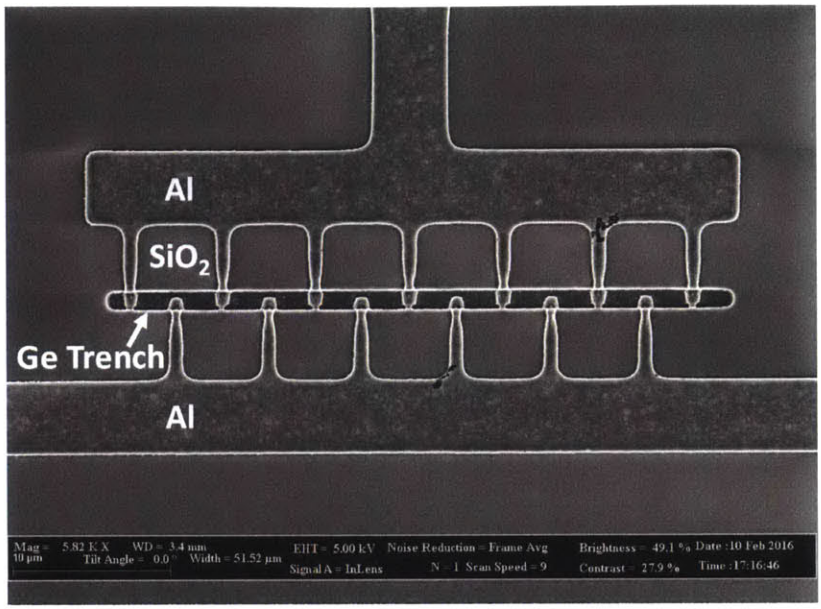


Figure 5-7: Representative device structure for MSM made on selectively grown crystalline Ge.

These devices are based on standard epitaxial Ge material and thermal cycling was used in order to obtain the highest crystalline quality possible. Due to the requirement of high temperature annealing and the utilization of the crystalline Si as an epitaxial seed, these devices are not compatible with back end of line integration. However, they are fully compatible with front end of line CMOS processing and standard integration techniques.

These devices are not waveguide-integrated, as they would need to be in order to interface with an external system. They are illuminated from the surface in order to determine their photoresponse. However, efficiently coupling light from waveguides into Ge photodetectors is a well studied process and has been demonstrated in many other Ge photodetectors. These coupling techniques are either based on butt coupling [43, 114, 115], evanescent coupling [16, 39, 40, 42, 116], or both [15, 20]. Since coupling light from a waveguide to a Ge photodetector is such a well studied topic, it was assumed to be a well understood process and not considered critical for the development of these photodetectors. In addition, single mode waveguides typically

require submicron lithography requirements with smooth sidewalls, which is beyond the capabilities of the i-line stepper available for lithography.

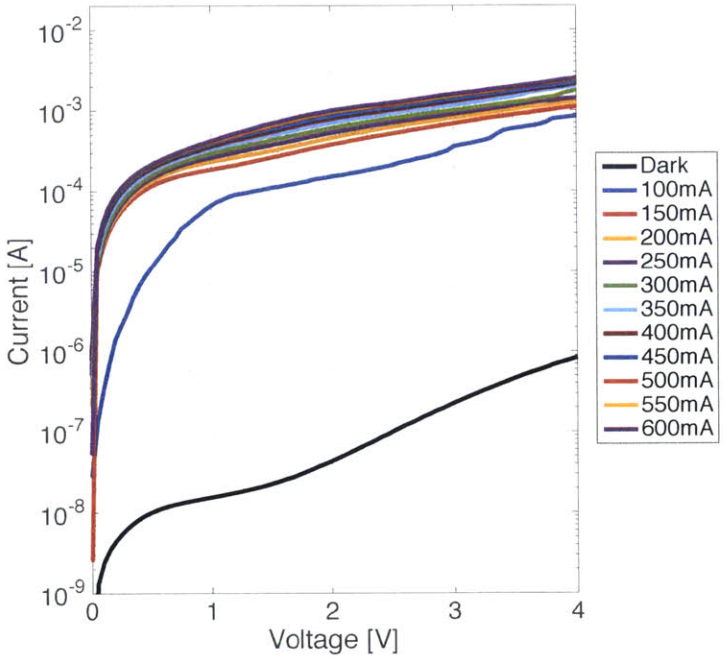


Figure 5-8: Light and dark I-V measurements for a 75 µm long detector with a contact separation of 2 µm. Illumination is at 980 nm and the legend denotes the current used to drive the laser. The significant increase in current is due to the generation of a photocurrent, and therefore the MSM structure is acting as an effective photodetector.

A representative photoresponse for the selectively grown crystalline Ge photodetectors is shown in the light and dark I-V measurement in Figure 5-8. Once again, it is obvious that the current increases dramatically with the presence of light and therefore these devices exhibit a clear photoresponse and are acting as photodetectors.

These devices exhibit very low leakage current in the dark with total dark current remaining below 1 µA for a bias up to 4 V. A leakage current of 1 µA is considered to be the upper limit of what is allowable for integration with high speed amplification circuits [117]. This is the threshold where the transimpedance amplifier (TIA) noise

becomes the main source of noise in the receiver. This specific device has a length of 75 µm and a contact pitch of 3 µm (contact separation of 2 µm). The leakage current for the detector scales linearly with device length, therefore a shorter device will have an even lower leakage current. The length of the device is determined by the optical absorption length in the detector, which is also dependent on the coupling approach. With butt-coupling, complete absorption can occur within a 10 µm long device [115]. Therefore, the total leakage current of this device can be reduced by a factor of 7.5 if this butt coupling approach is implemented.

Table 5.1: Steady-state performance summary for MSM detectors on selectively grown crystalline Ge.

Contact Separation	**Dark Current Density at 1 V**	**Maximum IQE at 4 V**
2 µm	2.07×10^{-2} A cm^{-2}	89 %
1 µm	3.21×10^{-2} A cm^{-2}	190 %
0.5 µm	5.37×10^{-2} A cm^{-2}	405 %

In order to standardize the results to be independent of coupling design, the dark current density is normalized to the area of the detector. This current density is summarized in Table 5.1. The leakage current scales with contact separation. For the same detector bias, the internal electric fields will be higher when the contacts are moved closer together. The increased electric fields induce Schottky barrier lowering, as elucidated in Figure 4-13 and Equation (4.6). Therefore, the closer the contact separation, the greater the leakage current for a given detector bias.

The responsivity of these detectors as a function of bias was determined by the same technique show in Figure 5-5. The responsivity is a strong function of contact separation, as shown in Figure 5-9. The responsivity increases as the contact separation decreases since the carrier transit time decreases as the contacts move closer together. The reduced carrier transit time is caused by the increased electric field

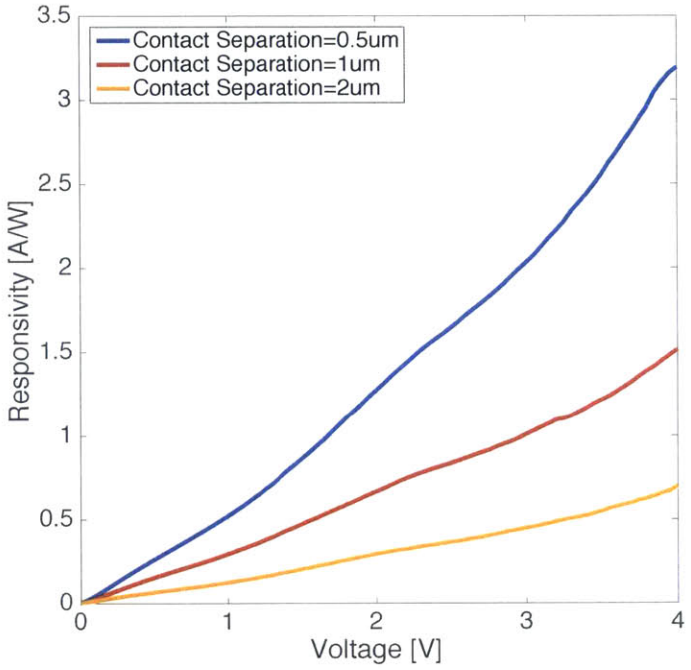


Figure 5-9: Responsivity of MSM photodetectors on selectively grown Ge with different contact separations. The responsivity is linearly increasing with bias, and scales inversely with contact separation. The magnitude of the responsivity confirms the presence of gain.

in the Ge for a given bias, as well as the shorter distance required for the photo-generated carriers to travel before they care collected by the metal contacts. The responsivity curve is also linear with bias, as predicted by the increasing gain term in Equation (5.17).

The magnitude of the responsivity is significantly greater than the $0.79\,\mathrm{A\,W^{-1}}$ limit with 100 % collection efficiency and no gain. Therefore, these detectors must exhibit gain. Assuming 100 % collection efficiency, the minimum gain in the device with a contact spacing of 0.5 µm is a factor of 4.05 at a bias of 4 V. Therefore the internal quantum efficiency (IQE) in the detectors at 4 V is 89 %, 190 % and 405 % for detectors with a contact spacing of 2 µm, 1 µm and 0.5 µm, respectively. A trend

is seen here where the responsivity approximately doubles as the contact separation is halved.

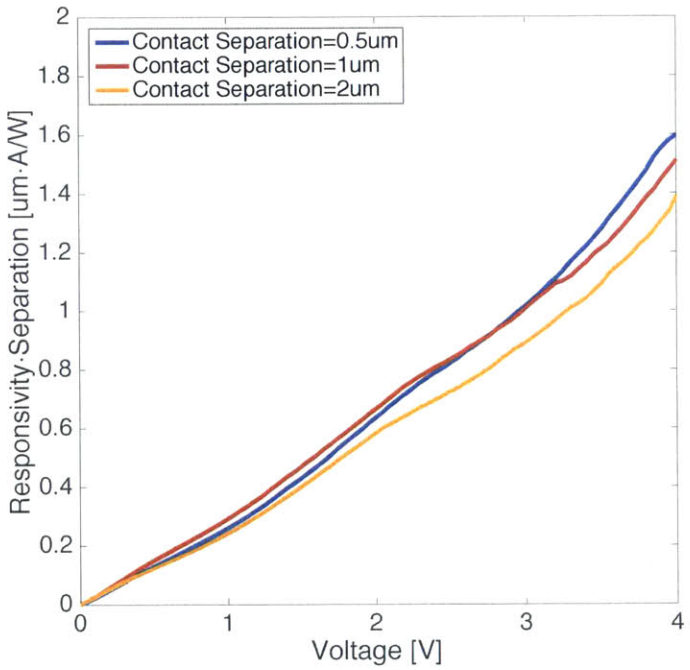


Figure 5-10: MSM responsivity multiplied by the contact separation. The responsivities for the three different devices all collapse onto the same line, indicating that the responsivity scales with $1/s$.

In order to elucidate this trend, the responsivity for each device is scaled by multiplying the measured responsivity with the contact separation. This results in Figure 5-10. With this scaling, it is evident that the responsivity for the three different detector lines all collapse onto a single linear relationship that scales with bias. Therefore, $\mathscr{R} \cdot s = R_0 V$ where R_0 is a constant and is equal to $0.375\,\mu\mathrm{m\,A\,V^{-1}\,W^{-1}}$, assuming that the contact spacing is measured in microns. This value is independent of contact spacing, and represents the slope of the line in Figure 5-10. With this unified relationship, it becomes possible to determine the responsivity of a detector with different contact spacing. For example, if the contact spacing was reduced from

500 nm, as fabricated here, to 100 nm, which would be easily possible in a modern fab with modern lithography equipment, the responsivity would be increased by a factor of 5. Therefore the expected responsivity at 4 V would be 16 A W^{-1} with a gain multiplication factor of approximately 20. This would allow the detector to operate at lower biases while still achieving gain in the detector. For example, a detector gain multiplication factor of >3 could be achieved at a low bias of 1 V if the contact spacing was reduced to 100 nm.

While this relationship is useful for projecting device performance for different contact spacings, it does not align with the predicted responsivity relationship in Equation (5.17). The responsivity was expected to scale with bias proportional to $1/s^2$, however it was shown to actually scale with $1/s$. This discrepancy is based on the breakdown of the fundamental assumptions used to calculate the responsivity relationship. In Equation (5.15), it was assumed that the electric field could be linearly approximated by $\mathscr{E} = V/s$. However, the true electric field in the Ge is not a simple constant. Figure 5-11 plots the electric field distribution in a Ge MSM photodetector under bias [118]. It is apparent that the electric field is not a constant within the Ge, but varies significantly with position. Therefore, the carrier velocity is not a constant with position, and the assumptions made in estimating the carrier transit time were invalid.

In this specific device, the contact spacing is 300 nm and the applied bias is 2.8 V. With the simple approximation that $\mathscr{E} \approx V/s$ the assumed electric field would be 93 kV cm^{-1}. However, the actual electric field in the Ge shows large areas where the electric field is 40 kV cm^{-1} to 60 kV cm^{-1}. Therefore the simple linear approximation drastically underestimates the magnitude of the electric field in the Ge and the model breaks down. The dependence on contact separation was shown to scale with $1/s$ and not $1/s^2$.

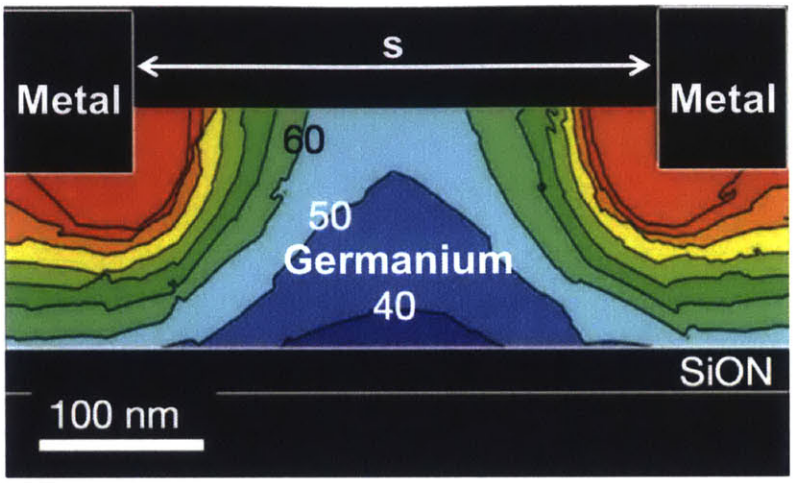


Figure 5-11: Simulated electric field distribution for a Ge MSM device structure similar to the one described here. The lines indicate iso-electric fields lines with units of $\mathrm{kV\,cm^{-1}}$. It is clear that the electric field is not a constant. From [118].

5.5.1 Discussion of Gain in Germanium Photodetectors

This MSM device is the first germanium MSM photodetector to demonstrate gain. Gain in MSM detectors have been demonstrated in other material systems, especially III-V semiconductors [109, 110, 119–123], however this is the first MSM device to demonstrate gain in Ge.

Previously reported Ge MSM photodetectors do not exhibit gain because they typically suffer from non-rectifying (or weakly rectifying) ohmic contacts, the introduction of defect states that quickly cause recombination at the contacts, or have too thick of an interlayer to allow image forces to sufficiently reduce the Schottky barrier height or promote electron tunneling across the barrier. The MSM detectors here have high quality Ge which results in long carrier lifetimes. They implement Schottky contacts with very high Schottky barriers (0.46 eV). In addition, the presence of a thin 1 nm Al_2O_3 interlayer allows the holes to pile up at the interface and promote tunneling across the barrier. Therefore, the MSM design presented here is idealized in order to maximize gain.

Other device structures can be used to observe gain in a Ge photodetector. One

such device is an avalanche photodiode (APD). While these can demonstrate responsivities $>15\,\mathrm{A\,W^{-1}}$, they need to be biased at greater than 20 V in order to achieve such high responsivities [124], or the applied bias has to be greater than 15 V in order to observe any multiplication [125], which is impractical for low voltage modern integrated circuits.

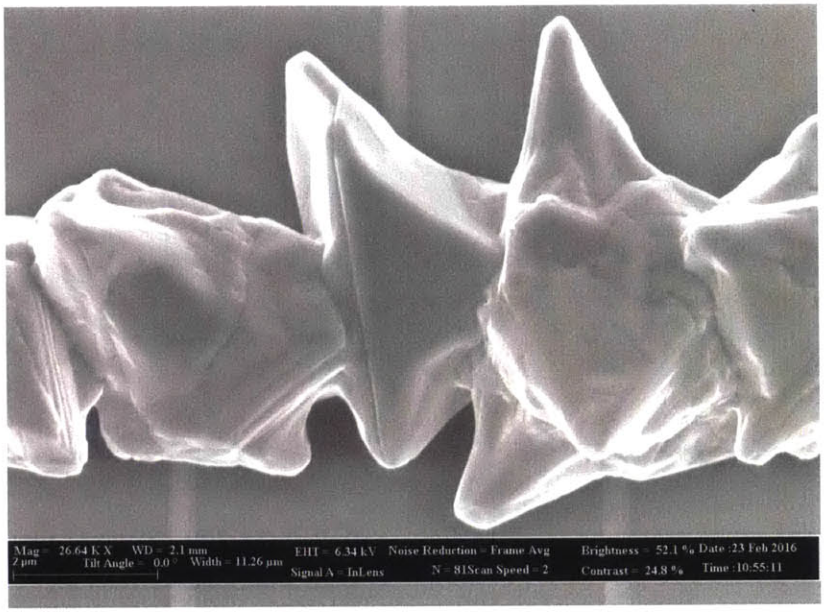
The MSM photodetectors presented here combine the benefits of possessing high responsivities due to the presence of gain, while operating a low biases. They also exhibit low dark current due to strongly rectifying Schottky contacts, all while maintaining a fully CMOS compatible material selection and fabrication process.

5.6 MSM Photodetectors on Amorphous Substrates

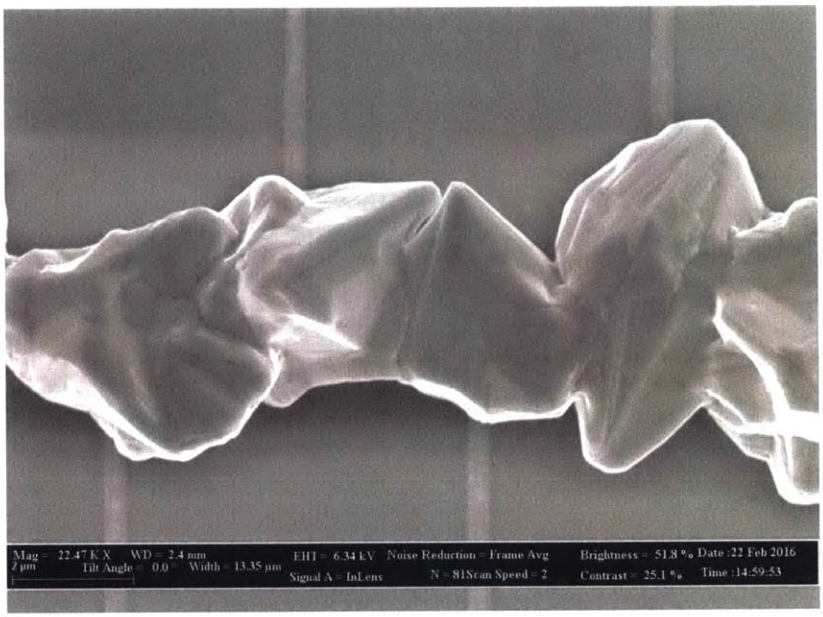
In Section 5.5, state of the art Ge MSM photodetectors were developed on epitaxially grown Ge. With the device structure proven to yield high performance results, the final step is to implement this device on Ge grown on amorphous substrates by the 2D GCLG technique, as outlined in Chapter 2.

5.6.1 Device Fabrication

In order to fabricate these devices Ge was grown on an amorphous SiO_2 pseudo-substrate, with the two dimensional geometrically confined growth technique that is detailed in Chapter 2. This growth technique is used to grow large-grain Ge on amorphous substrates, while adhering to low-temperature processing constraints (below 450 °C). The grains are then coalesced to form a continuous material within a lithographically defined 1 µm wide trench. These coalesced grains have a rough surface morphology with significant overgrowth over the Ge trench. Long range faceting was observed, indicating large grains. During the coalescence process, the Ge significantly overgrows the shallow 300 nm deep trenches, resulting in a very rough surface morphology, as seen in Figure 5-12.



(a) SEM image of a trench filled with coalesced Ge grains on SiO_2 utilizing the 2D GCLG technique. The image was taken immediately after Ge growth using a staggered seed structure.



(b) Additional SEM image of a trench filled with coalesced Ge grains on SiO_2 utilizing the 2D GCLG technique.

Figure 5-12: Images of Ge MSM on amorphous substrates immediately after growth. The Ge grains have coalesced to fill a trench, but have a very rough surface morphology and significant overgrowth over the trench.

After the trench has been filled with Ge, the next step involves metallization. One significant benefit to the geometrically confined growth technique is that all grains locations are lithographically defined by the placement of the confinement channel and nucleation seed. Therefore, the location of the grain boundaries is known. The metal contacts can then be designed such that they are located on the crystalline Ge or on the grain boundaries. The metal contacts apply the electric field in the Ge, and therefore the electron hole pairs are generated between the contacts and drift in separate directions towards the metal contacts where they are collected. If the metal contacts are placed on the grain boundaries, then the carriers are generated in the crystalline material and never have to cross a grain boundary before they are collected. Therefore, from the perspective of the carriers, the device is single-crystalline, despite the presence of grain boundaries. This is illustrated schematically in Figure 5-13.

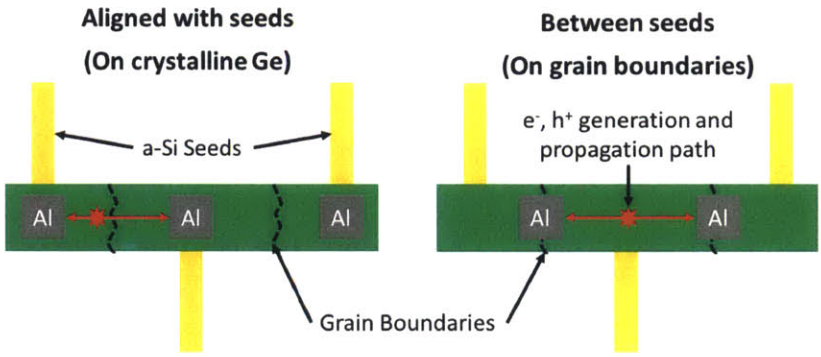


Figure 5-13: Since the seeds are lithographically defined, the grain boundary location is known. Metal contacts can either be placed on the crystalline Ge (left) or on the grain boundary (right). With contacts placed on the grain boundary, the photogenerated electron-hole pair can be collected without ever crossing a grain boundary.

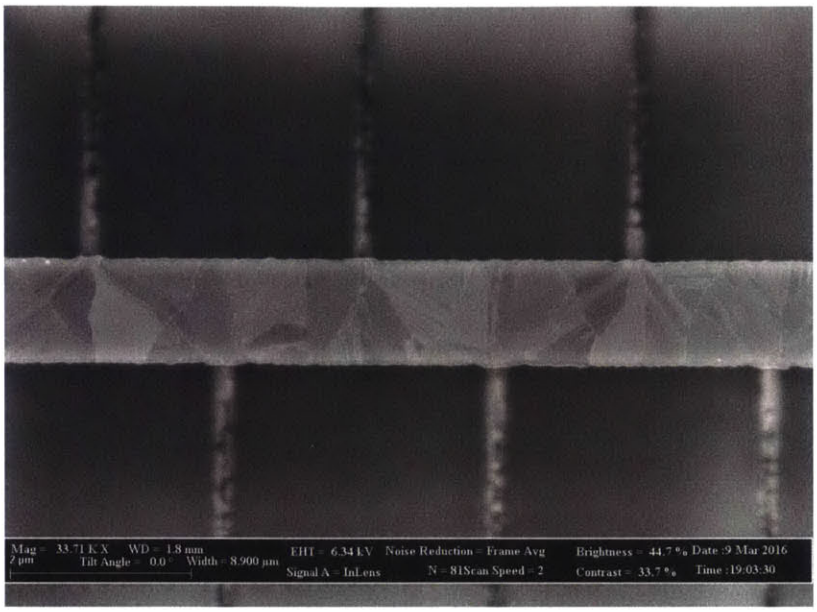
The Ge grains overgrow the oxide trench in the lateral dimension as well as the vertical dimension. Therefore they need to be planarized in order to create a planar surface for the metallization process. They also need to be planarized in order to strictly define the active area of these devices. The devices were planarized using a CMP process that was developed specifically for Ge selectively grown in waveguides [126]. Immediately after the CMP step, the trenches are well filled with

coalesced Ge and planar, as seen in Figure 5-14a.

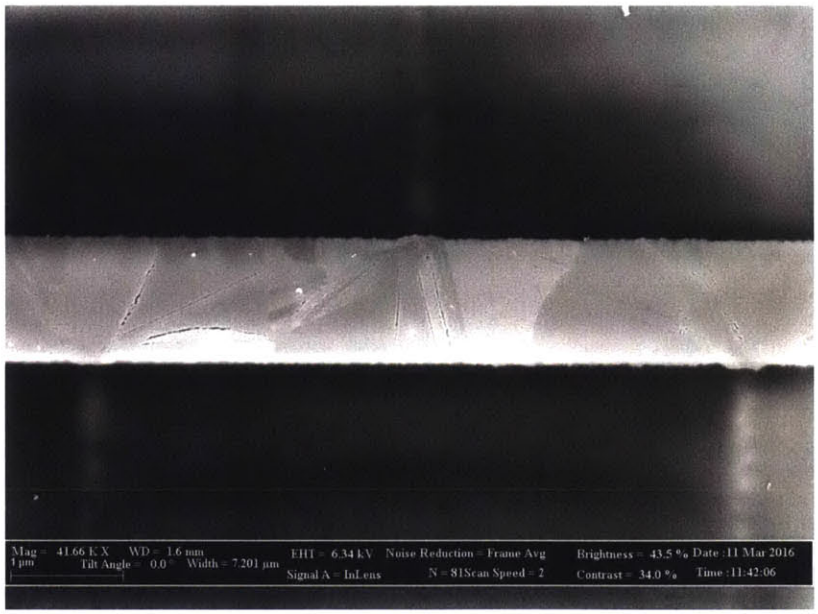
The CMP process involves direct physical contact with the top surface of the wafer and direct contact with the active Ge material. This direct contact can easily lead to contamination of the active material. Therefore the device must be cleaned in order to remove the remaining CMP slurry particles, any organic contamination, and any additional contamination that may degrade the performance of the detectors. A modified piranha clean was utilized which consisted of 5 min in 1:5 H_2SO_4:H_2O, then 15 sec in 1:50 HF:H_2O. This is the exact same post-CMP clean that was used for the crystalline Ge detectors in Section 5.5. After this cleaning step,the devices were imaged again. The post-CMP cleaning step caused slight damage to the Ge surface, as seen in Figure 5-14b. The damage appears to be isolated to grain boundaries or certain specific grain facet orientations. This surface damage effect was not observed in epitaxially grown crystalline Ge. This effect may be caused by the large strain in these devices, especially concentrated at grain boundaries, or the exposure of facets with high surface energies. These strained and high energy facets may be less stable and therefore facilitate the slight etch damage from the cleaning process.

After post-CMP cleaning, the pre-metallization clean and metallization process was exactly repeated from Section 4.5.2 and Section 5.5. However, when the final samples were observed, it was determined that there was no Ge remaining in the trench. The pre-metallization clean is exactly the same as the post-CMP clean, except for the addition of a peroxide step which included 2 min in 1:4 H_2O_2:H_2O. The purpose of the peroxide step is to form a chemical oxide on the surface, which is later removed by the HF dip. However, it was determined that the same peroxide step that produced state of the art devices on epitaxial Ge completely etches and removes Ge grown by the 2D GCLG technique.

Since the peroxide chemical oxidation step was shown to completely etch away the coalesced Ge, it was removed from the pre-metallization cleaning step. Therefore, after CMP, the final device had two equivalent chemical cleaning steps, both included



(a) SEM image of a trench filled with coalesced Ge grains on SiO_2 utilizing the 2D GCLG technique. The image was taken immediately after CMP after Ge growth.



(b) SEM image of an equivalent detector immediately after post-CMP cleaning in dilute H_2SO_4 and HF. Slight surface damage is observed where cleaning procedure has begun to attack some grain boundaries and specific facets.

Figure 5-14: Images of Ge MSM on amorphous substrates during during the fabrication process. The coalesced Ge is seen in the middle. The vertical lines staggered above and below the Ge trench are the nucleation seeds.

5 min in 1:5 H_2SO_4:H_2O, then 15 sec in 1:50 HF:H_2O. This process is similar to a piranha clean and removes organic contamination from the surface. However, it does not form a sacrificial oxide on the surface in order to expose an underlying pristine Ge surface. Since CMP relies heavily on mechanical removal of material, the top surface of the Ge is expected to contain structural defects. These structural defects in the surface create trap states within the Ge which can drastically increase dark current, due to Shockley-Read-Hall defect mediated generation. After performing the modified pre-metallization clean, the Al contacts with a 1 nm Al_2O_3 interlayer were formed exactly as they were in the crystalline Ge detector. The detailed fabrication process flow can be found in Appendix B.

Figure 5-15: Plan-view SEM of final detector. Moderate surface damage is seen on the Ge surface due to overly aggressive chemical cleaning.

After final device fabrication, moderate damage was observed on the Ge surface, as seen in Figure 5-15. It is clear that the cleaning procedure is too aggressive for the Ge grown on SiO_2 at low temperature. Therefore, further work should be done in order to optimize the pre-metallization cleaning procedure. It is unclear why the polycrystalline Ge responds differently to the chemical cleaning. This could be due

to the exposure of different facets which have higher energies and are therefore less stable. It could also be due to the excess strain causing a higher energy surface. In order to eliminate the clearly defective surface, a new chemical cleaning procedure must be developed in order to effectively clean the Ge surface, remove the damaged top surface after the CMP step, while not attacking the Ge.

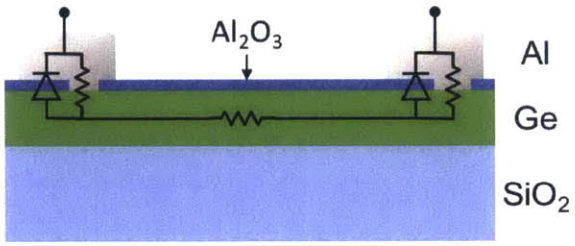


Figure 5-16: The surface roughness on the Ge can cause pinholes in the Al_2O_3 layer, meaning the the Al is in direct contact with Ge at some places. This creates Ohmic contacts in these regions, effectively shunting the Schottky diode contact and allowing for significant leakage current.

The surface damage on the Ge was caused by the chemical cleaning step. Therefore, the surface was significantly textured before the ALD Al_2O_3 and sputtered metal deposition steps. Since the ALD layer is only 1 nm thick, it is likely that the layer was not perfectly conformal and had slight pinholes in it. When the Al was sputter deposited onto this layer, there were likely some regions in which the Al was in direct contact with the Ge. As mentioned in Chapter 4, Al in direct contact with p-type Ge forms Ohmic contacts. Therefore, these regions where Al is directly contacting Ge effectively causes parallel leakage paths and shunts the Schottky diode contacts. This effect is seen schematically in Figure 5-16. These shunts dramatically diminish the effectiveness of the Schottky contacts for dark current suppression.

5.6.2 Detector Performance

Although the detectors on amorphous substrates exhibited process-induced surface damage, the photoresponse was still tested. The light and dark I-V curves are plotted

in Figure 5-17 for a 75 µm long MSM photodetector with a contact separation of 2 µm. These detectors exhibit a clear photoresponse, indicated by the increase in current under illumination when compared to the measurement in the dark.

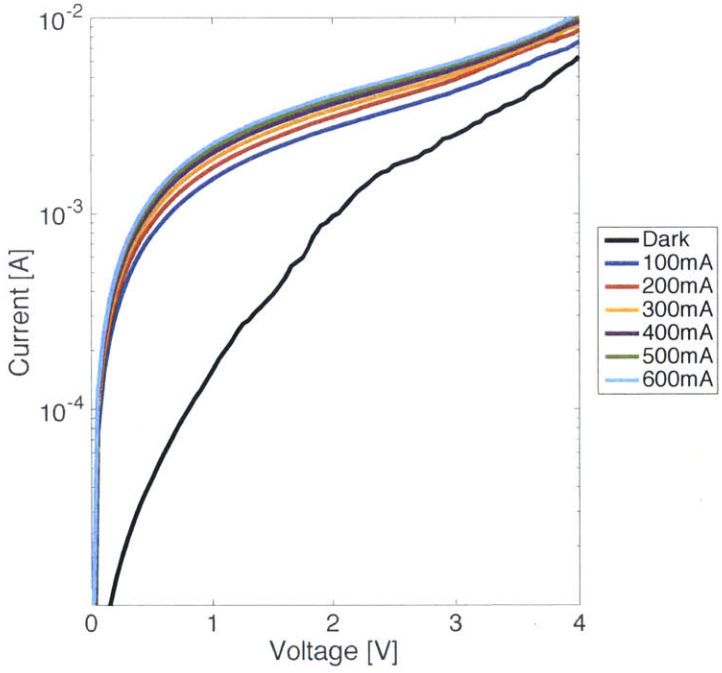


Figure 5-17: Light and dark I-V measurements of a 75 µm long MSM photodetector fabricated on amorphous substrates with a contact separation of 2 µm. Illumination is at 980 nm and the legend denotes the current used to drive the laser. The significant increase in current is due to the generation of a photocurrent, and therefore the MSM structure is acting as an effective photodetector. The high leakage current is due to process-induced surface damage.

The total dark current for these detectors has increased significantly compared to the devices on epitaxial Ge in selectively grown trenches. At a bias of 1 V, the dark current is increased by a factor of approximately 10^4 when compared to the equivalent 75 µm long MSM photodetector fabricated on selectively grown crystalline Ge with a contact separation of 2 µm. This dramatic increase in leakage current is attributed to the significant surface damage seen in Figure 5-15. The surface damage

was caused by the post-CMP and pre-metallization chemical cleaning process. The surface damage creates structural defects in the Ge, thereby introducing trap states in the active material. These trap states can cause significant increases in dark current by defect mediated Shockley-Read-Hall generation. In addition, the ALD process may not be able to conformally coat such a rough surface with only a 1 nm thick Al_2O_3 layer. Therefore, there may be some regions in which the Al is in direct contact with the Ge, thereby creating an Ohmic contact, as demonstrated in Chapter 4. If any part of the metal contact is ohmic, then it serves as a very large parallel conduction path, and therefore effectively shunts the Schottky diode and drastically increases the leakage current.

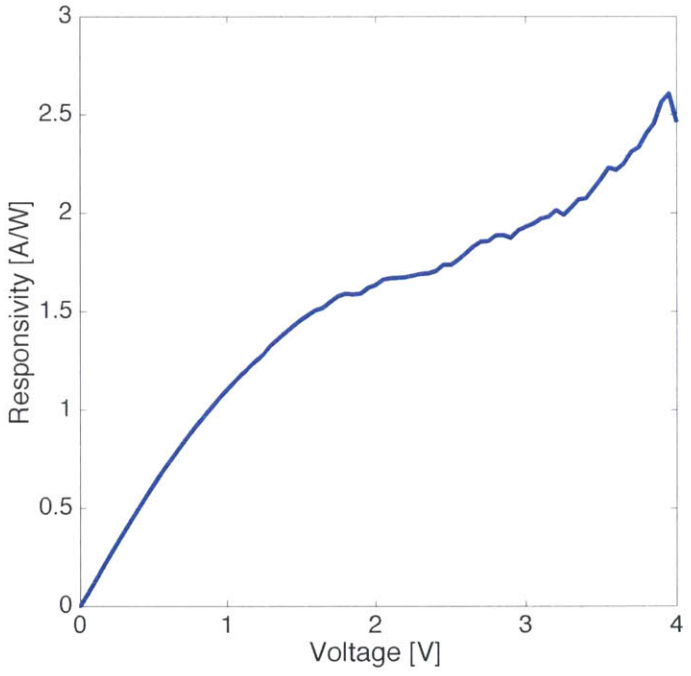


Figure 5-18: Responsivity of MSM photodetectors grown on geometrically confined structures on amorphous substrates. Processing challenges caused surface damage which increase the noise in the measurement.

Despite the significant leakage current present in the detectors on amorphous

substrates, very large responsivities were still measured. For a device with a contact spacing of 1 µm, a maximum responsivity of 2.5 A W^{-1} was measured at a bias of 4 V. The responsivity is not perfectly linear with bias, as expected. This can be attributed to excess noise in the detector due to the large leakage current. Photocurrent is defined by subtracting the dark current at a given bias from the measured current under illumination at that same bias. Therefore, the increase in magnitude and noise of the dark current at high biases contributes to the noise in the photocurrent and therefore the noise in the responsivity at high bias. The presence of process-induced defect states also adversely affects carrier lifetimes and therefore the detector responsivity.

The magnitude of the measured responsivity of these detectors demonstrate the presence of gain with a total internal quantum efficiency up to 315 %. Therefore, these detectors demonstrate a proof of concept for high performance Ge MSM photodetectors on amorphous substrates which are fully compatible with back end of line integration with standard CMOS processing.

5.7 Summary

In this chapter MSM photodetectors were fabricated on Ge. The steady state performance of these detectors was evaluated by measuring the current voltage relationship of the detectors in the dark and under illumination from the surface by a 980 nm fiber coupled laser. The dark measurements gave performance metrics for the leakage current of the device and power consumption. The *I-V* measurements under illumination were used in order to determine the detector responsivity.

Metal contacts were designed to implement an interdigitated contact in order to effectively reduce contact separation while simultaneously minimizing device capacitance. The capacitance was minimized in order to maximize the bandwidth of the detector, while the contact separation was minimized in order to decrease the carrier

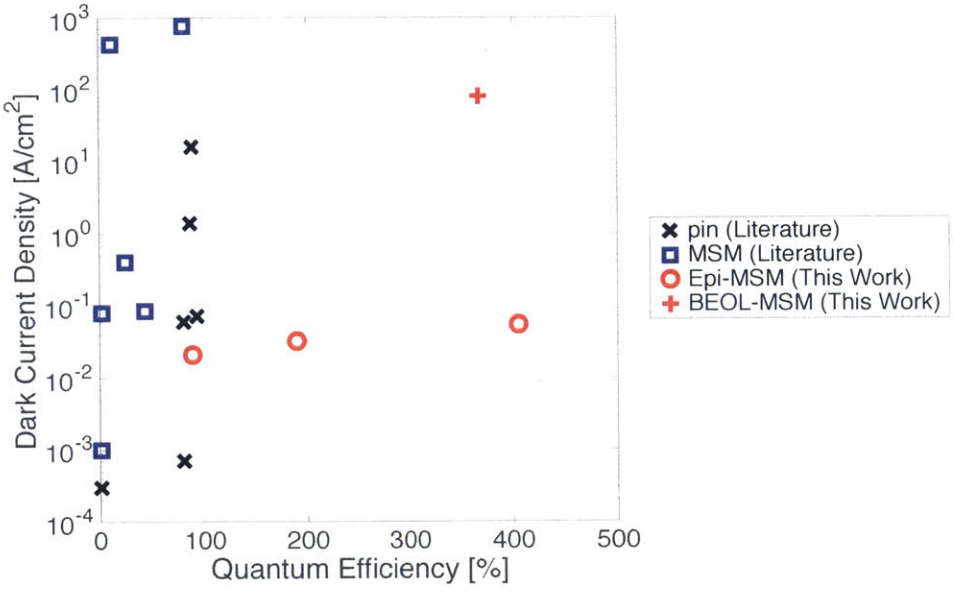


Figure 5-19: A comparison with the performance of the MSM detectors in this work, and published results for other Ge photodetectors. Results extracted from: [16, 18, 39, 42, 43, 99, 100, 115, 116, 127, 128].

transit time. Decreasing carrier transit time was shown to increase both the transit time limited bandwidth of the detector, as well as increase the gain, thereby increasing responsivity of the detector.

Steady state device performance was examined evaluated in a MSM photodetector on blanket epitaxially grown Ge films. These device proved the performance capabilities of the 1 nm Al_2O_3 interlayer contact design. The detector verified that the contacts effectively suppress dark current while simultaneously allowing photocurrent to be collected. The responsivity of the detector was determined by examining the increase in photocurrent as the illumination power was increased. These blanket MSM detectors exhibited high responsivities which were strongly bias dependent with values up to 11 A W^{-1} at a bias of 4 V. The high responsivities are only possible with the presence of gain, indicating the presence of gain in these detectors. However, the responsivity did not scale with contact spacing as expected. Therefore the detector

collection area was shown to be uncertain.

This device design was transferred to crystalline Ge which was selectively grown in 1 µm wide trenches. These device demonstrated very low dark current densities as well as responsivities greater than $3\,\mathrm{A\,W^{-1}}$ at a bias of 4 V and a contact separation of 0.5 µm. The internal quantum efficiency was shown to be in excess of 400 %, proving the presence of gain in these detectors. The responsivity was shown to scale with $1/s$ where s is the separation between contacts. This scaling relationship makes it possible to extrapolate device performance metrics for devices fabricated with more advanced lithography capabilities.

The device design was transferred to Ge grown on amorphous substrates at low temperature by the 2D GCLG technique. Standard post-CMP cleaning and pre-metallization cleaning procedures were shown to affect the polycrystalline Ge material very differently than the crystalline Ge. Significant surface damage was observed on these devices after chemical cleaning. These detectors still exhibited a significant photoresponse with a responsivity up to $2.5\,\mathrm{A\,W^{-1}}$ at a bias of 4 V. However, the damage to the Ge surface generated significant structural damage which contributed to a very large leakage current, and a relatively noisy responsivity relationship. Further work must be done in order to perfect the chemical cleaning procedure in order to eliminate surface damage and lower the leakage current.

Despite the processing damage, these detectors demonstrate a proof of concept for fabricating Ge MSM photodetectors on amorphous substrates while adhering to low temperature processing constraints. These detectors are fully compatible with monolithic integration in the back end of line of a standard CMOS process.

Chapter 6

Summary and Future Work

This thesis has been motivated by the goal of monolithic integration of electronic and photonic devices and systems. In order to continue scaling with Moore's Law, it becomes impractical to integrate photonic devices in the front end of line. Therefore, this thesis proposes integrating photonics in the back end of line of a standard CMOS process. The active components are the most challenging to integrate into the back end of line. Therefore a photodetector was chosen as a demonstration of the capability of fabricating active photonic devices while adhering to the strict back end of line processing constraints. These processing constraints include limiting the thermal budget to 450 °C, and eliminating standard epitaxy processes, since the devices must be fabricated on amorphous substrates.

6.1 Summary

In Chapter 1, the benefits of silicon photonics were elucidated with the opportunity for high-speed, low-power optical interconnects. The major drawback associated with the size of optical components was pointed out, but a solution was proposed. The solution is the integration of optical interconnects within the back end of line.

In Chapter 2, a growth process was developed in order to obtain high quality

Ge material while adhering to back end of line processing constraints. This process employed a two dimensional geometrically confined lateral growth (2D GCLG) technique. The technique relies on two main principles: (1) Ge selectively grows on Si and not SiO_2, and (2) different grain orientations grow at different rates. In order to take advantage of these two principles, a high aspect ratio channel is fabricated where there is amorphous silicon at the base of a channel that has SiO_2 on all side walls, and a narrow opening opposite the amorphous Si. The Ge grows selectively at the bottom of the channel, and the fast growing grain orientation eventually overtakes the slow growing grain orientations and will emerge from the channel as a single crystalline grain. These seeds were then arrayed to open up into a lithographically defined trench, which is of the same dimensions as a waveguide integrated photodetector. The crystalline grains grow until they coalesce with adjacent grains, filling the entire trench with high quality Ge material.

In Chapter 3, the Ge material grown by the 2D GCLG technique was characterized. The main goal of the characterization was to determine whether or not dislocations would form in the material during the growth process. The strain state of the material was measured in order to see if the shear stresses in the material were larger than the critical resolved shear stress, which would indicate the nucleation of dislocations. Optical measurement techniques were used for their high spatial resolution as well as their ease of sample preparation. Raman spectroscopy was used to measure the phonon energy of the Ge, which was related to the strain state of the material. The mismatch between thermal expansion coefficients was proposed as the source of the tensile strain in the Ge. This model accurately predicted the strain state of Ge grown on crystalline Si and amorphous Si, but was inaccurate for Ge grown on SiO_2 by the 2D GCLG technique. Photoluminescence was then used to measure the direct band gap of the Ge, which was also correlated to the strain state in the material. The PL measurements verified the strains that were measured by Raman and confirmed that the strain in the Ge on SiO_2 was twice as large as predicted from thermal mismatch

alone. FIB was used to image the cross section of the coalesced Ge grains, and small voids were observed from incomplete coalescence of neighboring grains. The effect of these voids were determined from finite element stress modeling in COMSOL multiphysics. The voids were shown to act as stress/strain concentrators, increasing the maximum in-plane strain by a factor of two or larger, confirming that they are the cause of high strain in the Ge on SiO_2. The maximum resolved shear stresses were then calculated from the measured strain, and it was verified to be significantly less than the critical resolved shear stress, thereby determining that no dislocation generation occurs in the Ge grown by the 2D GCLG technique.

In Chapter 4, a specific metallization process was developed in order to fabricate high-performance MSM photodetectors. The goal was to fabricate Schottky contacts with high Schottky barriers in order to reduce detector leakage current in the dark, thereby increasing the signal to noise ratio and reducing power consumption. Ge grown at 450 °C was shown to be p-type with a doping concentration of $1.1 \times 10^{18}\,\mathrm{cm}^{-3}$. Literature shows that direct metallization suffers from a Fermi level which is pinned slightly above the valence band, rendering all contacts to p-type Ge as ohmic. Experiments confirmed that contacts to p-type Ge are always ohmic independent of various pre-metallization surface treatments, as well as varying the metal work function. The approach was modified to de-pin the Fermi level by passivating surface states with the addition of a thin interlayer between the Ge and the metal contact. The Ge surface was passivated by a thin Si layer, and then the Si was passivated by thin dielectric SiO_2 or HfO_2 layers. The dielectric layers were kept thin at 1 nm to 2 nm in order to efficiently tunnel through them. This approach was shown to be effective at creating Schottky barriers, but proved to be unstable at elevated temperatures when using an aluminum metallization. The oxygen was found to be more stable when bonded to Al than when bonded to Si or Hf. Therefore, the dielectric was changed to a thin 1 nm Al_2O_3 layer which was deposited by an ALD process. This thin Al_2O_3 layer was found to efficiently passivate the Ge surface, de-pinning the Fermi level, allowing for

the formation of a 0.46 eV Schottky barrier. This metallization was also shown to be stable at elevated temperatures.

In Chapter 5, all of the work from the previous chapters was put together to form Ge MSM photodetectors. The detectors utilized an interdigitated top contact design. This design minimizes carrier transit time as well as device capacitance, thereby allowing for high speed operation. The device structure and process flow were initially tested and developed on blanket Ge material. These devices verified the low leakage current, as expected from the high Schottky barriers developed in Chapter 4. A very strong photoresponse was also observed from normal incidence excitation by a 980 nm laser. This process was transferred to a traditional high-temperature grown epitaxial Ge which was selectively grown in 1 µm wide trenches. State of the art low dark current densities were measured with current densities in the range of $2.07 \times 10^{-2}\,\mathrm{A\,cm^{-2}}$ to $5.73 \times 10^{-2}\,\mathrm{A\,cm^{-2}}$, depending on the contact separation. The highest ever responsivities were measured at greater than $3\,\mathrm{A\,W^{-1}}$ for a bias of 4 V. The high responsivity and the linear relationship with bias confirmed the presence of photoconductive grain in these detectors. The responsivity was shown to scale with $1/L$ where L is the contact separation. Therefore, device performance can be projected for devices with closer contact spacings, as would exist in fabs with higher resolution lithography capabilities. This high performance device structure was then fabricated on Ge on SiO_2 using the 2D GCLG technique. Fabrication problems created some surface damage which significantly increased the leakage current of the devices. However, these devices exhibited photoconductive gain and high responsivities of almost $3\,\mathrm{A\,W^{-1}}$, thereby effectively demonstrating a proof of concept for Ge photodetectors on amorphous substrates for monolithic electronic-phonic integration.

6.2 Future Work

While this thesis provides a proof of concept demonstration of Ge photodetectors that are compatible with back end of line processing constraints, there are still future work that should be carried out to push this concept into a reality. Further materials characterization should be performed in order to fully understand the grain structure of the Ge grown using the 2D GCLG technique. Electron back scatter diffraction (EBSD) mapping can be utilized to quantify the grain size and orientations. TEM can be used in order to verify the lack of dislocations in the material. Deep level transient spectroscopy (DLTS) can be used to quantify the electrical signature of the point defects present from low temperature Ge growth.

In terms of device fabrication, the timed undercut etch of the amorphous Si seeds using TMAH should be eliminated since it introduces significant variability. New designs were presented with the utilization of Si_3N_4 in order to lithographically define all channel dimensions. These improved fabrication approaches can be implemented in order to reduce the variability of the channel dimensions, and the resulting number of grains emerging from each channel. The pre-metallization cleaning procedure must also be revisited in order to reduce the surface damage of the Ge and therefore reduce the dark current leakage of the devices. A very dilute H_2O_2 dip may provide a solution. These devices should also be waveguide integrated in order to demonstrate integration with a larger system. Coupling approaches from Si waveguides to Ge detectors are well known, with butt-coupling and evanescent coupling both providing viable options.

Finally, this approach can be expanded upon in order to make additional active components. An electro-absorption modulator with Ge as the active material is an excellent candidate for the next device since this device does not require a specific doping profile, but only requires a method for applying a large electric field to the Ge. Next, a Ge laser can be made. This material was shown to have significant tensile strain, which is an advantage for luminescence efficiency in Ge. Therefore this

material has some inherent benefits that can be applied to Ge lasers.

While there is a significant amount of work that still must be done in order to make full systems in the back end of line, this thesis has demonstrated a significant proof of concept that high performance active photonic devices can be fabricated while adhering to the challenging back end of line processing constraints. This demonstration paves the way to dense monolithic electronic-photonic integration for the continuation of Moore's Law.

Appendix A

Detailed Process Flow for Epitaxial Ge MSM

This is a detailed process flow for how to fabricate selectively grown epitxial germanium MSM photodetectors, as described in Section 5.5. The notes relate to the specific tools at MIT's Microsystems Technology Laboratory (MTL) fabrication facility. Specific tool names are listed as well as details on process names in each tool and process parameters. The starting material is a 150 mm silicon wafer. The detailed process flow is as follows:

1. RCA clean: rca-ICL
   (a) Standard RCA clean
2. Oxidize wafers: 5D-ThickOx
   (a) Wet oxidation at 1000 °C for 1h 25min.
   (b) Total process time: 4hr, 17min.
   (c) Target SiO_2 thickness: 500 nm
3. Coat wafers: coater6

(a) Recipe: T1HMDS

4. Expose Trenches: i-stepper

   (a) Recipe: WPG.BPTRENCHES.

   (b) Blind:* XM = -9800, XP = 1300, YM = 0, YP = 11000

   (c) Step pitch = 11500 in x and y.

   (d) 130msec Exposure.

   (e) Alignment Method: 1st.

5. Develop wafers: coater6

   (a) Recipe: Puddle3

6. Dry Etch Oxide Trenches: AME5000

   (a) Recipe: BA-OX-TRENCH.

   (b) Etch time: 90 sec. Assume etch rate = 4 nm/s.

   (c) No endpoint (dip in monitor value) observed.

7. Ash resist: asher-ICL

   (a) 3 minutes plasma

8. BOE etch remaining oxide: oxEtch-BOE

   (a) Assume etch rate: 80 nm/min.

   (b) Etch time required: 56 sec. Did timed etch for 65 seconds to be safe (10 nm overetch).

9. RCA clean: rca-ICL

   (a) SC1, Rinse 1

(b) 10 sec HF, Rinse 1

(c) SC2, Rinse 2

(d) 5 sec HF, Rinse 1

(e) SRD Recipe 0: Dry

10. Germanium growth: UHVCVD in SEL

(a) Recipe: GeMSMWG.par (LT Buffer + 5hr growth at 730 + 5 thermal cycles (650-850C))

(b) 30 min anneal at ~850 °C under UHV

(c) Low-temperature Ge buffer growth: 60 nm Ge at 360 °C,

(d) High-temperature Ge growth: 5 h GeH_4 at 730 °C

(e) Anneal Ge at ~850 °C

(f) 5 cycles from 650 °C to 850 °C

11. CMP Ge facets: GnP

(a) Slurry: W2000. 1000mL Slurry + 2000mL Water + 100 mL H2O2 peroxide (30%). Note: G1000 slurry is better.

(b) 300 sec.

12. Acid Clean (TRL): acid-hood

(a) 5 min 1:5 H_2SO_4:H_2O in green tank

(b) Rinse

(c) 15 sec 1:50 HF:H_2O

(d) Rinse

(e) Spin-rinse-dry

13. Acid Clean: premetal-Piranha

    (a) 5 min 1:5 H_2SO_4:H_2O in blue tank

    (b) Rinse

    (c) 2 min 1:4 H_2O_2:H_2O in green tank

    (d) Rinse

    (e) 15 sec 1:50 HF:H_2O

    (f) Rinse

14. 1 nm ALD Al_2O_3 deposition: ALD-Oxford

    (a) Recipe: "ALD Al2O3 Plasma"

    (b) 9 Cycles (Assumed 1.1 Å per cycle deposition rate)

    (c) Chamber temperature: 300 °C

15. Sputter 200 nm aluminum: endura

    (a) Recipe: "AL 2KA DEP"

    (b) 10 sec deposition time

16. Coat with photoresist: coater6

    (a) Recipe: "T1HMDS"

17. Expose patterns: i-stepper

    (a) Recipe: WPG.BPTRENCHES.

    (b) Blind:7 XM = 0, XP = 11000, YM = 0, YP = 11000.

    (c) Step pitch = 11500 in x and y.

    (d) X Shift = -13750, Y Shift = -1.

    (e) 130msec Exposure.

(f) Align. Method: EGA.

(g) Changed alignment mark locations. Search X: (754.5, 5198), Search YT: (546, 5194), EGA X: (667, 4782), EGA Y: (1073, 4838)

18. Develop photoresist: coater6

(a) Recipe: "Puddle3"

19. Etch 200 nm aluminum contacts: rainbow

(a) Recipe: "Baseline"

(b) Endpoint set for 30 sec with 5 sec overetch (Assume etch rate of ~80 sec /μm)

(c) Endpoint reached in 18 sec

20. Ash photoresist: asher-ICL

(a) 3 min of plasma

Appendix B

Detailed Process Flow for Ge MSM on Amorphous Substrates

This is a detailed process flow for how to fabricate germanium MSM photodetectors on SiO_2 substrates, as described in Section 5.6. The notes relate to the specific tools at MIT's Microsystems Technology Laboratory (MTL) fabrication facility. Specific tool names are listed as well as details on process names in each tool and process parameters. The starting material is a 150 mm silicon wafer. The detailed process flow is as follows:

1. RCA clean: rca-ICL
   (a) Standard RCA clean
2. Oxidize wafers: 5D-ThickOx
   (a) Wet oxidation at 1000 °C for 1h 25min.
   (b) Total process time: 4hr, 17min.
   (c) Target SiO_2 thickness: 500 nm
3. Piranha Clean: premetal-Piranha

(a) Standard green piranha, no HF dip

4. Deposit 50 nm amorphous Si: DCVD

   (a) Recipe: A-SI 500A CHC

5. Coat wafers: coater6

   (a) Recipe: T1HMDS

6. Expose Nucleation Seeds: i-stepper

   (a) Recipe: WPG.BPTRENCH

   (b) 300,400,500,600 nm offsets in different quadrants.

   (c) xlimits 100:6500 for first exposure, then 1400:6500 for second exposure.

   (d) Exposure: 130 msec

   (e) Step pitch: 7000 in x and 11500 in y.

   (f) Blind number 1-4. Xlim(100,6500) then (1400,6500). Ylim(-11000,0) then (-11000,0).

   (g) Center shift(0,0) then (0.3,0),(0.4,0),(0.5,0),(0.6,0).

   (h) 300nm offset (Blind1) in upper left, 400nm offset (blind 2) in upper right, 500 nm offset (blind 3) lower left, 600 nm offset (blind 4) lower right.

   (i) Alignment: First

7. Develop wafers: coater6

   (a) Recipe: Puddle3

8. Thin resist in oxygen plasma: AME5000

   (a) Chamber A.

   (b) Recipie: PR THINNING.

(c) O_2 Plasma for 30sec

9. Etch a-Si seeds: AME5000

   (a) Chamber B

   (b) Recipe: BASELINE POLY

   (c) Endpoint detection for etch, max time of 35 sec. Overetch for 12 sec.

   (d) Reached endpoint at 28 sec. Cl and HBr etch gas. Monitor drops slightly, goes up to a peak, and endpoints when monitor flattens off at top of peak.

10. Ash resist: asher-ICL

    (a) 3 minutes plasma

11. Piranha Clean: premetal-Piranha

    (a) Standard green piranha, no HF dip

12. Deposit 300 nm SiO_2: DCVD

    (a) Recipe: OXIDE 3KA CHA.

    (b) Color was peach on blanket regions, and purple/blue/green on die where aSi had been etched.

13. Coat wafers: coater6

    (a) Recipe: T1HMDS

14. Expose Trenches: i-stepper

    (a) Recipe: WPG.BPTRENCH.

    (b) Blind 5.

    (c) Step pitch: x= 7000, y=11500

(d) XM = -11000, XP = -5500, YM = 0, YP = 11000

(e) X Shift = 13751, Y Shift = -11001

(f) Align. Method: EGA

15. Develop wafers: coater6

(a) Recipe: Puddle3

16. Dry Etch Oxide Trenches and s-Si Seeds: AME5000

(a) Chamber A then B.

(b) BA-OX-TRENCH in Chamber A. Timed for 75 sec. No endpoint detected. Very slight signal drop from oxide etch at 65 sec.

(c) BASELINE POLY in Chamber B. Endpoint w/ max. time of 35sec and 12 sec over-etch.

17. Ash resist: asher-ICL

(a) 3 minutes plasma

18. TMAH Undercut Etch: TMAH-KOHhood

(a) TMAH for 150 sec at 80°C. (Had even better results with 200 sec etch)

(b) 25% TMAH, straight from the bottle, no dilution.

(c) Assume 2 - 4.5 nm/s etch rate. (300nm - 675nm undercut).

19. Double Piranha Clean: premetal-Piranha

(a) 10 min in yellow tank, rinse

(b) 10 min right tank, rinse

(c) 3 sec HF, rinse

(d) SRD

20. RCA clean: rca-ICL
    (a) SC1, Rinse 1
    (b) 10 sec HF, Rinse 1
    (c) SC2, Rinse 2
    (d) 5 sec HF, Rinse 1
    (e) SRD Recipe 0: Dry
21. Germanium growth: UHVCVD in SEL
    (a) Recipe: GeMSMWG2.par.
    (b) 3 hr anneal at 450C for H_2 outgassing (100% throttle, no gas)
    (c) 32 hrs of Ge growth at 450C (1e-2 mBar).
22. CMP Ge Overgrowth: GnP
    (a) Slurry: G1000. 1000mL Slurry + 1000mL Water + 66 mL H2O2 peroxide (30%)
    (b) 140 sec total
23. Post-CMP Clean: premetal-Piranha
    (a) 5 min 1:5 H_2SO_4:H_2O in yellow tank
    (b) Rinse
    (c) 15 sec 1:50 HF:H_2O
    (d) Rinse
    (e) Spin-rinse-dry
24. Pre-metallization clean (Note: this caused surface damage): premetal-Piranha
    (a) 5 min 1:5 H_2SO_4:H_2O in yellow tank

(b) Rinse

(c) 15 sec 1:50 HF:H_2O

(d) Rinse

(e) Spin-rinse-dry

25. 1 nm ALD Al_2O_3 deposition: ALD-Oxford

(a) Recipe: "ALD Al2O3 Plasma"

(b) 9 Cycles (Assumed 1.1 Å per cycle deposition rate)

(c) Chamber temperature: 300 °C

26. Sputter 200 nm aluminum: endura

(a) Recipe: "AL 2KA DEP"

(b) 10 sec deposition time

27. Coat with photoresist: coater6

(a) Recipe: "T1HMDS"

28. Expose patterns: i-stepper

(a) Recipe: WPG.BPTRENCHES.

(b) Blind:7

(c) XM = 0, XP = 11000, YM = 0, YP = 11000

(d) Step pitch = 7000 in x and 11500 in y.

(e) 130msec Exposure

(f) X Shift = 0, Y Shift = -11001

(g) Alignment Method: EGA.

(h) Changed Focus to -0.5um because of note on stepper

29. Develop photoresist: coater6

    (a) Recipe: "Puddle3"

30. Etch 200 nm aluminum contacts: rainbow

    (a) Recipe: "Baseline"

    (b) Endpoint set for 30 sec with 5 sec overetch (Assume etch rate of ~80 sec /μm)

    (c) Endpoint reached in 18 sec

31. Ash photoresist: asher-ICL

    (a) 3 min of plasma

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