GATED AMPLIFIERS FOR DATA PROCESSING IN SPACE

by

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ABSTRACT

The gated amplifier, a new circuit which incorporates integral electronic switching into the design of an operational amplifier, is described. Salient features of the gated amplifier are its low power consumption and its versatility for use in a variety of data-processing operations. Many gated-amplifier data-processing systems are less complex than systems which use conventional circuits to perform similar functions. The power consumption of gated-amplifier systems is often 1/100 to 1/1000 that of conventional systems. These features make the gated-amplifier concept particularly attractive for use in space data-processing applications.

A gated-amplifier circuit is designed and analyzed. Measured and predicted performance characteristics are compared. Representative data-processing systems are designed with gated amplifiers and test results for two systems, a digital-to-analog converter and an analog multiplier-divider, are presented.

In order to realize the full advantage of the gated-amplifier concept, certain ancillary circuits such as logic circuits and shunt switches are required. Representative designs are included.

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CHAPTER I

INTRODUCTION

This report presents the results of a program of research concerned with the development of a new type of operational amplifier that I call a gated amplifier. The gated amplifier incorporates electronic switching into the design of an operational amplifier in order to enhance versatility and to reduce the power required to perform many types of analog data-processing operations.

These two major advantages are best illustrated with examples of systems developed as part of the research. Systems have been designed to perform function generation, multiplication or division, and analog-to-digital and digital-to-analog conversion, as well as linear operations such as integration. These systems require a small amount of auxiliary circuitry in addition to the gated amplifier. Furthermore, most of the auxiliary circuits are logic circuits which require no adjustment and which consume low power.

In many situations gated amplifiers can reduce the power required to perform analog data-processing operations by two to three orders of magnitude compared with conventional techniques. Two of the systems which were designed were constructed and tested to demonstrate the value of the gated-amplifier approach to data processing. One of these was a D-A converter. Ten-bit accuracy is possible with this system, and system energy requirements are less than 10 microjoules per bit. For example, the system can perform 10-bit conversions at a rate of 10 complete conversions per second with an average power consumption under 1 mW. A second tested system is an analog multiplier-divider which generates ratios of the form $\frac{XY}{Z}$. The three input variables can contain frequency components greater than 100 c/s, and the system power consumption varies from 1 mW to 6 mW depending on the types of inputs applied to the system.

The experimental circuits and systems were specifically tailored toward use in space-electronic systems, since the most immediate use of the gated amplifier may be in space experiments where power is at

a premium. In order to design circuits of this type, complexity and in some cases certain performance characteristics were compromised to reduce power consumption. This does not imply that gated-amplifier applications are limited to space-electronic systems. The basic concepts and simulation techniques developed as part of the research can also be used for general-purpose analog computation, particularly in the area of hybrid computation where the inherent switching capability of the gated amplifier should prove useful. Some circuit redesign would be required in order to realize the maximum potential of the technique in hybrid computers.

This chapter provides a summary of the most important gated-amplifier concepts, as well as a section indicating the content of remaining chapters. The reader may then select those chapters with the greatest relevance to his particular interests.

A. THE BASIC APPROACH

Certain types of digital switching circuits are self-optimizing in the sense that the power required is essentially linearly related to the instantaneous frequency of operation. Circuits of this type are realized with complementary-transistor logic and specific examples are included in Chapter V where the designs used for ancillary circuits are described.

The same general approach where power consumption automatically adjusts as a function of frequency of operation does not seem to exist for circuits operating continuously as linear circuits for fundamental reasons. The bandwidth of a particular transistor (at least a low current levels) is directly proportional to collector current, while the maximum dynamic range of an amplifier is directly related to supply voltage. Therefore, bandwidth and dynamic range cannot be specified independent of operating power level.

Although the operational amplifier is a very useful analog data-processing element, it is subject to the bandwidth-dynamic range-power limitation characteristic of linear circuits. A first approach to circumventing this limitation might involve switches which could be used to disconnect the amplifier from its power supply when power is not required for data processing. This approach is unsatisfactory for

at least two reasons. First, an average power reduction is possible only for a limited class of input signals. To take advantage of power-supply switching one must have a signal which is present only a fraction of the time, and advance knowledge of the time the input signal will be present is required. Second, no versatility is gained from this approach compared with a continuously-on operational amplifier.

The approach used with the gated amplifier is illustrated by the model shown in Fig. 1-1. The gated amplifier represented by this model possesses two states as follows:

The three switches are closed and the output voltage (as a function of the complex frequency s) is related to the two inputs as

$$E_{out}(s) = [E_1(s) - E_2(s)]\ A(s)$$

This state is defined as the ON state. (All voltages are referred to a common ground which is not included in the block diagrams presented in this report).

The amplifier is defined as OFF with the three switches open and in this state the power consumption is close to zero. No intermediate condition exists; all three switches shown in Fig. 1-1 must have the same state. Only the three terminals shown external to the dashed lines in Fig. 1-1 are available for use.

The gating characteristics of the gated amplifier represented by Fig. 1-1 offer several significant advantages when the circuit is used as a data-processing element in space systems. Average power consumption can be reduced for a large class of input signals because of the possibility of operating the amplifier in a periodically-gated or sampling mode. Certain simple processing operations including storage, scaling of variables, and filtering are possible while the amplifier is OFF. Furthermore, sampling can be combined with capacitive storage and processing during intervals when the amplifier is OFF in order to increase the versatility of the gated amplifier.

B. THE GATED-AMPLIFIER CIRCUIT

The design approach used to realize the gated-amplifier circuit differs from that normally used for operational amplifiers because of

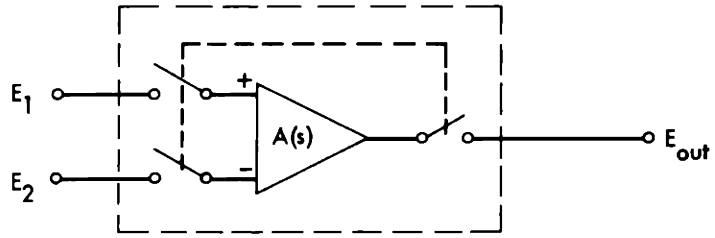

Fig. 1-1 Model for the Gated Amplifier
(Shown in OFF State)

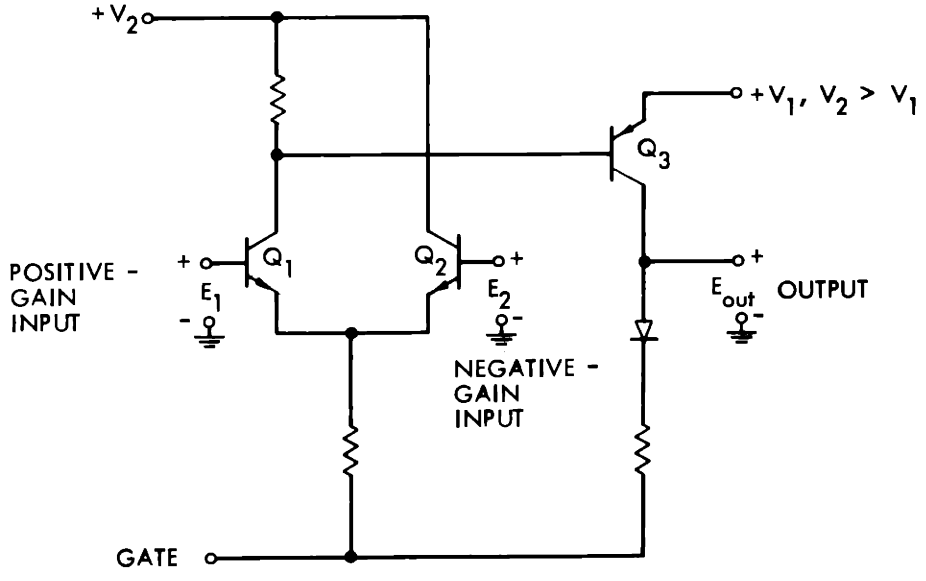

Fig. 1-2 Simple Gated Amplifier

the special characteristics of the circuit. The most important of these characteristics are:

1. It is necessary to include provision for gating.
2. ON-state power consumption must be minimized even though gating is used to reduce average power consumption. At best, gating leads to an average power consumption equal to the amplifier ON-state power consumption multiplied by its duty factor (ratio of ON time to total time). Therefore, reduction of ON-state power leads directly to an average power reduction.
3. The circuit must deliver high output current to permit rapid charging of the large capacitors often used as loads.
4. It is necessary to include provision for modification of the amplifier transfer function in order to compensate for widely varying feedback ratios and loads often used with the gated amplifier.

A very simple amplifier which displays two of the required gated-amplifier characteristics is shown in Fig. 1-2. This circuit is ON with the gate lead at a negative potential, and in this state provides gain between a differential input stage* and a single-ended output. If the gate lead is switched to a positive voltage, the two inputs are isolated since transistors Q_1 and Q_2 are cut off. Transistor Q_3 is also turned off and the diode is reverse biased so that the output is isolated. The power consumption is reduced to a level determined by various leakage currents.

The dominant pole of this type of amplifier is caused by collector-to-base (or Miller) capacitance associated with transistor Q_3, and increasing the size of this capacitance controls the transfer function. Small capacitors suffice because of the high gain associated with Q_3,

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*Throughout this report, the two inputs of the gated amplifier will be designated as the negative-gain input and the positive-gain input. A d-c signal applied between these two terminals so that the positive-gain input is more positive than the negative-gain input forces the output voltage positive with respect to ground.

and therefore gating time is not degraded by this compensation technique.

Unfortunately, many performance characteristics of the simple configuration are poor, and it is therefore unacceptable for use in demanding applications.

The prototype gated-amplifier circuit developed as part of the research maintains the two advantages of the simple circuit shown in Fig. 1-2, but numerous modifications are included to correct performance deficiencies. A constant current source is added to the differential stage in order to improve common-mode rejection ratio. The inverter shown as Q_3 in Fig. 1-2 is replaced with a cascode amplifier to improve frequency response. A current source is used as a load for the cascode amplifier, and this technique results in a voltage gain of 25,000 across a single amplifying stage. This approach of obtaining most of the voltage gain in one stage results in a transfer function which is nearly ideal for use in applications involving feedback. The transfer function has only two poles located at frequencies where the amplifier voltage gain exceeds unity, and the separation between these two poles is more than two decades. Greater separation can be obtained by shunting small capacitors around the cascode amplifier, and this method can be used to stabilize the amplifier for all expected loads and feedback ratios.

A unity-voltage-gain buffer amplifier is used to isolate the high-impedance node at the output of the cascode circuit from loads which may be connected to the gated amplifier. The buffer amplifier employs emitter followers biased in a novel way as a Class-B output stage. The quiescent bias current required by the buffer amplifier is approximately 100 μA and the stage can deliver output currents in excess of 250 mA.

The prototype gated-amplifier circuit has a unity-voltage-gain frequency in excess of 30 Mc and requires approximately 15 mW of power when ON.

Gating is accomplished using the two current sources as gating switches. These current sources are required when the amplifier is ON and are not included only to permit gating.

Certain additional components are added to the basic gated-amplifier circuit to improve performance characteristics as follows:

1. Transistors are used to discharge several critical nodes in the amplifier at turn OFF in order to minimize turn-off time. Slow turn OFF could introduce errors in the value of a voltage stored on a capacitor.

2. Temperature-dependent compensation is used to reduce both ON-and OFF-state input current.

3. The voltage drift referred to the input of the amplifier is reduced by compensation.

The ON-state performance characteristics of the gated amplifier have been compared with several commercially-available operational amplifiers. Many specifications are essentially identical. The major differences summarized below reflect the differences in intended application and the novel design approach used to realize the gated-amplifier circuit:

1. The maximum output voltage of the gated amplifier is ± 4 volts compared with a typical value of ± 10 volts for solid-state operational amplifiers.

2. The maximum output current of the gated amplifier is more than an order of magnitude higher than conventional operational amplifiers. This is required to permit rapid capacitor charging.

3. The d-c open-loop gain of the gated amplifier is somewhat lower than that of conventional operational amplifiers. This reflects an engineering tradeoff made in the choice of certain transistors to improve frequency response. The open-loop gain of the gated amplifier (80,000) is sufficient for all intended applications.

4. The unity-voltage-gain frequency of the gated amplifier is at least a factor of three higher than any existing differential-input operational amplifier.

5. The power consumption of the gated amplifier in the ON state is between 1 and 2 orders of magnitude lower than conventional operational amplifiers.

The important characteristics of the amplifier which are directly attributable to gating include:

1. The turn-on time (time required for the amplifier to become active following application of an ON pulse) is 0.7 μs.
2. The total charge supplied by any of the three available terminals at turn OFF is less than 4×10^{-11} coulomb. This insures errors from this source of less than 1 mV in typical sampling operations.
3. The leakage current at any of the three terminals with the amplifier OFF is typically 10^{-11} A. Prolonged storage of voltages on capacitors connected to the terminals is thus assured.
4. The OFF-state power consumption is 50 μW.

C. APPLICATIONS

The design approach used to realize the gated amplifier and the resultant performance characteristics summarized to this point represent an important part of the research. However, the ultimate value of gated-amplifier techniques can only be determined from the possible applications of the circuit; this section outlines some of these applications.

The approach to power minimization used with gated amplifiers is threefold. First, a data-processing system should be designed with a minimum number of gated amplifiers. Second, the system should be organized so that the amplifiers are ON a minimum fraction of the time. Third, the amplifiers should consume low power when ON. Only the third of these items has been mentioned in connection with the design procedure outlined earlier; the other two are intimately related to the system-design techniques used with gated amplifiers.

Complex data-processing operations are realized by combining several fundamental operations. The number of these fundamental

operations is at present quite low, and I feel that many additional equally important operations will be discovered as greater experience is gained with the gated amplifier. The known techniques of greatest value are summarized in the following paragraphs.

Sampling in one form or another is included in nearly all gated-amplifier applications. Sample and hold circuits can be constructed using only a gated amplifier and a storage capacitor. The switching required to change from the sample to the hold mode is easily accomplished. The ultimate accuracy of gated-amplifier samplers is limited by dielectric absorption in the hold capacitor rather than by gated-amplifier errors. Samples can be acquired in less than 5 μs, and the typical ratio of hold time to sample time is 4×10^7 for an error of one percent of full output. This compares favorably with conventional circuits where ratios from 10^4 to 10^6 are typical.

A second basic operation provides a particular type of time summation. The value of an analog variable at discrete time intervals can be summed over any number of these intervals. One application of this operation is as an approximate integrator, where average power can be drastically reduced since the amplifier remains OFF most of the time.

A gated integrator is identical to a conventional analog integrator except that a gated amplifier is used in place of an operational amplifier. This permits control of initial conditions with no need for additional switching in most cases. One important use of the gated integrator is in voltage-to-time conversion circuits. The time required for the ramp generated by a gated integrator supplied with a slowly varying input Y to reach a magnitude X is determined using a second gated amplifier as a comparator. The resultant time is proportional to $\frac{X}{Y}$. Power consumption is minimized by gating both amplifiers OFF as soon as the conversion is complete. One possible application of voltage-to-time conversion is as a means for A-D conversion.

Examples of three of the more complex operations which are possible by combining the basic operations are summarized below.

Function generations (generation of $Y = F(X)$ where X is an analog variable) can be easily instrumented with gated amplifiers. In

many cases the resultant system is less complex than a conventional realization since the need for nonlinear diode networks is eliminated. One technique uses cascaded gated integrators to generate outputs proportional to t, t^2, t^3, etc. The required function is expanded in a Taylor series using time as the independent variable. The expansion is sampled at a time proportional to X in order to generate the required function. A second approach involves the simulation of a differential equation with a solution equal to $F(t)$ using essentially standard analog simulation methods. The solution is sampled at a time proportional to X.

A multiplier-divider system using gated amplifiers was constructed as part of the experimental program. A time proportional to the ratio of two slowly varying analog quantities $\frac{X}{Z}$ is generated. A gated integrator with an input Y is operated for the time interval $\frac{X}{Z}$, with a resultant final output equal to $\frac{XY}{Z}$. This value is sampled. The experimental system is operated repetitively at a 1-Kc sampling rate and the output of the sample-and-hold circuit is filtered to provide a continuous ratio in cases where the frequency components of the input signals are low compared to 1 Kc.

The system has an rms error for time-invariant inputs of 0.5 percent of full output, and minor modifications should improve this figure to 0.1 percent. In cases where the ideal output contains no frequency components above 100 c/s, the actual system output is the ideal output delayed by approximately 1 ms. Higher-frequency signals lead to a somewhat distorted output, but in many less demanding applications operation to 250 c/s is possible. The power requirements of this system varied from 1 mW to 6 mW depending on the amplitude and frequency of the three input signals.

A second experimental system was designed to provide direct conversion of sequential, natural-binary inputs to a proportional analog output. An interesting feature of this system is that all required temporary data storage is accomplished with capacitors so that no flip-flop storage is needed. This approach results in a compact system.

A modified sampling circuit is used in conjunction with passive charge transfer between two capacitors during intervals when the sampling amplifier is OFF to generate a waveform with values equal

to 4, 2, 1, etc. volts at time intervals when a binary input can be present. A time summation circuit totalizes the magnitude of this waveform at all times when the input is a binary "1", and also attenuates the resultant sum by a factor of 1/2 to provide an analog output with 2 volts corresponding to the most significant digital bit.

The system error is 2 mV rms so that 10-or 11-bit conversions are possible. The required energy per bit of conversion is less than 10 microjoules.

D. RELATED TECHNIQUES

The basic operational method of using feedback for the accurate generation of transfer functions has been recognized for many years. The development of chopper stabilization[1*] in 1950, which permitted reduction of the drift inherent in earlier d-c amplifier designs to a tolerable level, made possible electronic analog computation as it is known today. More recently, semiconductors have been used in the design of operational amplifiers, leading to significantly increased computing frequencies and reducing voltage drift to the point where chopper stabilization is no longer required in many applications. Many manufacturers now offer solid-state operational amplifiers.

Solid-state electronic switches have also been designed within the past few years, and these switches are being used to increase the versatility of operational amplifiers. This has led to the new area of hybrid analog computation.

The diamond circuit[2] is one existing design which incorporates switching into an active-circuit design. The diamond circuit is essentially a four-diode gate where the diodes have been replaced with base-to-emitter junctions of transistors. This results in a design with high current gain and unity voltage gain. This circuit is very useful as a high-speed sample-and-hold circuit and has been used in several space experiments. Methods have been reported for using this circuit in more complex data-processing operations. However, the diamond

*Numerical superscripts refer to items in the Bibliography

circuit does not have a differential input and cannot be used directly to provide voltage gain greater than unity. Therefore, most of the techniques developed for use with the gated amplifier cannot be implemented with the diamond circuit.

At least one digital technique has been reported[3] which is somewhat analogous to a technique used with gated amplifiers. Ordinary flip-flops are pulsed ON periodically by including a switch in series with the power-supply voltage. Logic must be included which insures that the flip-flops are ON whenever a change in state is required. During the time interval when a flip-flop is OFF its state is maintained as a capacitor voltage. This voltage is used to restore the original state of the flip-flop when power is reapplied. This method has been tested experimentally and has resulted in dramatic average power reduction, particularly in cases where the input signals are low in frequency so that the flip-flops are ON a minimum fraction of the time. It will be seen that this type of average power-bandwidth tradeoff is also characteristic of gated-amplifier systems.

The voltage gain of a gated amplifier when ON is supplied by a differential amplifier followed by a cascode amplifier. This combination provides excellent high-frequency performance, and the standard circuits are modified so that high d-c gain is achieved simultaneously. The advantages of the differential amplifier-cascode amplifier interconnection as a design for high-frequency, low-power amplifiers have been reported earlier.[4]

E. CONTENT OF REMAINING CHAPTERS

This section is included to assist the reader in selecting sections of the report that are of greatest interest to him. To permit selective reading, the chapters have been written so that any one chapter can be read with minimum reference to other chapters. Chapters II and III pertain to the design and testing of the gated amplifier, Chapter IV presents system applications, and Chapter V pertains to the ancillary circuits.

Chapter II outlines the design of the gated amplifier, starting from the design objectives. The three individual stages used for the circuit are introduced and models which may be used to relate linear-region

performance to circuit parameters are developed.

An operational amplifier is designed by interconnecting the three circuits and the transfer function of this operational amplifier is developed for the specific element values used and for two loading conditions.

The technique used to gate the amplifier is introduced, and additional gating components are added to the basic operational amplifier to form the basic gated amplifier.

Certain additional components are required to improve both ON- and OFF-state performance. Incorporating these elements into the basic gated-amplifier circuit completes the design of the circuit used for the experimental portions of the research.

Chapter III presents the measured performance characteristics of the gated amplifier, and the actual measurement techniques employed are included in many cases. It is necessary to include details of measurement since indirect measurements are often required and care is needed to minimize instrumentation errors.

The measured linear region transfer function is compared with the expression derived in Chapter II for two amplifier loads.

A brief analysis of many gated-amplifier performance characteristics is included in Chapter III, and the results are used to show that measured characteristics are realistic in terms of device parameters.

The performance of the gated amplifier in the ON state is compared with five commercially available operational amplifiers. While the design of the gated amplifier has not been optimized for use as a continuously ON amplifier, this comparison does illustrate the advantages of the basic design approach.

A section on the reliability of the gated amplifier is included. Certain features of the gated amplifier such as low-power operation of active devices and the simplifications which are possible in system design are shown to offset the somewhat greater complexity of the gated-amplifier circuit compared with conventional operational amplifiers.

Chapter IV is devoted to gated-amplifier applications. The techniques used for assembling low-power data-processing systems are illustrated in the form of a series of examples. The basic operations

are described initially and more complex systems for function generation, multiplication-division, and D-A conversion are then developed from the basic operations. Several applications of gated amplifiers to hybrid analog computation are indicated.

The methods which are used to predict system average power consumption and errors from amplifier characteristics are included with the examples. The test results of the systems that were constructed are correlated with predicted values.

Chapter V presents the designs used for the various ancillary circuits required in gated-amplifier systems. Circuit diagrams, performance characteristics, and a brief description of operation are included for various logic circuits, a clock, and shunt switches.

Design approaches which may be used for several additional circuits that will probably be required in more complex systems are also outlined. These circuits, which have not been built, include a high-efficiency power supply and improved shunt switches.

The ancillary circuits are general-purpose designs, and should prove useful in many systems not involving gated amplifiers. To this end, most of Chapter V is written so that no reference to other chapters is required.

Chapter VI summarizes the most important results of the research. Several areas where minor circuit modifications could yield improved performance are outlined, along with suggestions concerning more extensive redesign which should be possible with improved device and fabrication technology.

One possible improvement in system organization that may result in further power economy is suggested for future research.

Appendix I presents the actual details of construction of the prototype circuits. Parts-selection procedures and initial adjustments made to the circuits are included. This material, together with the design and test results of Chapter II and III, should permit duplication of the prototype gated-amplifier circuit if required.

Appendix II outlines an extension of the gated-amplifier concept which is useful for multiplexing.

CHAPTER II

THE GATED-AMPLIFIER CIRCUIT

This chapter describes the design techniques that have been used to realize the gated-amplifier circuit.

The initial section outlines the objectives of the gated-amplifier design procedure. In many cases the performance characteristics typical of existing operational amplifiers must be improved so that the gated amplifier can be used to full advantage in all intended applications. As a result, much of the material can be used directly for the design of improved operational amplifiers, and this represents a subsidiary benefit of the research.

The three circuits that form the basic structure of the gated amplifier (differential amplifier, cascode amplifier, and a particular type of Class-B emitter-follower buffer amplifier) are discussed and linear-region models are developed with the aid of an appropriate transistor model. The analysis leading to the linear-region models is completely general in the case of the differential amplifier and the cascode amplifier, whereas the buffer amplifier analysis is limited to the cases of high-impedance load or large capacitance load. These two types of loads include all loads used during the course of the research and permit a significant simplification of the buffer-amplifier model.

A basic operational amplifier is formed by the interconnection of the three amplifying stages. All circuit elements that influence the linear-region ON-state performance of the gated amplifier are included. The linear-region transfer function is developed for the two loading conditions and results are presented in the form of Bode plots. The effects of including capacitive feedback around the cascode amplifier in order to control its transfer function (and therefore the transfer function of the basic operational amplifier) are illustrated.

The basic operational amplifier can be turned ON and OFF without any circuit modifications. However, turn-off time is slow, and therefore its performance as a gated amplifier is unacceptable. Additional components to speed up turn OFF are added to the basic operational amplifier to form the basic gated amplifier. Other additional

components are included to improve certain characteristics (primarily drift referred to the input and ON-and OFF-state terminal currents) so that the resultant gated-amplifier circuit can be used in all applications without modification.

The gated-amplifier circuit presented in this chapter is, of course, only one possible implementation of the gated-amplifier concept. The circuit is intended for use in space applications, and for this reason many of the engineering compromises required in the design process are made in favor of reduced power consumption. The basic design approach, however, can easily be used to develop other gated-amplifier circuits better suited to other specific applications.

A. DESIGN OBJECTIVES

A model for the gated amplifier has been presented in Fig. 1-1 and the gated amplifier represented by this model has two states; ON (switches closed) and OFF (switches open). In the ON state the gated amplifier is indistinguishable from an operational amplifier, and the performance of this operational amplifier determines to a large degree the usefulness of the gated-amplifier circuit, since gating offers no method to circumvent poor ON-state performance.

The ideal characteristics of operational amplifiers are well known[5] and the calculation of errors introduced by nonideal characteristics is straightforward. The most important characteristics shared by the gated amplifier and operational amplifiers can be summarized as follows:

1. The open-loop gain should be sufficiently high so that the transfer function of the amplifier with feedback is determined only by the feedback elements.
2. The voltage drift referred to the input should be low.
3. The input current should be low.
4. The common-mode rejection ratio should be high. In many operational-amplifier applications inputs need be applied only to the negative-gain input terminal, and in such cases common-mode rejection is unimportant. However, gated-

amplifier applications often require that signals be applied to both input terminals.

5. The noise referred to the input should be low.

The techniques used for system design with gated amplifiers differ considerably from those employed with operational amplifiers. As a result, the gated-amplifier characteristics listed below must be improved beyond those normally required with operational amplifiers:

1. The maximum output current of most operational-amplifier designs is less than 20 mA. Gated amplifiers are often used in sampling circuits where large capacitors must be charged. In order to permit rapid charging it is necessary to design the gated amplifier to supply output currents in excess of 100 mA.

2. The gated amplifier must be designed for low power consumption in the ON state, since any ON-state power reduction is reflected by lower system average power requirements.

3. The feedback ratios and loads connected to the gated amplifier vary widely in different applications. In order to optimize performance under these varying conditions it is necessary to modify the open-loop transfer function of the gated amplifier. Furthermore, large capacitors can not be used for control since they would deteriorate gating.

The gating feature introduces certain additional design constraints that have no parallel in operational-amplifier design. The most obvious is that provision for gating must be included in the design. Other required characteristics are:

1. Turn-on time (the time required for the amplifier to become active following application of an ON pulse) should be low. While delayed turn ON normally does not introduce errors, it limits the maximum rate of sampling operations.

2. Turn OFF is essentially an instantaneous process, and any attempt to define turn-off time precisely is meaningless. The important parameter is the net charge which leaves the

three available amplifier terminals during the turn-off process. This quantity is defined as the integral of the current leaving a particular terminal over the 1-μs interval immediately following turn OFF. Any net charge leads to errors in applications where capacitive data storage is used.

3. The leakage current at any of the three available terminals should be low with the amplifier OFF to minimize the rate of decay of voltages stored on capacitors connected to these terminals.

The design of the gated amplifier typifies most design problems in that performance characteristics are interrelated and ultimately limited by device capabilities. Numerous engineering compromises are required during the design procedure and these compromises are discussed in subsequent sections.

B. THE BASIC DESIGN APPROACH

The design of the gated amplifier is initiated with the design of a basic operational amplifier. This approach is used because of the paramount importance of ON-state characteristics. Inclusion of a few additional components permits gating of the basic amplifier. The design approach outlined in this section differs from that normally used for operational amplifiers because improved performance characteristics are necessary for the gated amplifier.

A common feature of all operational amplifiers, including the gated amplifier, is high open-loop gain. A significant advantage exists if most of this gain is obtained in one stage. A high-gain stage will normally have a dominant pole in its transfer function, and other singularities will be located at much higher frequencies. If a single high-gain stage is combined with low-gain stages (which usually have all singularities located at high frequencies), the transfer function of the resultant amplifier is approximately first order. This type of transfer function is ideally suited to feedback applications. Furthermore, if the high-gain stage provides inversion, local capacitive feedback can be used to change the location of the dominant pole and thus to optimize performance for different operating conditions.

Various approaches can be used for the design of high-gain stages. For example, local positive feedback can increase the gain of an amplifying stage. Most designs for high-gain stages are unacceptable for use as part of the gated amplifier, however, because of complexity, high power consumption, low input impedance which complicates the design of the preceding stage, or poor gain or operating-point stability.

A cascode amplifier (a grounded-emitter transistor driving a grounded-base transistor) can be used to provide high voltage gain if the high incremental resistance of a current source is used as a load. This circuit is ideal for use as the high-gain stage in a gated-amplifier for the following reasons:

1. The cascode amplifier minimizes input capacitance.
2. This connection yields higher bandwidth than any other known circuit that provides the same gain and dynamic range, and requires the same power.
3. The gain of the stage is more stable than that of stages using positive feedback.
4. The operating point is constrained by the current source and can therefore be made very stable.
5. The cascode circuit inverts and local capacitive feedback provides excellent control of its transfer function.

In order to minimize the complexity of the gated amplifier and to maintain high bandwidth, it is advantageous to use a single amplifying stage between the input terminals of the gated amplifier and the input of the cascode circuit. Intended applications dictate that the gated amplifier incorporate a differential input with low voltage drift and high common-mode rejection ratio. The differential-amplifier connection is a natural choice for the input circuit of the gated amplifier since it combines the features mentioned above.

The output resistance of the cascode amplifier is high because a current source is used as the load resistance and the output current capability of this circuit is limited because of low operating current levels. It is necessary to isolate the output of the cascode amplifier

from loads that are applied to the output of the gated amplifier with a buffer amplifier. The buffer amplifier is the only part of the gated amplifier that provides high currents, and care must be taken in its design so that buffer-amplifier power requirements do not predominate in the gated-amplifier circuit.

Several stages were investigated; as a result a two-stage Class-B emitter follower which incorporates a novel biasing technique was selected for use as a buffer. This stage combines excellent isolation with low power requirements. A nonlinear operating mode is included so that peak output currents more than three orders of magnitude above the quiescent level are possible.

The basic operational amplifier formed by the combination of the three circuits — differential amplifier, cascode amplifier, and Class-B emitter follower — can be easily gated. Compensation for input current and voltage drift is possible, and the inclusion of compensating components completes the basic structure of the gated amplifier.

C. A TRANSISTOR MODEL

As a preliminary to the discussion of the various circuits, a linear transistor model is introduced in this section. The model is shown in Fig. 2-1 and this model is used for the analysis of all circuits. The T model is used in preference to equivalent hybrid-π or other models since it permits a more straightforward analysis of grounded-base and emitter-follower connections.

The base resistance often included in a transistor model is omitted in Fig. 2-1. This simplification is valid for all intended applications of the model since all the transistors used in the gated-amplifier circuit operate at quiescent current levels under 0.5 mA. As a result the base resistance is always less than 10 percent of the emitter resistance r_e, and it can be shown that this ratio eliminates the effects of base resistance in the circuits used.

D. THE DIFFERENTIAL AMPLIFIER

A simplified schematic of a differential amplifier which is suitable for linear-region analysis is shown in Fig. 2-2.* Note that a resistor with magnitude $2r_e$ (where r_e is the emitter resistance of Q_1 or Q_2) is included in the circuit. This element is not inherent to the design of a differential amplifier, but is included to represent the effects of two diodes which must be added to a differential-amplifier circuit used as part of a gated amplifier. The necessity for these elements is explained later.

Several assumptions which are valid for all intended applications are introduced:

1. Transistors Q_1 and Q_2 are identical.
2. The total resistance between the emitters of Q_1 and Q_2 is exactly twice the emitter resistance of either transistor.
3. The load impedance connected to the collector of Q_2 is small enough so that the voltage gain from the base to the collector multiplied by μ is much less than unity. It is thus possible to assume that $\mu = 0$.
4. The grounded-emitter current gain, β, is defined as $\frac{\alpha}{1-\alpha}$. Since β is large, it is assumed that $\beta+1 \approx \beta$.

Substitution of the transistor model of Fig. 2-1 into the differential-amplifier circuit of Fig. 2-2 results in a circuit which can be reduced to the equivalent circuit shown in Fig. 2-3. Since reduction is straightforward the steps are left to the reader.

One further simplification of the differential-amplifier model is normally used in the analysis of the gated amplifier and is included here for completeness. In usual applications, feedback around the amplifier is applied only to the base of Q_1 in Fig. 2-2 since this input is the negative-gain terminal of the complete amplifier. The base of Q_2 is either grounded or connected to a low impedance

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*The lower-case letters i and e denote incremental currents and voltages respectively in this chapter. Unless stated otherwise these variables are functions of the complex frequency s. Capital I denotes quiescent current.

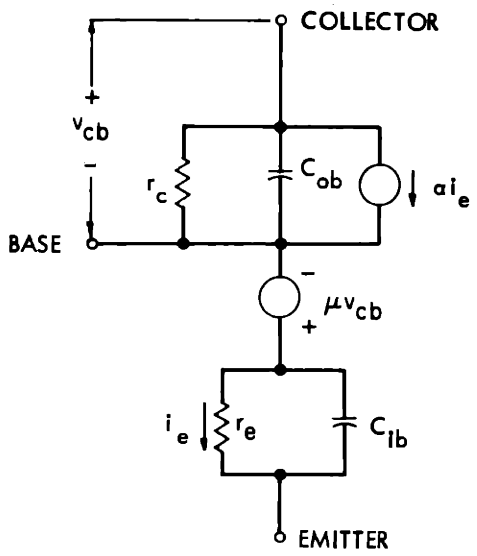


Fig. 2-1 Linear-Region Transistor Model

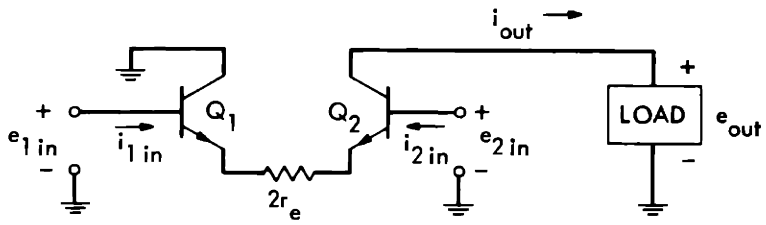


Fig. 2-2 Differential Amplifier with Emitter Degeneration (Bias not shown)

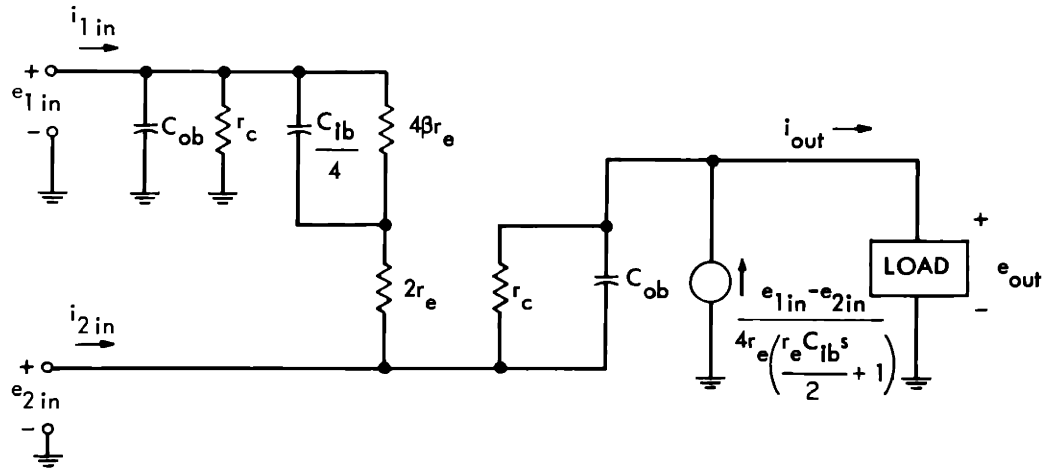


Fig. 2-3 Equivalent-Circuit Model for the Differential Amplifier

source which may be considered an incremental (or a-c) ground.

If the base of Q_2 in Fig. 2-2 is incrementally grounded (corresponding to grounding the e_2 input in Fig. 2-3), the circuit is unilateral so that the input impedance is independent of gain. Furthermore, the capacitor C_{ob} and resistor r_c connecting the e_2 input to the output can be included as part of the load impedance.

E. APPROXIMATE ANALYSIS OF THE CASCODE AMPLIFIER

The second major circuit of the gated amplifier is the cascode amplifier shown in simplified form in Fig. 2-4. Since a detailed analysis of this circuit is fairly complex and since such an analysis may be important only to readers interested in making circuit modifications in order to satisfy particular requirements, the detailed version is deferred until the next section.

The complete analysis shows that a cascode amplifier can be represented by the equivalent-circuit model shown in Fig. 2-5, and this model is used in all further analyses of circuits which include the cascode amplifier. Note that i_{out} has been redefined in this figure compared with Fig. 2-4 so that the output impedance of Q_2 can be easily combined with the load. It can be shown that this model is at least reasonable without a detailed analysis, and this is done in the following paragraphs.

The input impedance to the amplifier is the impedance seen at the base of the grounded-emitter transistor Q_1 in Fig. 2-4. The resistive component of the input impedance is simply the grounded-emitter input resistance βr_e. The reactive component consists of two capacitors in parallel. The base-to-emitter capacitance, C_{ib}, appears directly. Miller effect multiplies the component attributable to C_{ob} by a factor of two, since at frequencies where the input capacitance is important, the voltage gain of transistor Q_1 is -1. The output current is effectively equal to the current in the emitter resistance of Q_1, and the grounded-base output impedance of Q_2 is the output impedance of the cascode amplifier. It is shown in the next section that this intuitive development is valid to frequencies approaching the transistor gain-bandwidth product ω_T.

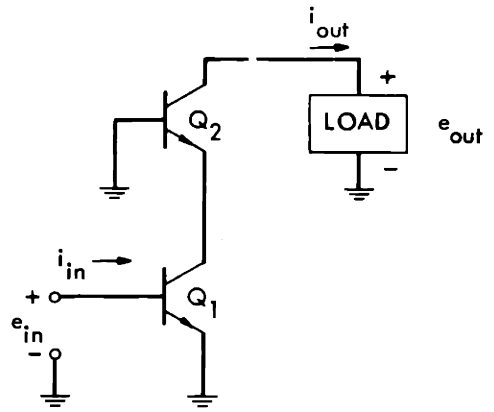


Fig. 2-4 Cascode Amplifier (Bias not shown)

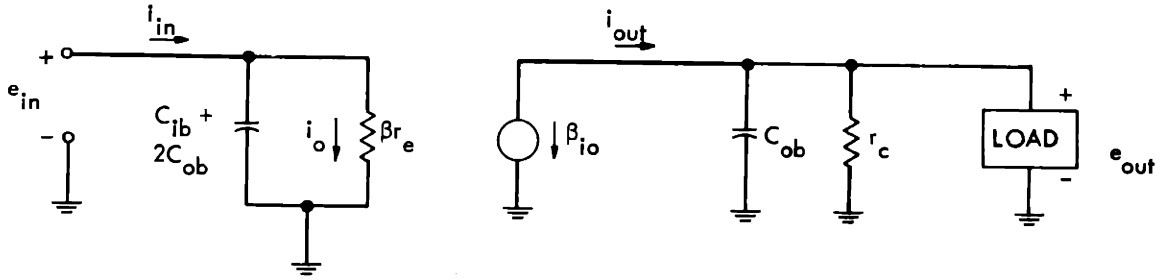


Fig. 2-5 Simplified Equivalent Ciruit for the Cascode Amplifier

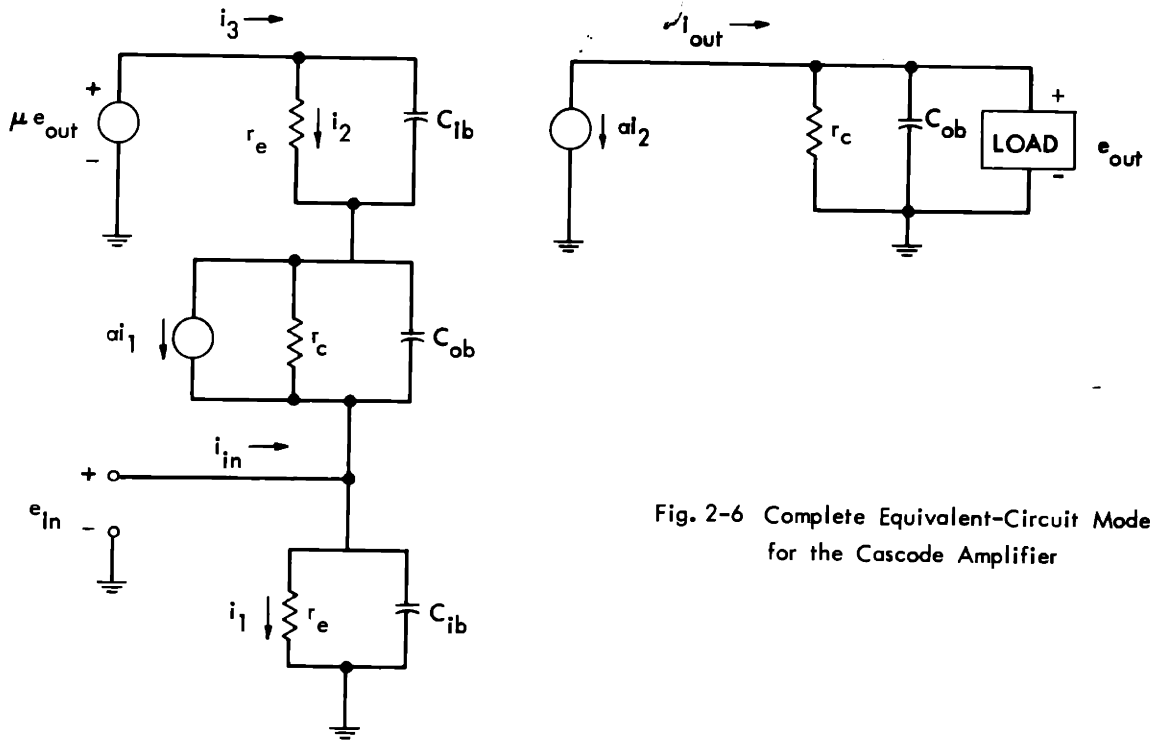


Fig. 2-6 Complete Equivalent-Circuit Model for the Cascode Amplifier

The question can be raised as to whether the reverse (or μ) generators of the two transistors change the results significantly in view of the extremely high gains obtained from the cascode amplifier. Most of the gain is obtained across the grounded-base section, and therefore only the μ generator of Q_2 (Fig. 2-4) need be considered. At low frequencies it is evident that this generator does not alter the results since it appears in series with a current source. At high frequencies the gain of the stage is reduced by the capacitive portion of the output impedance, and this minimizes the effect of the μ generator.

F. DETAILED ANALYSIS OF THE CASCODE AMPLIFIER

This section shows that the simplified equivalent circuit model of Fig. 2-5 accurately represents the relationships that exist among the terminal voltages and currents of the cascode amplifier.

A detailed equivalent circuit for the cascode amplifier is shown in Fig. 2-6. This model is derived from the cascode circuit of Fig. 2-4 with the aid of the transistor model (Fig. 2-1) and the following assumptions:

1. Both transistors in Fig. 2-4 are identical.
2. Since the voltage gain of Q_1 is low, it is possible to assume that $\mu = 0$ for this transistor. The reverse generator of Q_2 is retained.

It is convenient to define the following quantities:

$$Z_e = r_e \parallel sC_{ib} = \frac{r_e}{r_e C_{ib} s + 1}$$

$$Z_c = r_c \parallel sC_{ob} = \frac{r_c}{r_c C_{ob} s + 1}$$

$$\tau_e = r_e C_{ib}$$

$$\tau_c = r_c C_{ob}$$

Also, following convention, let

$$\frac{1}{\omega_T} = r_e(C_{ob} + C_{ib}) ,$$

where ω_T is the gain-bandwidth product of the transistor.

Through use of the variables i_1, i_2, and i_3 shown in Fig. 2-6, it is possible to write the following set of equations:

$$i_1 = \frac{e_{in}}{r_e}$$

$$i_2 = i_3 \frac{Z_e}{r_e}$$

$$i_{in} = \frac{e_{in}}{Z_e} - i_3$$

$$i_3 = \frac{1}{Z_e + Z_c}\left[\mu e_{out} + e_{in}\left(\frac{\alpha Z_c}{r_e} - 1\right)\right]$$

$$i_{out} = \frac{-\alpha i_3 Z_e}{r_e}$$

In order to reduce the circuit to form shown in Fig. 2-5, it is necessary to show that the remaining μ generator in Fig. 2-6 can be ignored, since this will eliminate the dependence of the input impedance on the load. It is evident that the nature of the load causes variations in the effect of the μ generator, since the load determines the magnitude of e_{out} for a given e_{in}. However, the way the cascode circuit is used in a gated amplifier precludes an inductive load. Thus, at any frequency, the magnitude of the load applied to the current generator of transistor Q_2 must be less than or equal to the magnitude of Z_c. (In practice, the maximum magnitude of the load connected to the cascode is approximately $\frac{Z_c}{3}$.) Since the maximum load impedance will result in maximum gain, and hence maximum effect of the μ generator, the cascode circuit is investigated for the case where the load shown in Fig. 2-6 is an open circuit. This results in one further equation, $e_{out} = Z_c i_{out}$.

Solving these equations for i_{in} and i_{out} as functions of e_{in} yields

$$y_{in} \triangleq \frac{i_{in}}{e_{in}} = \frac{1}{Z_e} - \frac{\left(\frac{\alpha Z_c}{r_e} - 1\right)\left(\frac{1}{Z_e+Z_c}\right)}{1 + \frac{\mu\alpha Z_e Z_c}{r_e(Z_e+Z_c)}}$$

$$y_{tr} \triangleq \frac{i_{out}}{e_{in}} = - \frac{\left(\frac{\alpha Z_c}{r_e} - 1\right)\left(\frac{\alpha Z_e}{r_e(Z_e+Z_c)}\right)}{1 + \frac{\mu\alpha Z_e Z_c}{r_e(Z_e+Z_c)}}$$

Consider the term $\frac{\mu\alpha Z_e Z_c}{r_e(Z_e+Z_c)}$, which is the only term that contains μ. From the definitions introduced earlier it is clear that at all frequencies

$$\left| \frac{Z_e}{r_e} \right| \leq 1 \quad \text{and} \quad \left| \frac{Z_c}{Z_e+Z_c} \right| \leq 1$$

The quantity α must be less than 1 for any transistor. Therefore,

$$\left| \frac{\mu\alpha Z_e Z_c}{r_e(Z_e+Z_c)} \right| \leq \mu$$

Since the magnitude of μ is typically 10^{-3} to 10^{-4}, it is possible to drop the terms containing μ because they are small compared to 1. Therefore, the equations for the input admittance and the transadmittance can be simplified as

$$y_{in} = \frac{1}{Z_e} - \left(\frac{\alpha Z_c}{r_e} - 1\right)\left(\frac{1}{Z_e+Z_c}\right)$$

and

$$y_{tr} = -\left(\frac{\alpha Z_c}{r_e} - 1\right)\left(\frac{\alpha Z_e}{r_e(Z_e+Z_c)}\right)$$

Through use of the relationships that $\frac{r_c}{r_e} >> 1$ (this ratio is typically on the order of 10^5) and that $\alpha \approx 1$ except in cases where a term such as $1-\alpha$ appears, the input admittance expression becomes

$$y_{in} \approx \frac{\frac{\beta}{r_c}(2r_e\tau_c\tau_e + r_c\tau_e^2)s^2 + \frac{\beta}{r_c}(2r_e\tau_c + r_c\tau_e)s + 1}{\beta r_e\left[\left(\frac{r_e\tau_c + r_c\tau_e}{r_c}\right)s + 1\right]}$$

Provided β is greater than 10 (certainly a realistic assumption for any high-quality transistor), the expression can be factored as

$$y_{in} = \frac{\left[\frac{\beta}{r_c}(2r_e\tau_c + r_c\tau_e)s + 1\right]\left[\tau_e s + 1\right]}{\frac{\beta r_e(r_e\tau_c + r_c\tau_e)}{r_c}s + 1}$$

Through use of the original definitions of τ_e and τ_c, this expression becomes

$$y_{in} = \frac{\left[\beta r_e(2C_{ob} + C_{ib})s + 1\right]\left[r_e C_{ib}\, s + 1\right]}{\beta r_e\left[r_e(C_{ob} + C_{ib})s + 1\right]}$$

The two high-frequency singularities in this expression are located close to each other since C_{ob} is normally less than C_{ib}. Fortunately a closely spaced pole-zero doublet has small effect on a transfer function, and furthermore, these singularities are located at frequencies equal to or above ω_T. The amplifier is never operated at these frequencies. It should be noted that the entire modeling process is somewhat academic at frequencies close to ω_T because of inherent limitations of the transistor model. Accordingly, with the two high-frequency singularities omitted, y_{in} becomes

$$y_{in} = \frac{\beta r_e(C_{ib} + 2C_{ob})s + 1}{\beta r_e}$$

which indicates that the cascode input circuit can be modeled as a resistor βr_e in parallel with a capacitor $C_{ib} + 2C_{ob}$.

The same type of reduction is applied to the cascode circuit trans-admittance expression with the final result that

$$y_{tr} \approx \frac{1 - r_e C_{ob} s}{r_e\left(\frac{s}{\omega_T} + 1\right)}$$

The two singularities appearing in this expression are located at or above ω_T. However, both contribute negative phase shift at all frequencies. These singularities are temporarily ignored, and an approximate method to include the effects of the phase shift will be introduced later in the development. Subject to this restriction, a cascode amplifier model can be drawn as shown in Fig. 2-5.

G. BUFFER AMPLIFIER

The cascode amplifier as used in the gated amplifier is loaded with a current source so that this circuit provides most of the voltage gain of the gated amplifier. It is necessary to isolate the high-impedance node at the output of the cascode amplifier from loads which may be connected to the gated amplifier by means of a buffer amplifier. While it is not necessary for the buffer amplifier to provide voltage gain greater than unity, two stringent requirements are placed on this amplifier by intended gated-amplifier applications:

1. The bandwidth inherent with the cascode and differential amplifiers should not be impaired by the buffer stage, at least in the absence of load. With large capacitive loads, some bandwidth compromises must be made in order to minimize power consumption.

2. The buffer amplifier must operate at low quiescent current levels to maintain low power dissipation, yet must deliver extremely high peak currents to permit rapid capacitor charging when required in a specific application. Typical values for the quiescent and peak current levels in the final circuit are 100 μA and 400 mA respectively.

The circuit developed for use as a buffer amplifier is basically a two-stage emitter follower where the second stage consists of a push-pull or complementary Class-B emitter-follower pair to provide high output current capability, while maintaining low quiescent current drain. A simplified diagram of this circuit, suitable for linear-region analysis, is shown in Fig. 2-7.

Several novel features of the buffer-amplifier circuit which result in further power economy are not included in this schematic diagram. These features are explained later in the chapter.

Two relationships among component values are required to show clearly the basic operation of this circuit. Resistor r_1 represents the collector-to-base resistance of the transistor used as a load for the cascode amplifier, and this resistance is several orders of magnitude larger than r_2. Also, resistor r_3 is approximately an order of magnitude larger than $4r_{e1}$. Therefore, the main amplifying path is from the input to the base of Q_1 through r_2 and then to the bases of the output transistors.

The relationship between circuit element values, particularly the relationship between the resistors connected to the emitters of Q_1, Q_2, and Q_3 and the emitter resistance of the particular transistor is a consequence of including a number of diodes in the buffer-amplifier circuit. The reason for including these diodes is outlined in a subsequent section.

Two circuit relationships, the input impedance $\frac{e_{in}}{i_{in}}$ and the gain $\frac{e_{out}}{e_{in}}$, are required. In contrast to the differential and cascode amplifiers which are unilateral, both of these quantities depend on the load connected to the buffer amplifier.

The transistor model can be substituted into the circuit to yield the equivalent-circuit model shown in Fig. 2-8. The assumptions used in this transformation are that the transistor reverse generators can be neglected (since the voltage gain of an emitter follower is always less than unity), and that transistors Q_2 and Q_3 are identical.

A complete analysis of this circuit was conducted during the research, and the results of this analysis have been used to verify the

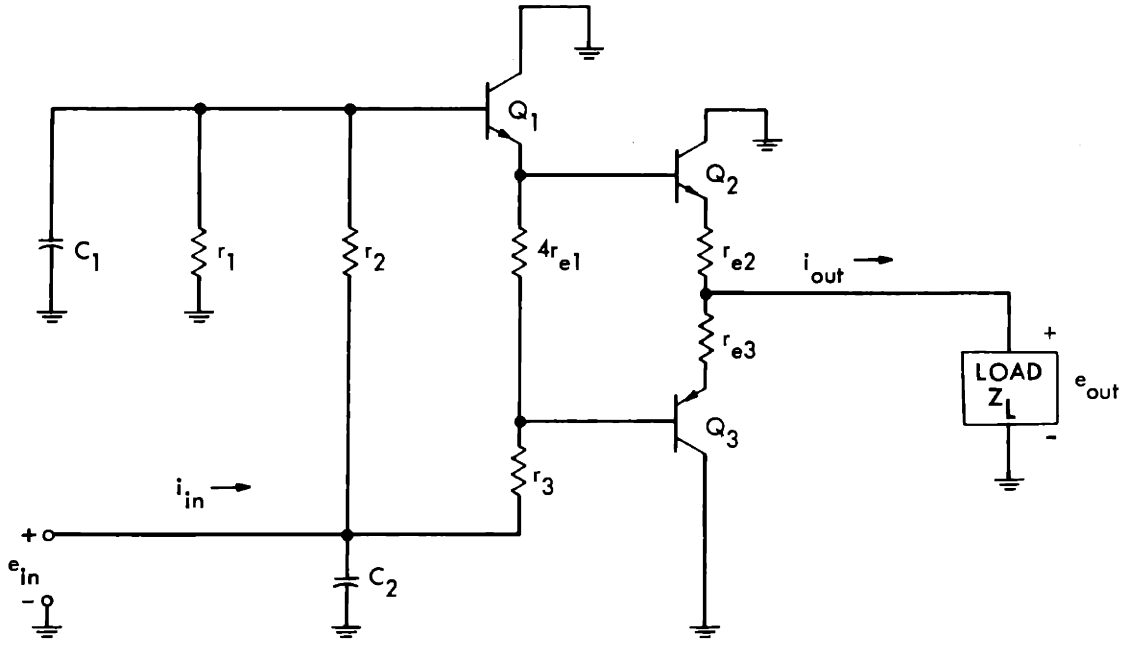


Fig. 2-7 Buffer-Amplifier Circuit Diagram

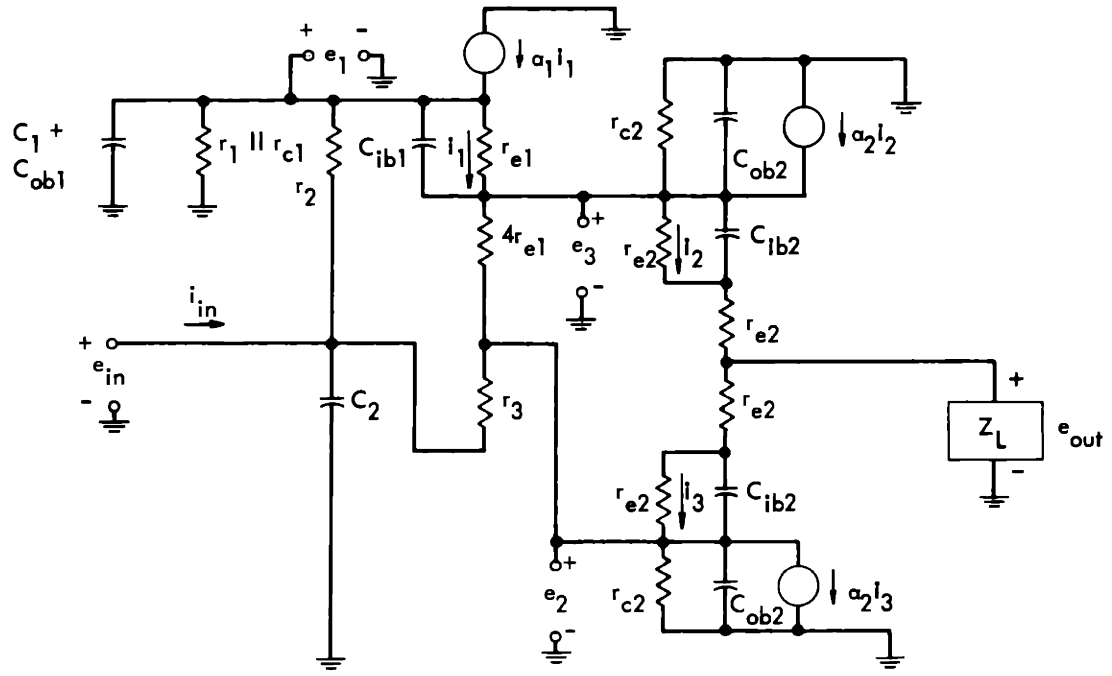


Fig. 2-8 Complete Equivalent-Circuit Model for the Buffer Amplifier

approximate analysis presented in the following two sections. The generalized analyses is omitted for several reasons. The buffer amplifier, in contrast to the differential amplifier and cascode amplifier, is not a general-purpose circuit. Hence, the relationships among various element values are closely constrained, and altering these relationships by any large amount renders the circuit useless. Also, the relationships are complex and as a result all insight into the operation of the circuit is lost in the mathematics. Finally, all buffer amplifier loads used in the course of the research fall into two broad categories. The amplifier is either loaded with a high impedance (greater than 5 K shunted by a small capacitor) or a large capacitor (greater than 0.05 μF) in series with a resistor on the order of 1Ω. Limiting the loads to these types and restricting the range of parameter variation to realistic values permits a significantly simplified analysis which maintains insight. The two loading conditions are considered separately in the following two sections.

H. BUFFER AMPLIFIER WITH HIGH-IMPEDANCE LOAD

The buffer amplifier with high-impedance load can be approximately modeled as shown in Fig. 2-9. A "hybrid" model that combines circuit elements with an idealized transfer-function section results in the most useful model in this case. This model is derived by inspection from Fig. 2-8.

The low-frequency gain of the circuit must be close to unity because all shunt resistors to ground (r_1, r_{c1}, r_{c2}) are large compared to resistors in the forward-gain path (r_2, r_{e1}). The input resistance includes three parallel components. These are resistors r_1 and r_{c1}, plus a resistor that represents r_{c2} multiplied by the current gain from the amplifier input to the bases of transistors Q_2 and Q_3. A d-c analysis yields a multiplying factor equal to $\frac{r_3}{6\, r_{e1}}$.

Capacitor C_2 appears directly to ground at the input of the amplifier. Resistor r_2 is approximately a factor of three smaller than resistor r_3. Also, the capacitance at the node labelled e_1 in Fig. 2-8 is essentially equal to $C_1 + C_{ob1}$ because the gain of Q_1 minimizes the effects of other circuit capacitance reflected to this node. Therefore,

the network representing the input impedance of the amplifier can be completed with the series connection of r_2 and $C_{ob1} + C_1$.

The transfer function of the ideal element shown in Fig. 2-9 is determined from a consideration of circuit singularities. In the absence of load, the output voltage is equal to $\frac{e_2+e_3}{2}$ because of the symmetry of the output circuit. Furthermore, r_{e2} can be considered infinite when calculating e_2 and e_3 since r_{e2} multiplied by the current gain of Q_2 is large compared to r_{e1}.

Reference to Fig. 2-8 shows that this simplification and the relationship $r_3 >> r_{e1}$ yield

$$e_3 \approx \frac{e_{in}}{[(C_{ob1} + C_1)r_1 s+1][r_{e1}C_{ob2}s+1]}$$

$$e_2 \approx [e_3 + \frac{4r_{e1}}{r_3} e_{in}] [\frac{1}{4r_{e1}C_{ob2}s+1}]$$

Combining these equations and dropping insignificant terms shows that

$$e_{out} = \frac{e_2+e_3}{2} \approx$$

$$\frac{e_{in}[2r_{e1}C_{ob2}s+1][\frac{r_{e1}r_2(C_{ob1}+C_1)s}{r_3}+1]}{[r_2(C_{ob1}+C_1)s+1][4r_{e1}C_{ob2}s+1][r_{e1}C_{ob2}s+1]}$$

The buffer-amplifier output impedance is required to complete the analysis in the case of high load impedance. In this case the output impedance is small enough so that the loading can be neglected at low frequencies. There is, however, the possibility of one additional pole from capacitve loading. This pole location can be obtained from the high-frequency output impedance of the circuit shown in Fig. 2-8 which is approximately r_{e2} at any frequency where a small load capacitance could contribute a pole. The output resistor r_{e2} completes the model for the buffer amplifier with high-impedance load shown in Fig. 2-9.

I. BUFFER AMPLIFIER WITH LARGE CAPACITIVE LOAD

Large capacitive loads reduce the bandwidth of the gated amplifier to relatively low frequencies compared with the unloaded case. As a result, the gain of the transistors used in the buffer amplifier can be considered constant and equal to the d-c value. Furthermore, the collector-to-base capacitance of transistors Q_2 and Q_3 (Fig. 2-7) can be eliminated from the model. These conditions allow a significant simplification of Fig. 2-8, since a d-c transistor model can be substituted for the more complex model.

One possible simplification, obtained by reflecting the emitter-circuit impedance of a particular transistor to the base circuit through multiplication by the transistor current gain, is shown in Fig. 2-10. To obtain this model the capacitance $C_1 + C_{obl}$ is combined with C_2 at the input to the circuit. This is permissible since the model will be used only at frequencies lower than $\frac{1}{r_2(C_1 + C_{obl})}$. Note that while this transformation retains voltage relationships, various currents in the circuit are altered, and i'_{in} must be calculated from the relationship $i'_{in} = \frac{e_{in}-e_1}{r_2} + \frac{e_{in}-e_2}{r_3}$, rather than directly from Fig. 2-10.

Use of the relationships $r_{e1} \ll r_3$, $\beta r_{e1} > r_2$ and $r_3 > r_2$ permit further simplification as shown in Fig. 2-11. This model is used for all further analysis involving large capacitive loads.

J. THE BASIC OPERATIONAL AMPLIFIER

The three circuits—differential amplifier, cascode amplifier and a particular form of buffer amplifier—which are used as building blocks for the basic operational amplifier have been presented in preceding sections of this chapter. The basic operational amplifier is, of course, designed with consideration for its intended use as a gated amplifier.

This section illustrates the implementation of these circuits and the way they are interconnected to form the basic operational amplifier. The numerous techniques necessary to convert the simplified designs presented earlier to practical circuits are included.

The basic operational-amplifier schematic diagram is shown in Fig. 2-12. (The transistor and diode numbering sequence shown in

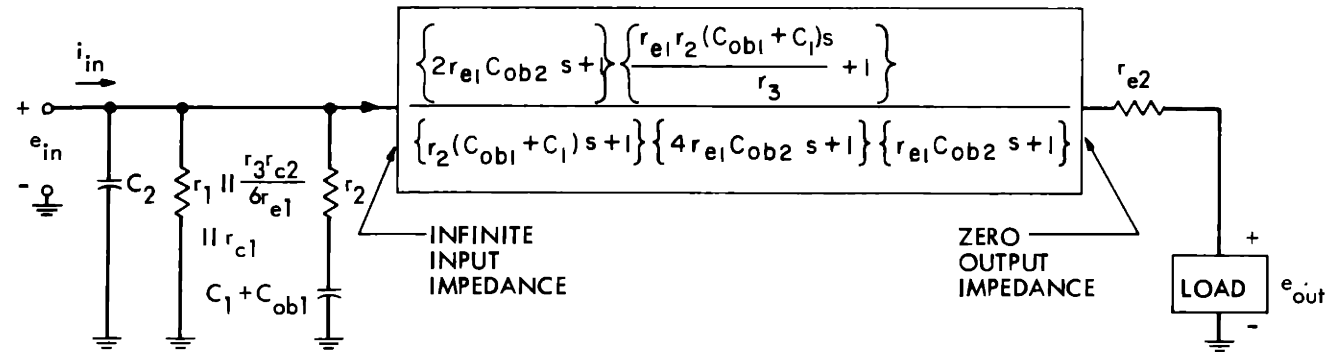


Fig. 2-9 Final Buffer-Amplifier Model for the Case of High-Impedance Load

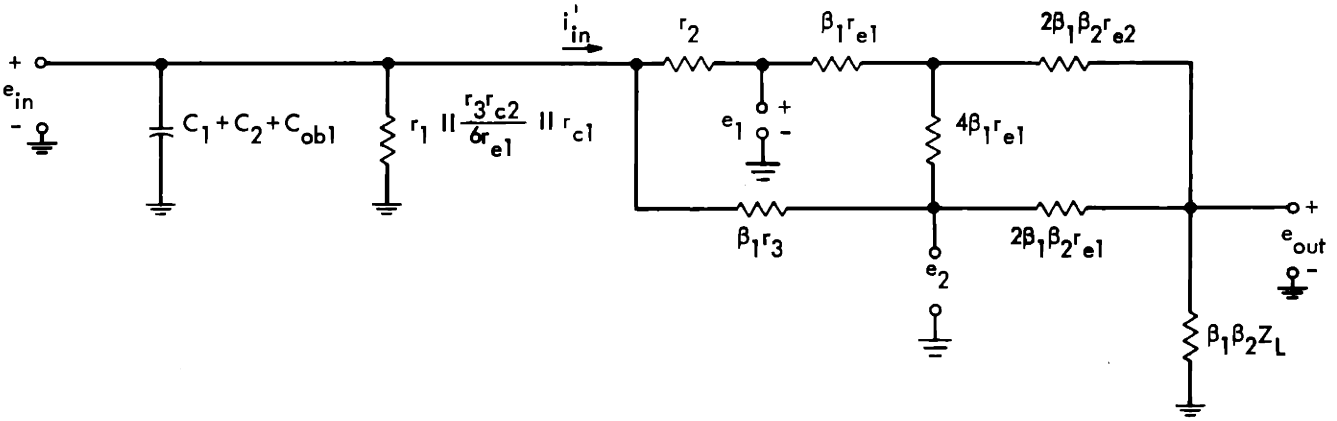


Fig. 2-10 Complete Buffer-Amplifier Equivalent Circuit for Large Capactive Load

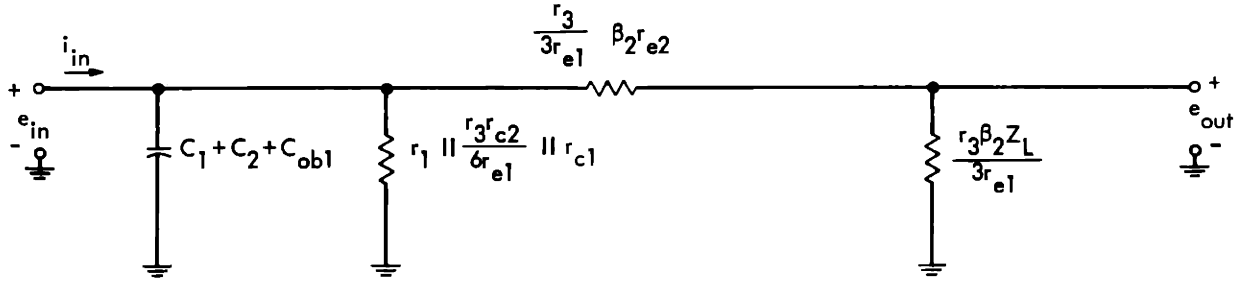


Fig. 2-11 Simplified Buffer-Amplifier Model for Large Capacitive Load

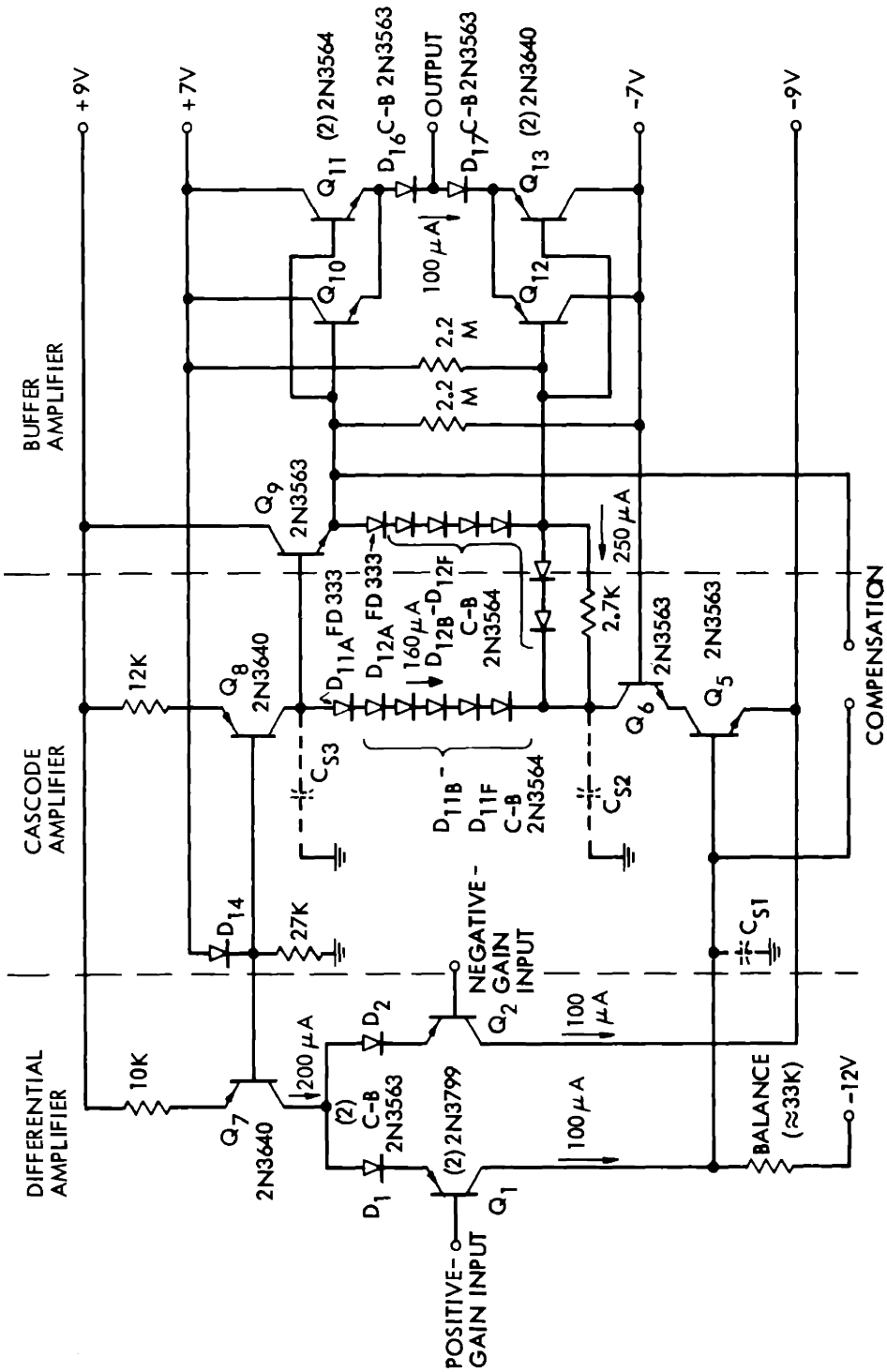


Fig. 2-12 Basic Operational Amplifier

Fig. 2-12 is chosen for convenience in adding components as the design progresses, and will seem unusual until the design is completed.) Important quiescent current levels are indicated in this diagram.

The supply voltages are chosen to permit an output-signal range of ±4 volts and to allow sufficient quiescent voltage across bias resistors to insure stability of operating points with temperature variation. The rather unusual approach of using five supply voltages permits a design with lower power consumption than if fewer voltages are used and simplifies the gated-amplifier circuit. While the power supply becomes more complex, only one multiple-voltage power supply is required in any system, and the increase in its complexity is justifiable in light of improved amplifier performance.

The maximum output voltage of ±4 volts compares with a customary value of ±10 volts for most commercially-available solid-state operational amplifiers. While the reduced output of the gated amplifier leads to larger percentage errors from voltage drift and noise, it permits operation at a reduced power level. This is one of the many design compromises made in order to minimize power consumption.

The differential amplifier consists of transistors Q_1 and Q_2 which are operated from a constant current source Q_7. The constant-current source is used to control operating point and to insure high common-mode rejection. Diodes D_1 and D_2 are included to prevent breakdown of the base-to-emitter junctions of Q_1 and Q_2 when the circuit is in the OFF state. The need for these elements, as well as several other circuit components which are included to permit gating, is demonstrated as the design progresses.

Transistor Q_7 operates at a collector-current level of 200 μA. The sum of the base-to-emitter voltage of Q_1 and the forward voltage of D_1 is matched to that of Q_2 and D_2. Therefore, Q_1 and Q_2 operate at approximately 100 μA when the amplifier is balanced. The 100-μA quiescent-current level represents a compromise between improved gain and bandwidth at higher currents and lower power consumption, drift, and input current at lower levels.

Amplifier balance is accomplished by varying the collector load resistor of Q_1, so that at balance the sum of the voltages across the

base-to-emitter junction of Q_1 and diode D_1 is equal to the sum of those of Q_2 and D_2 despite slight mismatches in these components. Hoffait and Thornton[6] have shown that this type of balancing is extremely effective in minimizing voltage drift in a differential pair. A parallel argument can be used to show that the same approach should work with diodes included in series with the transistor emitters, and this has been experimentally verified. As a consequence of this balancing technique, most of the drift referred to the input for the complete amplifier can be traced to changes in the operating point of Q_5 with temperature.

The choice of type 2N3799 transistors for the differential pair was dictated by two considerations. It is advantageous to use NPN types in the cascode amplifier because of their inherently better high-frequency performance, since the cascode amplifier is the most important part of the amplifier from the point of view of maintaining high frequency response. If NPN types are used in the cascode, PNP types are required in the differential amplifier. The second consideration is that high current gain is required to minimize input current. The 2N3799 is one of the highest-gain PNP types available, with a typical β of 400 at 100 μA of collector current.

The cascode amplifier consists of two 2N3563 transistors, Q_5 and Q_6. The 2N3563 was selected since it has extremely low junction capacitances, a necessary condition to maximize frequency response. Three capacitances to ground, C_{S1}, C_{S2}, and C_{S3} are indicated with dashed lined in the cascode amplifier. These capacitances are included to represent the effects of stray capacitances that cannot be ignored in this section of the amplifier. Capacitance C_{S1} represents the capacitance distributed to ground (other than transistor capacitance) at the node including the base of Q_5. In the complete amplifier this node has several connections made to it, so that the shunt capacitance to ground is relatively high. The approximate value of C_{S1} is 7 pF.

Capacitance C_{S2} has two major components. One of these is conductor-to-ground capacitance. The other is one half of the total capacitance distributed between the diode chain D_{11A} - D_{11F} and ground. The other half of this distributed capacitance is lumped with the capacitance of a

reverse-biased diode which is required for gating but not shown in Fig. 2-12, and the sum appears as the shunt capacitance C_{S3}. Capacitors C_{S2} and C_{S3} both have an approximate value of 4 pF.

The cascode transistors are operated at a collector-current level of 400 μA, a value which results from a compromise between frequency response and power requirements.

Transistor Q_8 is used as a current source operating at a quiescent level of 160 μA. This current source provides a very high load resistance for the cascode amplifier in order to maintain high unloaded d-c open-loop gain.

The buffer amplifier consists of transistors Q_9 through Q_{13} plus 14 diodes. The somewhat unusual arrangement maintains low quiescent power consumption and simultaneously provides the capability to supply high peak output current.

The output complementary emitter follower consists of Q_{10} and Q_{11} in parallel as the NPN, with Q_{12} and Q_{13} as the PNP. The parallel connection is used to maintain β at higher current levels than would be the case if single transistors were used. While the buffer-amplifier analysis developed earlier in this chapter assumed single output transistors, the analysis remains valid, since the parallel connection can be considered as a single transistor with twice the value of capacitors C_{ob} and C_{ib} and half the value of resistors r_e and r_c of either individual transistor.

Transistors Q_{10} - Q_{13} operate at approximately 50 μA of collector current each, resulting in a total quiescent current consumption of 100 μA for these transistors. Diodes D_{16} and D_{17} are necessary to maintain low output current when the amplifier is in the OFF state.

The quiescent voltage appearing between the bases of Q_{10} and Q_{12} is 2.5 volts at normal operating levels. This bias voltage is supplied by the forward-biased voltages of diodes D_{12A} -D_{12D}. Normally this is considered a somewhat unstable method of operating-point control because base-to-emitter voltage, rather than emitter current, is constrained. Small changes in diode voltages can lead to large changes in operating currents because of the exponential relationship between current and voltage. In practice, however, control of the output-transistor quiescent current level has proved to be an insignificant

problem. The transistor junctions used in this part of the circuit (note that the diodes are also transistor junctions) display an amazing uniformity, with the result that even without selection, variations in quiescent current from amplifier to amplifier or with temperature would be less than 2 to 1. Very simple selection procedures (which basically consist of eliminating the extremes of the distribution) reduce the variations to less than 1.5 to 1.

Transistor Q_9 is used as an emitter follower which is biased in a novel way. The diode chain D_{11A} - D_{11F} establishes a bias potential of 6 diode voltages, while the base-to-emitter junction of Q_9 and diodes D_{12A} - D_{12D} produce a potential of 5 diode voltages. The difference between the voltages of these two chains, approximately 600 mV, appears across the 2.7-K resistor located in the emitter circuit of Q_9, and produces a current of approximately 250 μA through this resistor. Diodes D_{12E} and D_{12F} are each forward biased by only 300 mV and consequently conduct a current of less than 0.1 μA. These two diodes are included to increase output current capability and are discussed later.

The collector current for Q_6 is the sum of the collector current of Q_8 and the current through the 2.7-K resistor, and now the reason for this particular form of biasing becomes apparent. All of the collector current of Q_9 also flows through Q_6. This reduces the current load on both 9-volt supplies by 250 μA compared with a conventional biasing technique where the collector current of Q_9 is returned to the -9 volt supply through a resistor or current source. The resultant power reduction of 4.5 mW represents approximately 25 percent of the quiescent power consumption of the amplifier.

The two 2.2-M resistors incorporated in the buffer amplifier are elements necessary for gating and are paralleled with the collector resistances of Q_{10} and Q_{12} for purposes of analysis. Two terminals labelled compensation are included to allow modification of the open-loop transfer function of the amplifier and are discussed in following sections.

A very common gated-amplifier application involves rapid charging of large capacitive loads, and therefore high output current is mandatory.

The buffer amplifier supplies high output current in a nonlinear mode as follows. Consider a large positive input signal to the base of Q_1. This signal turns off Q_1, back biases the base-to-emitter junction of Q_5, and reduces the collector current of Q_6 to zero. This forces all of the collector current of Q_8 (160 μA) to flow into the base of Q_9 and provides drive current for the parallel combination of Q_{10} and Q_{11} equal to 160 μA multiplied by the current gain of Q_9. Since transistors Q_{12} and Q_{13} are cut off in this mode, the amplifier output current becomes the emitter current of Q_9 multiplied by the current gain of the Q_{10} - Q_{11} combination. At anticipated current levels, the current gain from the base of Q_9 to the output is typically 2500, so that the maximum positive output current is approximately 400 mA.

The second possibility is a large negative input to the base of Q_1. In this case all of the collector current of Q_7 (200 μA) is switched through Q_1. Of this current, 100 μA flows into the 33-K resistor, with the remaining 100 μA shunted into the base of Q_5. This increases the collector current of Q_5 to approximately 5 mA. Since the current through the diode chain D_{11A} - D_{11F} is limited to 160 μA by Q_8, the 5-mA current must flow through the path containing the 2.7-K resistor shunted by D_{12E} and D_{12F}. The diodes conduct this current directly to the bases of the Q_{12} - Q_{13} combination. The negative output current is 5 mA multiplied by the current gain of the Q_{12} - Q_{13}, or typically 250 mA.

The supply voltage levels are chosen in part to insure that no transistor enters voltage saturation in either of the high-current states until the magnitude of the output voltage exceeds 4 volts.

In the high-current states, the operating current level of either transistor pair Q_{10} - Q_{11} or Q_{12} - Q_{13} increases more than 3 orders of magnitude from the quiescent level. The transistor types used for these pairs are both epitaxial devices which are characterized by uniform gain over a wide dynamic range of current levels, and were selected in part for this important characteristic.

The amplifier shown in Fig. 2-12 and described in this section is the amplifier which is modified for use as a gated amplifier. All of the elements that affect the linear-region ON-state performance of the gated amplifier are included in Fig. 2-12. Accordingly, it is possible

to predict analytically the linear-region performance of the gated amplifier from the circuit shown in Fig. 2-12. These calculations are made in the following sections.

It is useful to point out the elements included in preparation for gating. These include diodes D_1, D_2, D_{16}, D_{17}, and the two 2.2-M resistors. Also, two diodes in both the D_{11} and D_{12} diode chains are required to provide bias voltages necessitated by the forward voltages of D_{16} and D_{17}. All other circuit components would be required if this approach were used for the design of an operational amplifier intended for use in low-power applications.

K. SEMICONDUCTOR CHARACTERISTICS

The values of all resistors used in the basic gated amplifier are included in Fig. 2-12. It is necessary to have the characteristics of the semiconductors employed to initiate linear-region analysis of this circuit.

It is sufficient to specify only the incremental resistance of the diodes for purposes of linear-region analysis, since the effects of shunt capacitance across the diodes are negligible in this circuit. The incremental resistance of all diodes can be determined from the relationship

$$r_d \approx \frac{k25}{I_d}$$

where r_d is diode incremental resistance in ohms and I_d is the current through the diode expressed in milliamperes. The factor k has a value between one and two, depending on the diode type. Tests indicate that the constant is one for all diodes used in the design of the basic operational amplifier. Hence, for this design $r_d = \frac{25}{I_d}$.

The transistor parameters which are used for circuit analysis are presented in Table 2-1, and these parameters apply for the quiescent operating levels of the particular transistor. This table includes all of the transistors in the operational amplifier shown in Fig. 2-12, as well as four additional transistors used elesewhere in the gated amplifier

Table 2-1

Parameters of Transistors as they are used in the Gated Amplifier

Transistor No.	Type	$I_c(\mu A)$	$r_e(\Omega)$	$r_c(\Omega)$	$C_{ob}(pF)$	$C_{ib}(pF)$	β	$I_{CBO}(A)$
Q_1, Q_2	2N3799	100	250	2×10^8	5	10 pf	400	10^{-10}
Q_3, Q_4	2N3707	0.25	*	*	5	*	50	$<10^{-11}$
Q_5, Q_6	2N3563	400	62	5×10^6	3	6	50	*
Q_7	2N3640	200	*	5×10^6	4	*	*	*
Q_8	2N3640	160	*	5×10^6	4	*	*	*
Q_9	2N3563	250	100	8×10^6	3	5	50	*
Q_{10}, Q_{11}	2N3564	50	500	10^7	4	7	25	*
Q_{12}, Q_{13}	2N3640	50	500	10^7	4	7	25	*
Q_{14}	2N3563	GATING TRANSISTORS						
Q_{15}	2N3640	PULSED AT TURNOFF						

*Indicates Parameter Value is Unimportant

which are discussed later. These parameters were obtained from four sources:

1. Published data was used whenever available and when it was felt that the published value was typical rather than a "less than" or "greater than" value. An example of this type of parameter is C_{ob} for all transistors.

2. Emitter resistance for all transistors was obtained from the well-established relationship

$$r_e \approx \frac{25}{I_e}$$

where r_e is the emitter resistance in ohms and I_e is the emitter current expressed in milliamperes. This expression is accurate within several percent at room temperature and at all operating current levels encountered in linear-region operation.

3. Some parameters were derived from published data. An example is the value of C_{ib} at various collector currents for the 2N3563. Typical values for ω_T vs. collector current are available for this device. Since by definition

$$\omega_T = \frac{1}{r_e(C_{ob}+C_{ib})}$$

C_{ib} can be calculated from the ω_T curves, r_e, and C_{ob} which is furnished.

4. Many of the parameters were measured directly including C_{ib} for all transistors other than the 2N3563, r_c for all transistors, and common-emitter current gain (β) for all transistors. The collector-to-base junction leakage current, I_{CBO}, was also measured.

It should be noted that there is a fairly large variation from device to device in many of these parameters, and that the values listed represent typical values. In certain critical locations in the circuit devices must be selected to obtain greater uniformity, and the details of this selection process are outlined in the Appendix I.

It should also be noted that in the case of the capacitances, a correction term of 1 pF has been added to all values to approximate the inevitable stray capacitances present in the circuit.

The rationale behind the selection of these five transistor types from the more than 4000 types currently available is as follows. Probably 95 percent of the available devices are either unacceptable in the intended applications (for example, entertainment-quality germanium transistors or power transistors) or are redundant in the sense that they are identical to other transistors except for some minor variation such as packaging. Selection of the five types from the remaining transistors was made on the basis of experience, either with the particular transistor or with devices of similar geometry and processing, and manufacturer's specifications. The desirability of keeping the number of different types to a minimum was also an important factor.

The following paragraphs discuss some of the more important characteristics of these transistor types. With a single exception, all of the devices listed are the recently introduced plastic-encapsulated types, which have the significant advantage of dramatically reducing the cost of components used in the experimental gated-amplifier circuits. I have concluded these devices are at least as reliable as their metal-cased counterparts, but as yet manufacturers have not offered data which either supports or refutes this conclusion. In any case, the use of these devices in prototype gated amplifiers does not place any limitations on the design, since metal-cased electrically-equivalent devices are available and could be used if required.

All of the devices are silicon planar types. Planar devices are mandatory because of their much more stable parameter values, particularly at low operating current levels.

The devices listed below include those used in Fig. 2-12, as well as one other type used elsewhere in the gated-amplifier circuit. The reason for including switching characteristics in connection with the 2N3563 will become apparent later in this chapter.

2N3563 (Fairchild)

The 2N3563 is an NPN transistor with an extremely high gain-bandwidth product (reaching a maximum of 900 Mc at high collector currents). A

gain-bandwidth product in excess of 200 Mc is maintained at collector currents as low as 100 μA. The current gain is typically 50. This device functions very well in switching circuits, and rise times of less than 5 ns are possible in some circuits. The collector-to-base junction is also used as a diode because of very low leakage current (typically less than 10^{-11}A at 10 volts) and a reverse-bias capacitance under 2 pF.

2N3564 (Fairchild)

The 2N3654 is a larger geometry version of the 2N3563. Because of increased size the capacitances are higher, but current gain is maintained to higher current levels.

2N3640 (Fairchild)

The 2N3640 is an approximate complement to the 2N3563. Because of the problems inherent to PNP technology, capacitances are slightly higher and low-current gain-bandwidth product is lower than those of the 2N3563. Current gain is maintained to higher collector-current levels.

2N3707 (Texas Instruments)

The 2N3707 is an NPN transistor which features excellent current gain at low current levels (typically 50 at 0.1 μA) and low leakage current (less than 10^{-11}A at 10 volts).

2N3799 (Motorola)

The 2N3799 is a PNP which was selected primarily for high-current gain (typically 400 at 100 μA of collector current). Disadvantages include somewhat higher leakage current and capacitances than an NPN with the same gain, but overall circuit considerations dictated the use of PNP transistors in the first stage. This is the only metal-cased transistor used.

L. TRANSFER FUNCTION WITH HIGH-IMPEDANCE LOAD

Models for the individual circuits used in the basic operational amplifier have been developed earlier in this chapter. In this section the models are combined and the linear-region transfer function is developed for the case of a high-impedance load. The results of this

analysis yield the gain and phase curves shown as the Bode plot labelled "uncompensated" in Fig. 2-14.

The circuit models shown in Figs. 2-3, 2-5, and 2-9 are combined with element values shown in Fig. 2-12 and transistor parameters listed in Table 2-1 to form an equivalent-circuit model for the basic operational amplifier. The resultant operational-amplifier circuit model is shown in Fig. 2-13. (In this figure the positive-gain input terminal is assumed grounded, since inputs to the negative terminal are sufficient for the stability calculations.) The boundaries which divide the circuit into three sections are only approximate, as the output impedance of one section is lumped with the input impedance of the following section. The origin of most of the elements in Fig. 2-13 is evident by inspection of the circuit of Fig. 2-12 and the models used for the building blocks, (numerical subscripts on parameter values refer to particular transistors in Fig. 2-12) but several elements require further explanation.

Capacitance C_1 in Fig. 2-13 represents the total capacitance at the node including the base of transistor Q_5 and is the sum

$$C_1 = C_{S1} + C_{ob1} + C_{ib5} + 2C_{ob5}$$

The term C_{ob1} appears because this capacitance shunts the base of Q_5 when the base of Q_1 is grounded. The terms $C_{1b5} + 2C_{ob5}$ represent the input capacitance of the cascode circuit as shown in Fig. 2-5.

Resistance R_2 is the parallel combination $r_{c6} \| r_{c8} \| r_{c9}$ all in parallel with $4.5 \times 2.2\ M \| \frac{r_{c10}}{2}$. This value can be obtained from the buffer model of Fig. 2-9. In order to develop the parameters relating to the buffer amplifier the following relationships are useful:

1. Resistance r_2 in Fig. 2-8 is the dynamic resistance of the diode chain D_{11A} - D_{11F} in Fig. 2-12. The value is 1 K since each diode is operating at approximately 150 μA.

2. Resistance r_3 in Fig. 2-8 is equal to 2.7 K.

3. In order to convert the parameters of Q_9, Q_{10}, Q_{11} and Q_{12} in Fig. 2-12 to the form shown in Fig. 2-8, it is necessary

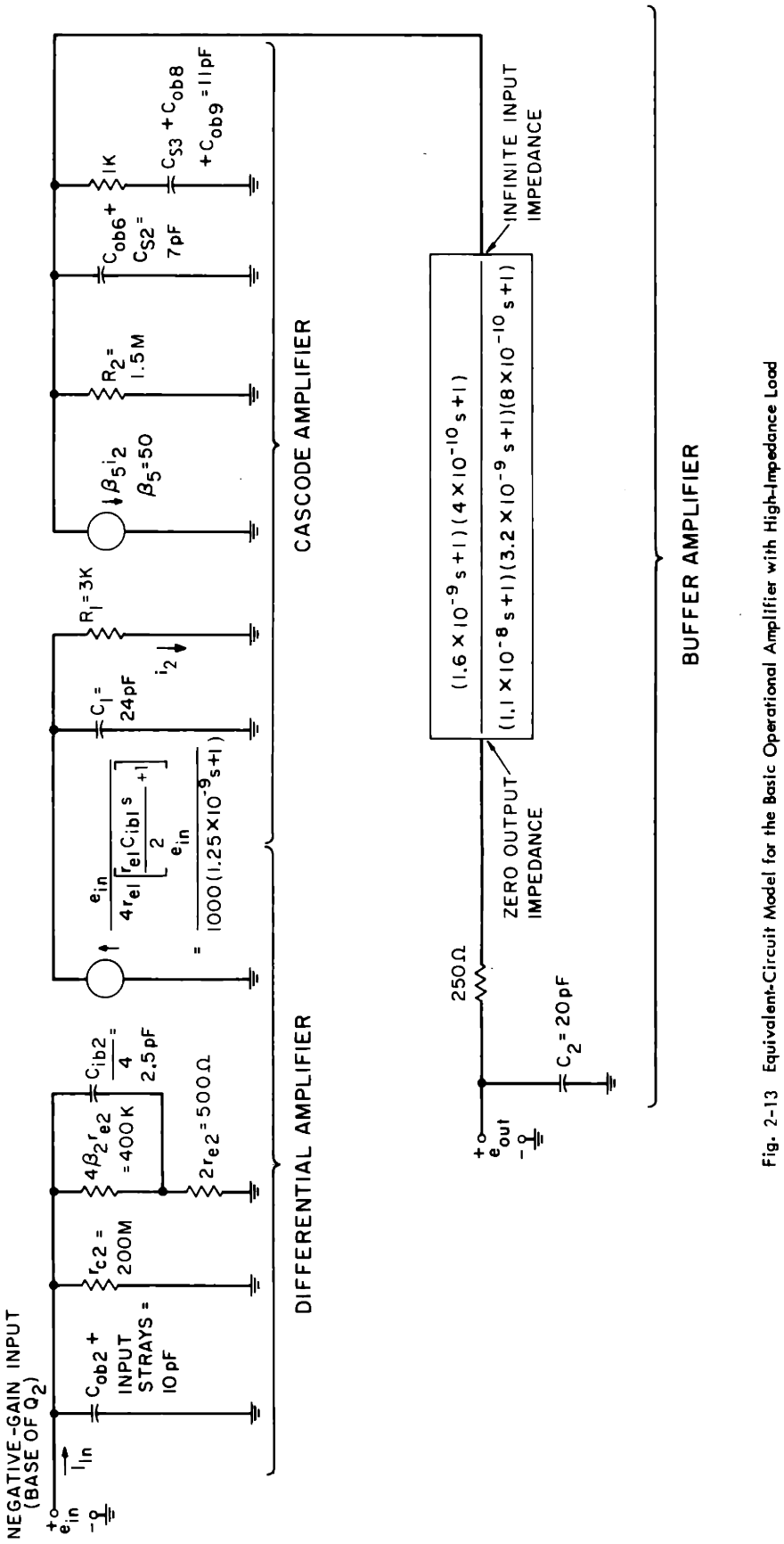


Fig. 2-13 Equivalent-Circuit Model for the Basic Operational Amplifier with High-Impedance Load

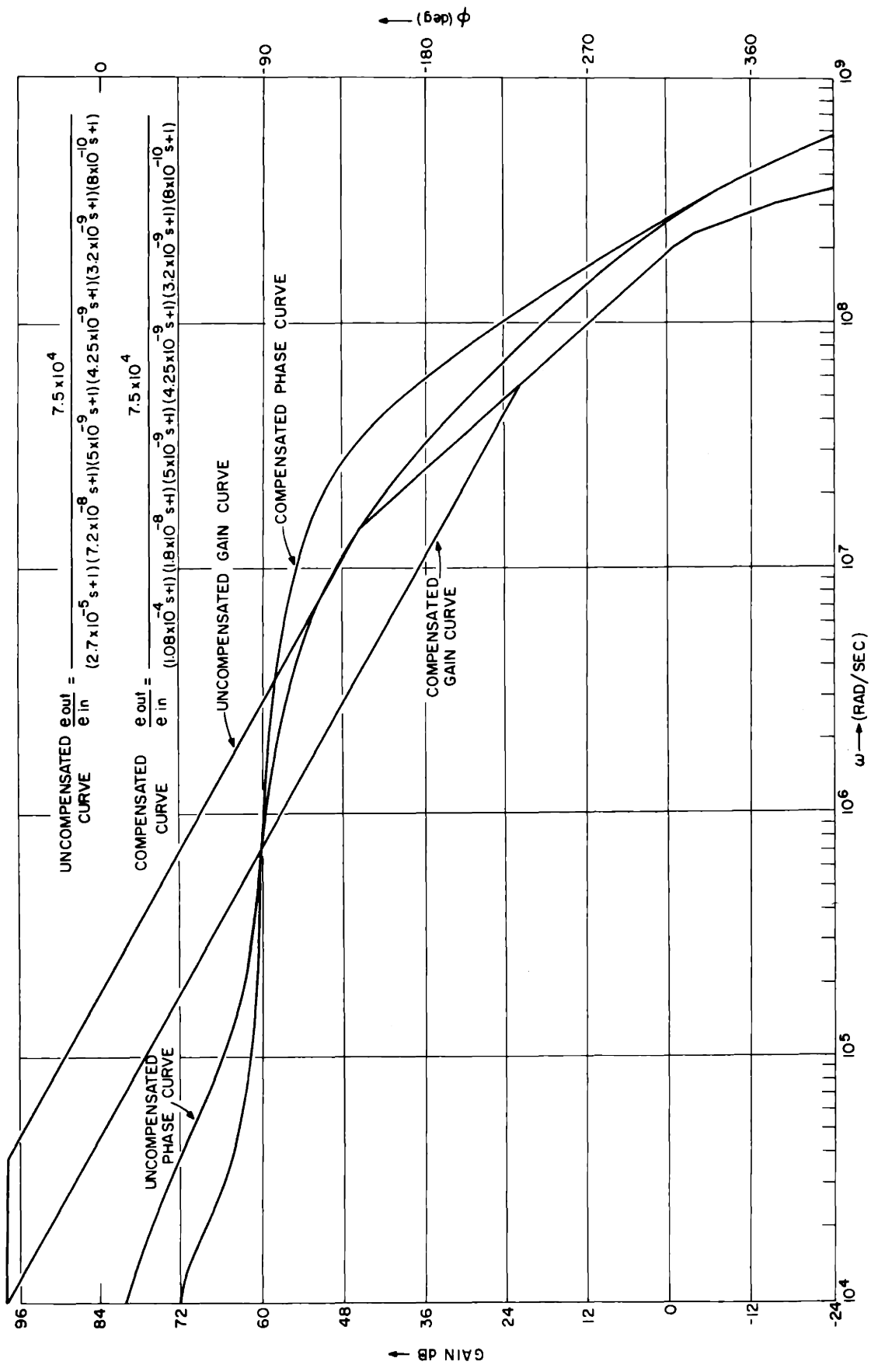


Fig. 2-14 Bode Plots for the Basic Operational Amplifier with High-Impedance Load

to divide resistances by 2, multiply capacitances by 2 and leave β unchanged, since two parallel transistors are actually used for each output transistor shown in Fig. 2-8.

Capacitance C_2 is included to represent the effect of stray capacitance at the output mode (≈ 10 pF) plus the nominal loading capacitance of typically-used feedback networks.

The open-loop gain from the model shown in Fig. 2-13 is

$$\frac{e_{out}}{e_{in}} = \frac{-7.5 \times 10^4 (1.6 \times 10^{-9} s+1)(4\times10^{-10}s+1)}{(2.7\times10^{-5}s+1)(7.2\times10^{-8}s+1)(5\times10^{-9}s+1)(4.25\times10^{-9}s+1)(3.2\times10^{-9}s+1)(1.25\times10^{-9}s+1)(8\times10^{-9}s+1)}$$

The essential features of this expression are related to circuit parameters as follows:

1. The d-c gain, 7.5×10^4, is $\frac{\beta_5 r^*}{4r_{el}}$, where r^* represents the resistance to ground at the collector of transistor Q_6.
2. The first pole occurs at $\frac{1}{r^* C^*}$ radians per second, where C^* is the capacitance to ground at the collector of Q_6. It is evident that this node should produce the dominant pole because of the extremely high resistance to ground.
3. The second pole occurs where the base-to-collector current gain of Q_5 drops 3 db from its d-c value, and is located two and one half decades beyond the first pole.
4. All other singularities are located at least a decade beyond the second pole.

These observations summarize the reasons that this particular configuration is extremely useful as an operational amplifier. Because most of the gain is obtained in one stage and because this stage has low input capacitance, the transfer function of the amplifier can be approximated as a first-order transfer function over a wide range of frequencies. This type of transfer function is easy to compensate and is ideally suited for use with feedback.

One further approximation is introduced at this time. It will be shown that the amplifier cannot be stabilized for cross-over frequencies much in excess of 10^8 radians per second. Four of the singularities in

the transfer function occur at frequencies in excess of 5×10^8 radians per second. The four singularities which fall into this category include zeros located at 6.25×10^8 and 2.5×10^9 radians per second and poles at 8×10^8 and 1.25×10^9 radians per second. The only noticeable effect of singularities located this far above the cross-over frequency arises from phase shift. For example, at 1/5 of its break frequency a pole contributes 11.3° of negative phase shift to a transfer function, yet only reduces the amplitude by 2 percent. Two high-frequency singularities mentioned in the analysis of the cascode circuit and then temporarily dropped can also be included. These singularities are a right-half-plane zero at 5.5×10^9 radians per second and a pole at 1.8×10^9 radians per second. The approximate phase shift of all of these singularities at frequencies of interest is given as

$$\phi = 1.6 \times 10^{-9}\omega + 4 \times 10^{-10}\omega - 1.25 \times 10^{-9}\omega - 8 \times 10^{-10}\omega$$

$$- 5.5 \times 10^{-10}\omega - 1.8 \times 10^{-10}\omega = -8 \times 10^{-10}\omega$$

All of these singularities can be modeled as a single pole $\frac{1}{8\times10^{-10}s+1}$, which has equal phase shift at frequencies of interest. With this simplification the transfer function becomes

$$\frac{e_{out}}{e_{in}} = \frac{-7.5 \times 10^4}{(2.7\times10^{-5}s+1)(7.2\times10^{-8}s+1)(5\times10^{-9}s+1)(4.25\times10^{-9}s+1)(3.2\times10^{-9}s+1)(8\times10^{-10}s+1)}$$

This equation is shown as an asymptotic log magnitude and phase vs. log frequency plot (or Bode plot) in Fig. 2-14. The curves labelled "uncompensated" pertain to the amplifier as shown in Fig. 2-12.

M. A METHOD FOR COMPENSATION

An open-loop transfer function which is approximately first order, at least at frequencies where the gain is near unity, is ideal in many gated-amplifier applications. This type of transfer function results in a well-damped closed-loop transient response. Furthermore, it can be shown by means of describing-function analysis [7] that a first-order system remains absolutely stable in the presence of saturation. This type of stability is important

in the case of the gated amplifier because the amplifier always saturates during the turn-on transient, and the low quiescent currents used in the design lead to momentary saturation for many types of input signals. Rapid, well-damped recovery from saturation is required in many applications.

Examination of Fig. 2-14 shows that the transfer function of the basic operational amplifier is approximately first order if frequency-independent feedback with an attenuation greater than 46 dB is used. Instability will result if less attenuation than 30 dB is used in the feedback path since the amplifier gain is 30 dB at the frequency that the phase shift equals -180°. Since it is necessary to use the amplifier with unity feedback in many applications, some method for modifying the transfer function is required.

It can be shown that r-c networks can be used to modify the transfer function of an amplifier in any desired way subject to the constraint that the magnitude of the modified transfer function must be less than or equal to that of the unmodified transfer function at all frequencies. For example, the first pole of the amplifier discussed here occurs because of capacitive loading at the collector of Q_6. It is possible to move this pole toward lower frequencies by adding a capacitor to ground at this node. A zero can then be added to the transfer function at some higher frequency by including a resistor in series with the capacitor used for compensation. This zero can be located so as to compensate a pole. One possible modification of the transfer function is shown in Fig. 2-14 as the compensated curves. These curves could be obtained by loading the collector of Q_6 with a network consisting of a 56-pF capacitor in series with a 1.2-K resistor.

This type of compensation increases the separation between open-loop poles so that the amplifier is stable for larger feedback ratios. Theoretically, the process could be continued by adding r-c networks to ground at other nodes so that the resultant compensated transfer function was first order at all frequencies where the gain exceeded unity.

This method is unsatisfactory for at least two reasons. First, simple modification of the transfer function to optimize performance for various feedback ratios would not be possible. Second, the required capacitors can become quite large. A 1000-pF capacitor would

be required at the node including the collector of Q_6 to stabilize the amplifier in applications involving unity feedback. In order to gate the amplifier this capacitor would have to be charged and would introduce a prohibitively long turn-on delay.

Sufficient transfer-function control for all intended applications can be obtained through the use of a small capacitor across the terminals labelled compensation in Fig. 2-12 without introducing the disadvantages inherent to large capacitor values. This compensating capacitor appears between the base of Q_5 and the emitter of Q_9. Since Q_9 is an emitter follower, the voltage at its emitter is the same as that at the collector of Q_6, and inclusion of this compensating capacitor introduces an artificial Miller capacitance around the cascode-amplifier section. Because of the high gain of the cascode amplifier, extremely small capacitors in this location cause significant changes in the transfer function.

The effect of this type of compensation can be predicted by considering it as feedback around a high-gain portion of the amplifier. The transimpedance of the section of interest is

$$\frac{e_{out}}{i_{in}} = \frac{-7.5 \times 10^{7}}{(2.7 \times 10^{-5}s+1)(7.2 \times 10^{-8}s+1)(4.2 \times 10^{-9}s+1)}$$

where e_{out} is the voltage at the emitter of Q_9 and i_{in} is the current supplied to the base of Q_5.

If a capacitor is placed between the emitter of Q_9 and the base of Q_5 (this capacitor is designated as C_c), the capacitor forms a feedback path with an admittance given by $C_c s$. The effect of such a compensating capacitor can be approximated as follows:

The transimpedance of this stage remains

$$\frac{e_{out}}{i_{in}} = \frac{-7.5 \times 10^{7}}{(2.7 \times 10^{-5}s+1)(7.2 \times 10^{-8}s+1)(4.2 \times 10^{-9}s+1)}$$

at any frequency where the gain around the loop including C_c is less than unity. The transimpedance of this portion of the amplifier is changed

to $-\frac{1}{C_c s}$ at any frequency where the gain around this loop exceeds unity. The loop gain is given by

$$\frac{7.5 \times 10^{7} C_c s}{(2.7 \times 10^{-5} s+1)(7.2 \times 10^{-8} s+1)(4.2 \times 10^{-9} s+1)}$$

A more detailed analysis shows that this approximate relationship is valid for the range of capacitor values (1.5 pF to 25 pF) used to compensate the gated amplifier.

Even if no external capacitor is used, the amplifier is partially compensated by stray circuit capacitance. It can be seen from Fig. 2-12 that it is not necessary to apply compensation between the emitter of Q_9 and the base of Q_5. Since the amplifier gain is unity between the collector of Q_6 and the output, a capacitor between any point in the amplifier beyond the collector of Q_6 and the base circuit of Q_5 has the same effect. It can be seen from the expression for the gain around the compensating loop that the minimum capacitance required to modify the transfer function is 0.3 pF.

In spite of attempts to minimize this stray capacitance during construction, values far in excess of 0.3 pF are present. It is necessary to measure the magnitude of this capacitance in order to predict linear-region performance and direct measurement seems impossible. One indirect method involves measurement of open-loop gain at some frequency where the gain is determined by the stray capacitance. This does not seem a particularly valid technique when one considers that the resultant value will be used to predict the open-loop transfer function.

A method which does not suffer from this inherent limitation is as follows. The amplifier is operated open loop and a positive step is applied to the base of Q_2 (see Fig. 2-12). This causes an increase of the base current of Q_5, forcing the output voltage negative. Because of the high gain of the amplifier from the base of Q_5 to the output, equilibrium is reached when the current supplied to the base of Q_5 equals the rate of change of output voltage multiplied by the capacitance between the output circuit and the base of Q_5.

The result of this measurement, made on several amplifiers, indicates that the effective compensating capacitance is 1.5 pF, with

an uncertainty including both variations from circuit to circuit and measurement errors of -0.5 pF, + 1.0 pF. A Bode plot for the complete amplifier including this compensation is shown in Fig. 2-14 as the compensated amplifier curve. It can be seen that the effect of the 1.5-pF stray compensating capacitance is the same as that of loading the collector of Q_6 with an r-c network to ground as described earlier. Predictions of amplifier performance based on this plot are compared with measured performance in Chapter III.

It is possible to question the value of the cascode circuit in view of the fact that the normal method of amplifier compensation involves the use of an artificial Miller capacitance which is often several times larger than the Miller capacitance which would be present if the cascode amplifier were replaced by a grounded-emitter stage. The use of the cascode circuit enhances amplifier performance for the following reasons:

1. The maximum gain which can be obtained at any frequency is shown in Fig. 2-14 as the compensated curve. The gain at frequencies from $\omega \approx 10^4$ radians per second to $\omega \approx 5 \times 10^7$ radians per second is controlled by the 1.5-pF compensating capacitance. If the cascode were replaced by a grounded-emitter stage, the gain over this frequency range would be reduced by a factor of 3 due to increased effective compensating capacitance. The compensating capacitance would be approximately 4.5 pF, including 3 pF from C_{ob} of the transistor and 1.5 pF from stray capacitance. (The stray capacitance is not introduced by the cascode circuit, and thus would not be changed by elimination of the cascode.)

2. The portion of the total compensating capacitance attributable to C_{ob} of the transistor involved would be dependent on the collector-to-base voltage of this transistor, since C_{ob} varies with applied voltage. This would lead to nonlinear performance.

3. The maximum low-frequency gain would be drastically reduced. The d-c gain of the amplifier shown in Fig. 2-12 is $\frac{\beta_5 r^*}{4 r_{e1}}$,

where r^* represents the total resistance to ground at the node including the collector of Q_6. For the devices used this equation predicts a gain of 7.5×10^4 at zero frequency. Because of feedback through the collector-to-base resistance of a grounded-emitter stage, eliminating Q_6 in Fig. 2-12 would reduce the d-c gain to $\frac{r_{c5}}{4r_{e1}}$, or about 5×10^3.

The third consideration leads to the somewhat unexpected conclusion that the cascode circuit, originally introduced as a method for improving high-frequency performance, has the added benefit of greatly increasing d-c open-loop gain.

N. POWER-BANDWIDTH TRADEOFF

A major design consideration for a gated amplifier circuit intended for use in space applications is the minimization of quiescent power consumption. It is probable that in certain other gated-amplifier applications (particularly in ground-based computers), the designer may be willing to expend greater power in order to enhance frequency response. Similarly, in some space applications where lower bandwidth is tolerable, a further power reduction would be advantageous.

This section illustrates the possibility of a power-bandwidth compromise. The analysis is limited to the case of scaling the quiescent collector current of each transistor by a constant factor K. Further, the discussion is limited to the devices used in the basic operational amplifier, but the same general relationships will be true for any transistor types. Several relationships between transistor parameters and current level are required to show the effects of a change in operating current:

1. The emitter resistance of a transistor in ohms is given by $r_e \approx \frac{25}{I_c} + r_o$, where I_c is expressed in milliamperes. The constant term r_o is typically 2-3 ohms for the devices used in the amplifier. Thus, at least up to current levels approximately 5 times greater than those used in the amplifier, the emitter resistance of a transistor is simply inversely related to collector current.

2. The collector-to-base conductance, $\frac{1}{r_c}$, equals $g_o + g_1 I_c$, where g_o represents the contribution from surface leakage. The term containing g_1 predominates at any current level which might be used, so that r_c is inversely related to collector current.

3. The collector-to-base capacitance, C_{ob}, is independent of collector current.

4. The current gain of planar transistors is largely independent of operating current. In the case of the transistors used in the circuit, β changes less than 20 percent with collector current variations from 1/2 to 5 times nominal values.

5. The base-to-emitter capacitance, C_{ib}, can be represented as $C_o + C_1 I_c$. For all transistors used in the circuit except the 3N3563's, the term C_o predominates until current levels in excess of 3 times those used. For the 2N3563, C_o is approximately 3 pF, while C_1 is approximately 8 pF per milliamp. Thus the C_{ib} term for the 2N3563's cannot be considered constant over the current range of interest.

The derivations leading to the open-loop plots of Fig. 2-14 show that all singularities in the amplifier transfer function are a result of r-c time constants. Aside from small modifications (less than 10 percent) arising from fixed resistances in the circuit, all resistances affecting the location of singularities are linear combinations of transistor resistances. These resistances would be reduced by a factor of $\frac{1}{K}$ if all collector currents were increased by a factor of K.

All capacitances are either transistor capacitances or stray capacitances. The only node where a change in quiescent current can change a node capacitance significantly is at the base of Q_5 (Fig. 2-12). At the normal current level, the portion of the node capacitance attributable to the variable portion of C_{ib5} is approximately 3 pF, or 12 percent of the total node capacitance. Increasing the collector current of Q_5 to 3 times its original value would increase the node capacitance by only 25 percent.

Thus, to a first approximation, the only change in the amplifier transfer function introduced by increasing all currents by a factor K is to shift the location of all singularities to frequencies which exceed their original locations by a factor of K. The d-c gain, which includes the ratio of two resistances, is unchanged. This approximation is valid for changes in operating current levels from approximately one half to three times nominal levels.

While this experiment was not performed on the gated-amplifier circuit, it has been performed with similar operational-amplifier circuits. The predicted result that, to a first approximation, bandwidth is directly proportional to d-c operating current and consequently (for the same output voltage range which fixes supply voltages) to steady-state power dissipation has been verified.

O. TRANSFER FUNCTION WITH LARGE CAPACITIVE LOAD

Large capacitors are used as amplifier loads in all sampling operations. The behavior of the amplifier for this type of load is predicted with the aid of the models of Figs. 2-3, 2-5, and 2-11. These models are combined with element values presented earlier to form the equivalent-circuit model shown in Fig. 2-15.

If the transfer function is evaluated for a capacitive load in the range of 0.05 μF to 1.0 μF (these are typically used values), the phase shift at the unity-gain frequency is several degrees more negative than -180°. This is an intolerable situation since unity feedback is normally used in sampling applications. One method which can be used to introduce a zero in order to stabilize the amplifier is to include a small resistor in series with the load capacitor.

The transfer function of the model shown in Fig. 2-15 was evaluated for a load impedance (Z_L) consisting of a 1-Ω resistor in series with a 1-μF capacitor. Under these conditions the amplifier unity-gain frequency is 3×10^6 radians per second, and the phase margin at this frequency is more than 50°. Linear theory predicts that this type of transfer function should yield well-damped responses with unity feedback applied around the amplifier.

One of the prototype amplifiers was tested with this load and unity feedback, and somewhat undesirable performance was observed. The

system is perfectly stable for small inputs, but exhibits a severe high-frequency oscillation at 10 Mc to 15 Mc for any input greater than 1 mV. The oscillation will always decay, but generally not for several microseconds. This type of oscillation is undesirable for several reasons:

1. The currents involved in the oscillation are typically several hundred mA, and this leads to high power dissipation.
2. The oscillation could cause a circuit driven by such an amplifier to malfunction because of saturation on the high-frequency large-amplitude signal.
3. The oscillation could couple to adjacent circuits.
4. The settling time is increased for certain capacitive loads.

Since it is not possible to demonstrate the existence of this mode of oscillation with linear analysis, an approximate describing-function analysis was performed in an attempt to determine its cause. This analysis shows that the major effect of applying inputs to the amplifier with a large capacitive load is to alter the gain, with little change in the location of singularities. The gain can either decrease or increase depending on the magnitude of the input. Large inputs reduce gain because of saturation. Small inputs increase gain, and this effect can be demonstrated with reference to Fig. 2-15. At high frequencies, one multiplicative term in the gain term is the ratio of the resistor included in series with the load capacitor to the 50-K resistor shown in Fig. 2-15.

The 50-K resistor represents the emitter resistance of the output transistors multiplied by a current-gain term. The magnitude of the emitter resistance is inversely related to output current. It can be shown that for some values of output current the high-frequency gain of the amplifier increases by more than 20 dB from this effect.

The types of transfer functions that will insure stability for all anticipated gain changes are somewhat restricted. It can be shown that the amplifier will remain stable if the phase shift is less negative than -180° at all frequencies from zero to approximately one decade beyond the nominal unity-gain frequency.

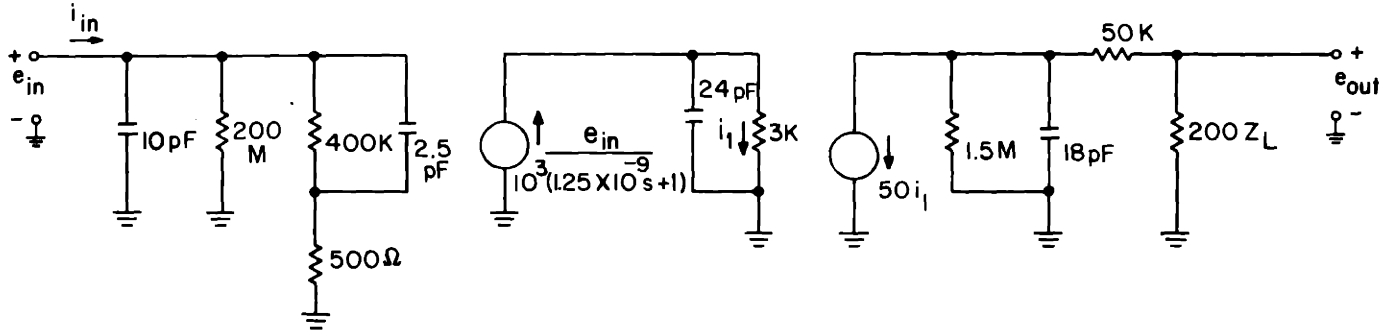


Fig. 2-15 Equivalent-Circuit Model for the Basic Operational Amplifier with Large Capacitive Load

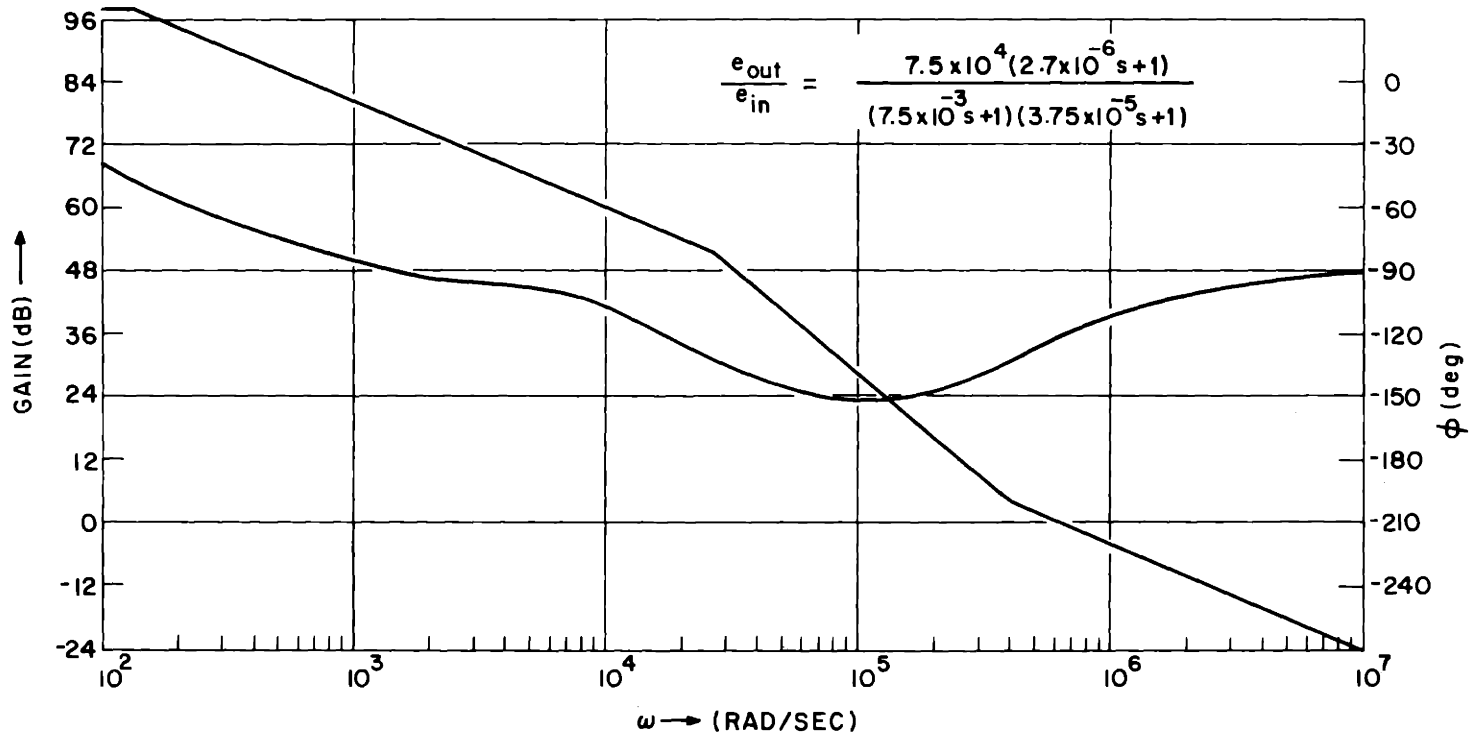


Fig. 2-16 Bode Plot for the Operational Amplifier with 1μF and 2.7Ω Load, 15pF Compensating Capacitor

This type of compensation can be accomplished by the combination of a small resistor in series with the load capacitor and a compensating capacitor. The parameter values selected for demonstration purposes are a load consisting of a 1-μF capacitor in series with a 2.7-Ω resistor and a 15-pF compensating capacitor. With this load, the transfer function predicted by the model of Fig. 2-15 (without including the effects of the compensating capacitor) is

$$\frac{e_{out}}{e_{in}} = \left[\frac{-7.5 \times 10^{7}(2.5 \times 10^{-4}s+1)}{(7.5 \times 10^{-3}s+1)(10^{-6}s+1)(7.2 \times 10^{-8}s+1)}\right] X$$

$$\left[\frac{10^{-3}(2.7 \times 10^{-6}s+1)}{2.5 \times 10^{-4}s+1}\right]$$

In this expression the pole from the input stage has been neglected, since it occurs at a frequency more than 3 decades beyond the unity-gain frequency.

The first bracketed term represents the transimpedance from the base of Q_5 to the emitter of Q_9 (Fig. 2-12). This is the only portion of the transfer function which can be modified with a compensating capacitor. By analogy to the case presented in Section K, a compensating capacitor should leave this portion of the transfer function unchanged at all frequencies where its magnitude is less $\frac{1}{\omega C_c}$, and change it to $\frac{-1}{sC_c}$ at all other frequencies. If a 15-pF compensating capacitor is included, the open-loop gain becomes

$$\frac{e_{out}}{e_{in}} = \frac{-7.5 \times 10^{4}(2.7 \times 10^{-6}s+1)}{(7.5 \times 10^{-3}s+1)(3.75 \times 10^{-5}s+1)}$$

There is one additional pole in this gain expression, but its location has been moved more than 2 decades beyond the unity-gain frequency by compensation.

This transfer function is plotted as Fig. 2-16. Note that the crossover frequency with unity feedback occurs at 6.5×10^{5} radians per second, with a phase margin of 60^{o}. While poles occurring more than

two decades beyond crossover have been eliminated, an approximation to the effects of these high-frequency poles indicates that the phase shift should not exceed -180° until some frequency beyond 10^{8} radians per second. Thus increases in open-loop gain should not cause instability unless the gain increase exceeds approximately 46 dB. Similarly, gain decreases cannot cause instability since the phase margin exceeds 30° for any cross-over frequency below 6.5×10^{5} radians per second.

While this example has used specific load and compensating element values, it can be shown that similar stabilization techniques can be used for any anticipated load capacitor. The type of compensation used with the amplifier to obtain the Bode plot of Fig. 2-16 is ideally suited for use with capacitively-loaded gated amplifiers for two reasons:

1. When in the linear region, the amplifier should display a well-damped, rapid (at least considering the size of the load capacitor) transient response.

2. If the main effect of changes in output current is a gain variation, stability should be maintained for any conceivable variation, resulting in an absolutely stable system.

These predictions are compared with experimental results in Chapter III.

P. A METHOD FOR GATING

The problem of gating the basic operational amplifier to obtain a gated amplifier has been completely ignored to this point in the development. This may seem somewhat unusual in view of the fact that this gating or switching capability is the major feature which distinguishes a gated amplifier from an operational amplifier, and that this feature is responsible for the power economy and versatility of the gated amplifier. This approach has been followed for two reasons. First, the usefulness of the circuit is determined to a very large extend by the performance of the gated amplifier in the ON state. Gating does not offer any way to circumvent problems caused by poor ON-state performance. Second, the gating technique is simple to include in the basic amplifier design considered here, and it is worthwhile compromising gating-circuit complexity to enhance ON-state characteristics.

The features that the gated amplifier should possess which are attributable to gating are:

1. Extremely low power consumption in the OFF state is mandatory to maintain low average power consumption.
2. Rapid transition to the OFF state is required, at least in cases where capacitors connected to the amplifier are used for storage of information during the OFF time. In these cases, a voltage is stored on the capacitor during the time the amplifier is ON, and slow turnoff would tend to alter its value.
3. Low leakage current in the OFF state is required to insure slow degradation of voltages held on capacitors.
4. Turn-on time should be minimized in order to increase the frequency of operation in pulsed applications, but this requirement is less important than the other three.

The circuit shown in Fig. 2-12 can be turned OFF in the following way:

The grounded end of the 27-K resistor connected to the bases of Q_7 and Q_8 is connected to +9 volts. This turns off Q_7 and Q_8. With transistor Q_7 off, Q_5 must turn off. Transistor Q_6 turns off and this reduces the current through diode chain D_{11} and the base drive for Q_9 to zero. Eventually, the node including the base of Q_{10} is charged to -7 volts by the 2.2-M resistor connected to this node and the node including the base of Q_{12} is charged to +7 volts by a separate 2.2-M resistor. In this state every transistor in the diagram is cut off, and every diode is back biased. The only currents which flow in the circuit in this state are leakage currents. The output current is the difference between the leakage currents of D_{16} and D_{17} which is less than 10^{-11} A at room temperature.

The OFF-state input current at either input terminal consists of two terms, the collector-to-base leakage current (I_{CBO}) of the particular input transistor and the reverse leakage current of the diode in the transistor emitter. (This assumes that the diode reverse leakage is smaller than emitter-to-base leakage I_{EBO} which is true for the devices used and further that the common connection of D_1 and D_2 is

biased negative. A technique which insures this condition is introduced later.)

The reason for diodes D_1, D_2, D_{16}, and D_{17} is now apparent. These devices minimize OFF-state terminal currents, and are used because diode leakages are typically several orders of magnitude lower than I_{EBO} values. Furthermore, these diodes prevent reverse breakdown of various base-to-emitter junctions.

The basic simplicity of the gating method is evident. Transistors Q_7 and Q_8 in Fig. 2-12 are used as gating switches, and these transistors were required to enhance linear region performance. Their inclusion does not represent a complexity penalty which is attributable to the gating feature. This natural gating ability is a further advantage of the basic operational-amplifier design.

From the considerations presented above it is evident that the basic operational-amplifier design shown in Fig. 2-12 is gatable. However, turn OFF is delayed; the amplifier spends a significant time in a "quasi ON" state following application of a turn-off signal because of relatively slow discharge of a number of nodes. This could result in the loss of voltage levels held on storage capacitors.

Figure 2-17 shows the basic operational amplifier modified for use as a gated amplifier. The differences between Figs. 2-12 and 2-17 are mainly elements that speed up the transition to the OFF state.

Turn OFF is accomplished by switching the gate lead from ground to +9 volts, and this transition is assumed to occur in less than 10 ns (10 percent to 90 percent of full value). The 68-pF speed-up capacitor added in parallel with the 27-K resistor in the gate lead insures rapid cutoff of Q_7 and Q_8. Diode D_7 is added to limit the maximum positive voltage applied to the bases of Q_7 and Q_8 in order to prevent breakdown.

Transistor Q_{14} (which is normally not conducting) is pulsed on momentarily by base current provided through the 47-pF capacitor, and its collector voltage is driven to -7 volts. This action turns on Q_{15} momentarily, and forces its collector voltage to +7 volts.

A number of diodes are connected between the collectors of Q_{14} and Q_{15} and certain nodes in the circuit. In normal operation these diodes are back biased and, since they are actually collector-to-base

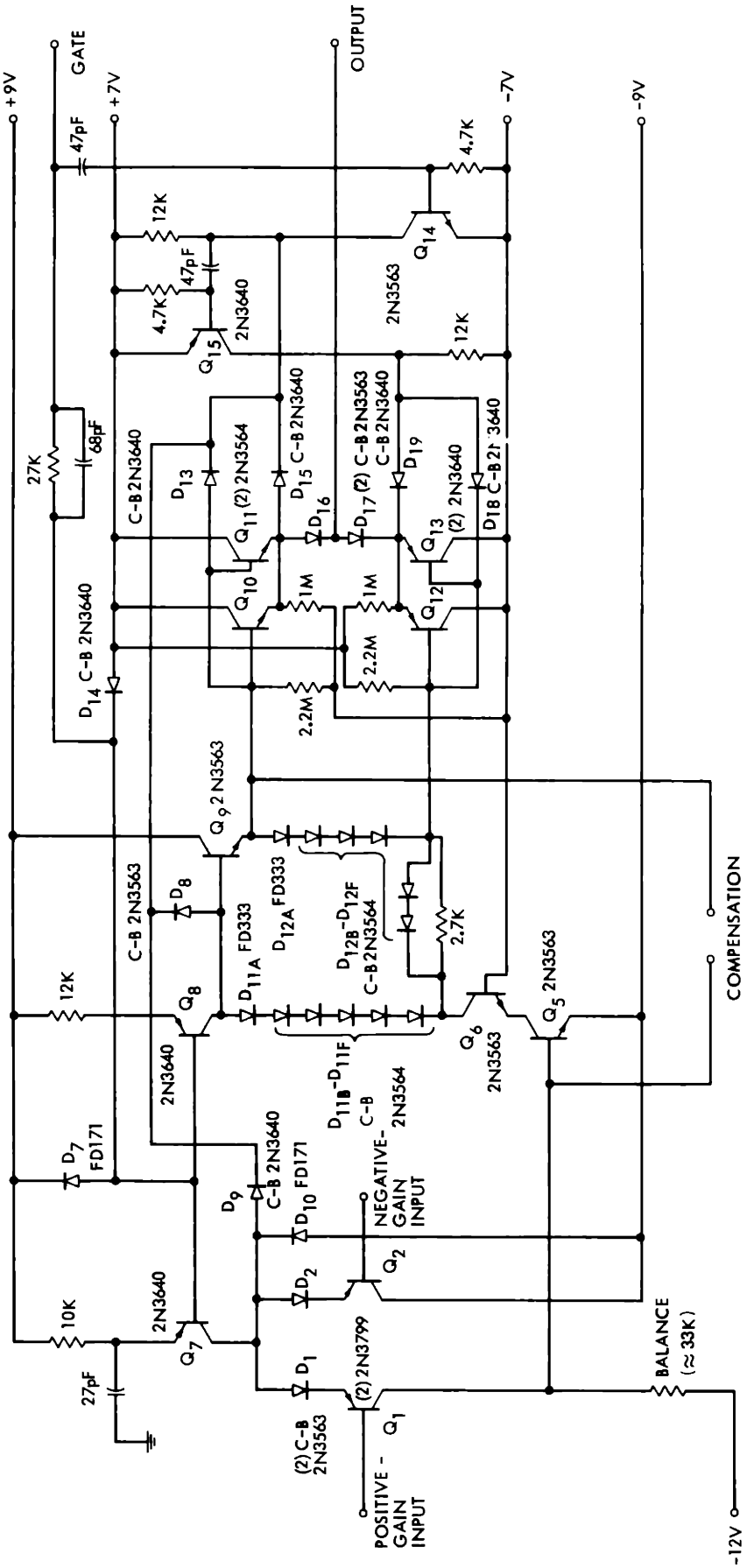


Fig. 2-17 Basic Gated Amplifier

junctions of high-frequency transistors, represent very high-impedance paths to incremental grounds and therefore do not affect normal operation.

The only time any of these diodes conducts is immediately following a turn-off signal. At this time diodes D_{15} and D_{19} back bias the output diodes, which disconnects the output lead. The 1-M resistors added between the emitters of Q_{10} - Q_{13} and supply voltages insure that diodes D_{16} and D_{17} remain reverse biased when the collector voltages of Q_{14} and Q_{15} recover to quiescent values. Since these resistors load low-impedance points, ON-state operation is not affected. Diodes D_{13} and D_{18} insure rapid turnoff of the output transistors by reverse biasing these devices, while diode D_8 turns off Q_9. Diode D_9 turns off the input transistor pair by pulsing the node including the collector of Q_7 to -7 volts. However, this node might tend to return to a more positive voltage at some later time because of the leakage current from Q_7. This action would cause Q_7 leakage current to appear at one of the input terminals by forward biasing D_1 or D_2. The leakage current of diode D_{10} prevents this type of recovery. The FD 171 diode type was selected since its room temperature leakage current (10^{-8}A) is typically 2 orders of magnitude greater than the leakage current of Q_7. A resistor could be used to perform the same function, but this would degrade performance in the ON state by reducing common-mode rejection. The FD 171 has a dynamic resistance of more than $10^9\Omega$ and a shunt capacitance of less than 1 pF and these values do not degrade ON-state performance.

It is useful to define a quantity which I call charge dump in connection with the turn-off process. This is the net amount of charge (the integral of the terminal current) which leaves the input or output terminals during the turn-off transient. In order to minimize errors in sampling operations the magnitude of this charge dump must be small.

The output terminal is considered first. The only elements which need be considered in this case are the output diodes, D_{16} and D_{17}. Charge will be dumped at turn OFF because of charge stored in these two devices. This charge is insignificantly small (less than 10^{-12} coulomb). A more significant charge is dumped into the output circuit because of the shunt capacitance across D_{16} and D_{17}. For example, if the output

voltage at turn OFF is V, the voltage which is switched across D_{16} is (V+7), and D_{16} supplies an amount of charge to the output equal to $-C_{16}(V+7)$. (C_{16} is the junction capacitance of diode D_{16}). Similarly, the charge from switching the voltage across D_{17} is $C_{17}(7-V)$. The maximum sum of these two terms occurs for maximum positive or negative V. With the assumptions that both capacitances are equal to 2 pF and that the maximum output voltage is ±4 volts, the total output charge dump must be less than 1.6×10^{-11} coulomb.

At the negative input terminal, the charge dump is limited to the charge stored in Q_2 plus a term from the voltage transition across the combination of diode D_2 and the base-to-emitter junction of Q_2. In this case the predominant contribution is related to the junction capacitance of diode D_2, and the maximum expected charge dump at the negative input terminal is 2.5×10^{-11} coulomb. The situation is similar at the positive input terminal, except that additional charge is dumped through the collector-to-base capacitance of transistor Q_1. The maximum charge dump at this terminal is limited to less than 4×10^{-11} coulomb.

In practice, the value of storage capacitors connected to these three amplifier terminals generally exceeds 0.05 μF. Thus the voltages stored on typical value capacitors are changed less than 1 mV by charge dump. This effect is normally masked by errors from dielectric absorption.

While the process of node discharge described above is helpful in minimizing turn-off time errors arising from charge dump, the equivalent technique can not be successfully implemented at turn ON for a fundamental reason. The node voltages required for linear region performance are not known a priori, since these node voltages are dependent upon the voltages present at the amplifier inputs and output at turn-on time. Accordingly, the amplifier incorporates no speed-up elements to minimize turn-on times.

Exact prediction of turn-on time is complex, but several considerations can be used to estimate typical times:

1. A significant factor is the time required to charge the node which includes the base of Q_5. The period when this node is charged may occur immediately following turn ON, or may

be delayed depending on input and output voltages. This transient can be represented by the charging transient of the capacitance at this node shunted by the 33-K resistor and driven by the total collector current of Q_7. Only half the transient need be completed to turn on Q_5. The node capacitance is 18 pF during the turn-on transient. This value is lower than the 24-pF capacitance present when Q_5 is on, since the input capacitance of Q_5 is lower when it is not active. This portion of the turn-on transient should therefore take 0.3 μs.

2. The node at the collector of Q_8 must also be charged to a voltage level determined by the output voltage. A maximum change in node voltage of 12 volts is possible, and this requires a charging time of 0.8 μs.

3. The time required to charge other nodes is quite small, since the available currents are larger.

4. It is possible for effects 1 and 2 to be additive since certain combinations of input and output voltages prevent the node including the base of Q_5 from starting to charge until the node including the collector of Q_8 has completed its transient.

These considerations lead to the conclusion that the maximum turn-on time should be less than 1.1 μs.

A significant feature of the circuitry added to enhance gating is that it does not add noticeably to average power consumption. The additional steady-state power consumption is limited to levels corresponding to various leakage currents. There is also a contribution from the power required by Q_{14} and Q_{15} at turn OFF, but since Q_{14} and Q_{15} are normally on for only 1 μs to 2 μs following application of a gating pulse, the average power consumption of these transistors is negligible at any reasonable gating frequency.

Q. MODIFICATIONS TO IMPROVE PERFORMANCE

The design described in preceding sections of this chapter incorporates the major characteristics of a gated amplifier and could be used in many intended applications. However, in order to insure that the

circuit yields ultimate performance in all applications it is necessary to improve certain characteristics further.

The modifications discussed in this section are included to minimize the following deficiencies of the design shown in Fig. 2-17:

1. ON-state input current is too high for some applications such as long-term integration. The input current is approximately 0.25 μA at room temperature.

2. OFF-state input current is relatively high (10^{-10} A), at least compared to the leakage current which appears at the output terminal. This value leads to high drift rates in sampling operations.

3. Voltage drift referred to the input is approximately 150 μV per degree centigrade. This value results in excessive errors with temperature variations.

4. The design shown in Fig. 2-17 includes no power-supply decoupling networks. This lack could lead to amplifier instabilities dependent upon the type of power supplies and lead lengths used, or undesired coupling among amplifiers in a system.

The gated-amplifier circuit shown in Fig. 2-18 incorporates certain additional components into the design in order to improve the characteristics listed above. The major penalty paid to improve these characteristics is one of circuit complexity, and in some less demanding applications the complexity increase may not be justifiable in terms of the resultant performance improvement. In these cases, certain components can be simply eliminated from the design shown in Fig. 2-18.

The compromise of increasing complexity to improve performance has been used throughout the design. The circuit illustrated in Fig. 1-2 is a gated amplifier and all of the additional components introduced in this chapter are included to overcome the obvious limitations of this circuit.

The circuit shown in Fig. 2-18 was used for all experimental phases of the research and all performance characteristics were determined from this circuit. The discussion of this section and the analysis included in Chapter III permits calculation of the performance degradation that can be expected if certain components are eliminated.

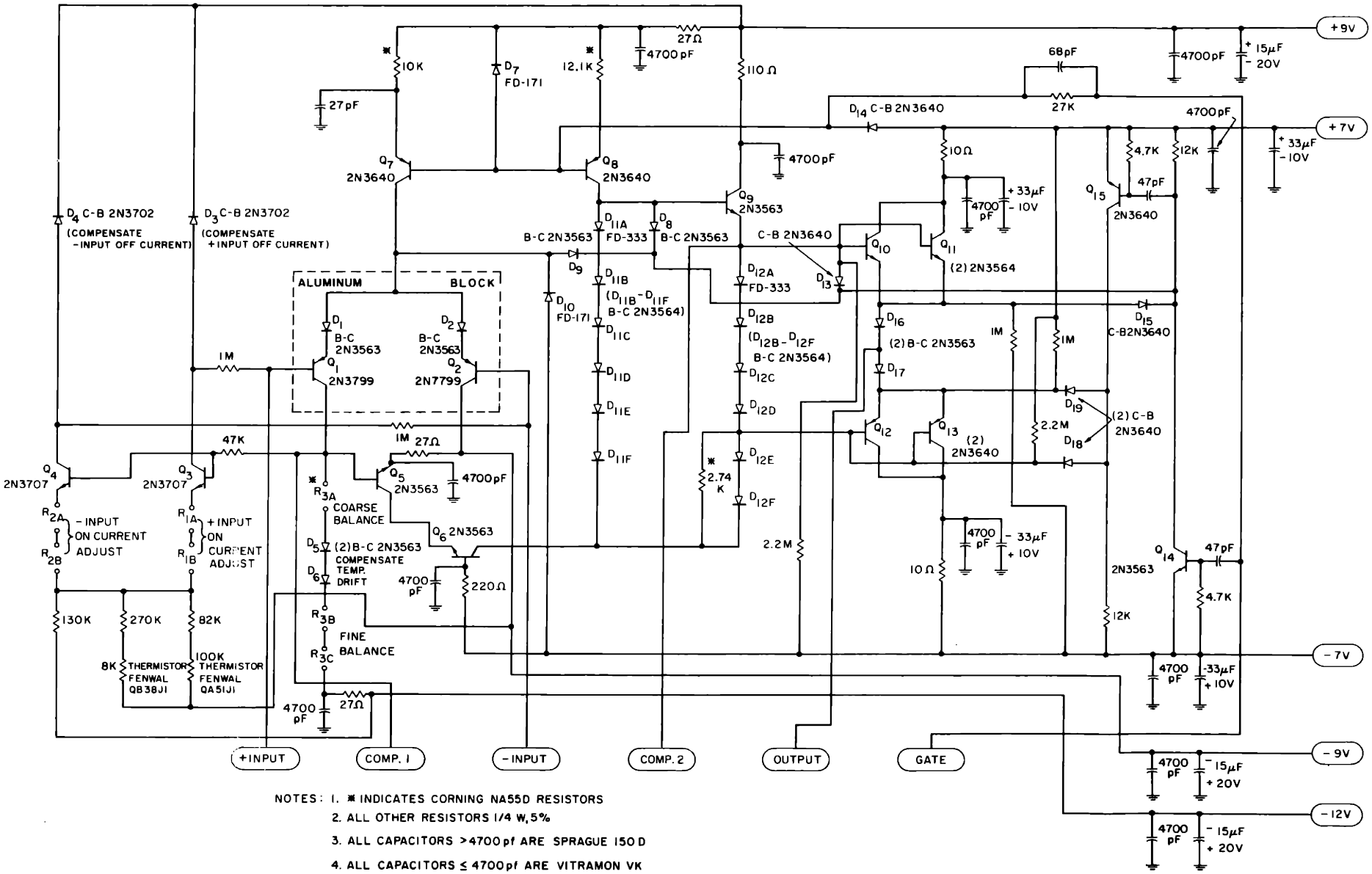
ON-state input current is compensated with transistors Q_3 and Q_4 operating as current sources. It is necessary to use current sources rather than resistors for compensation so that the compensation is independent of common-mode input level. Transistors Q_3 and Q_4 are automatically turned on and off with the amplifier by the 47-K resistor connected between the bases of Q_3 and Q_4 and the base of Q_5.

Resistors R_{1A}, R_{1B} and R_{2A}, R_{2B} located in the emitter circuits of Q_3 and Q_4 are used to adjust the magnitudes of the compensating currents. Input current compensation for temperature variation is accomplished with the network including three resistors and two thermistors. Thermistors are negative-temperature-coefficient resistors, so that the voltage across resistors R_1 and R_2 increases with decreasing temperature, and so increases compensating current.

There is no simple analytic expression which relates transistor current gain to temperature, or even any assurance that two seemingly identical transistors will display similar gain vs. temperature variations. The compensating network was designed empirically, by measuring the input current variation with temperature for six type 2N3799 transistors and matching the average variation with the network. It results in an order of magnitude reduction in input current over a 100°C temperature range.

One disadvantage of this method of compensation is evident from the figure. The thermistor network is connected to power-supply voltages continuously, and this causes a constant power consumption of 30 μW. In most applications average gated-amplifier power requirements exceed 200 μW, so the percentage attributable to this network is quite small. In certain applications requiring lower power but tolerant of higher input current, the network can be eliminated. Other possibilities which could be included in a future gated-amplifier design are those of gating the thermistor network or designing it with higher value components.

The 2N3707 was selected for use as the compensating transistor since it maintains a current gain in excess of 25 at the operating current of 0.2 μA to 0.3 μA, and because of typical leakage currents under 10^{-11} A, an important factor since these leakage currents appear as OFF-state input currents.



NOTES: 1. * INDICATES CORNING NA55D RESISTORS
2. ALL OTHER RESISTORS 1/4 W, 5%
3. ALL CAPACITORS >4700 pf ARE SPRAGUE 150 D
4. ALL CAPACITORS ≤ 4700 pf ARE VITRAMON VK

Fig. 2-18 The Complete Gated Amplifier

Diodes D_3 and D_4 are used to compensate the OFF-state input leakage currents. The 2N3702 is similar to the 2N3799 (the major difference is lower current gain), and theory predicts that the leakage currents of these devices should track quite well with temperature. This has been verified experimentally. The diodes are selected to match leakage currents of the devices they compensate and an order of magnitude improvement in OFF-state leakage currents is typically obtained.

Both the compensating diode and compensating transistor are connected to the base of the transistor they compensate through a single 1-M resistor. The resistor is included to prevent the capacitance of the two devices (15 pF) from appearing directly in parallel with an input.

Several approaches to the problem of d-c drift are evident in Fig 2-18. All critical resistors are tin-oxide types which exhibit a low (50 parts per million per degree centigrade) temperature coefficient. The first stage transistors and emitter diodes are mounted in an aluminum block to minimize temperature differences between these elements.

These precautions minimize random drift, and most of the drift referred to the input of the amplifier results from parameter changes of Q_5 with temperature. With a temperature decrease, the base-to-emitter voltage of Q_5 increases and the base current increases because current gain decreases. These effects require an increase in current into the node including the base of Q_5. A drift referred to the input would result if this current were supplied by Q_1. Diodes D_5 and D_6 can be used to supply most of the required current because of the negative temperature coefficient of diode junctions. This type of compensation results in reduction of drift referred to the input from its uncompensated value of 150 μV per degree centigrade to 10 μV to 25 μV per degree centigrade.

Numerous decoupling components are included in the amplifier schematic shown in Fig. 2-18. Two general types of decoupling are evident. Low-level points, such as the emitter of Q_5 and the base of Q_6, are decoupled to prevent power-supply noise from affecting these

nodes. High-level points, such as the collectors of Q_{10} through Q_{13}, are decoupled to prevent the large signals from entering power leads.

Many nodes are decoupled with a parallel connection of a ceramic high-frequency capacitor and a large tantalum unit. This combination provides effective isolation from low frequencies to over 100 Mc, but use of tantalum capacitors introduces one disadvantage. The leakage current of these units causes a 10 μW to 20 μW increase in OFF-state power consumption.

In order to show clearly the price paid in terms of complexity for the ability to gate an amplifier, it is convenient to construct a table which divides the 101 components shown in Fig. 2-18 into three broad categories as follows:

1. Components required in the basic operational amplifier. These are all the components shown in Fig. 2-12 with the exception of 8 diodes and 2 resistors which were included to permit gating. The total is 25.

2. Additional components required for the basic gated amplifier. These include all components added to Fig. 2-12 to form the circuit of Fig. 2-17 plus the 8 diodes and 2 resistors mentioned above. This category is effectively the price paid for the gating feature, since all other components would have to be included in operational-amplifier design with identical linear-region performance. The total is 28.

3. Components included to improve performance. This category includes all components not included in 1 or 2. As mentioned earlier, many of these components are not absolutely essential, and can be eliminated from the design in cases where degraded performance is tolerable. The total is 48.

A breakdown of the various types of components is given in Table 2-2.

This concludes the discussion of the considerations leading to the design of the gated-amplifier circuit shown in Fig. 2-18. The performance characteristics of this design are presented in Chapter III. Certain additional calculations of performance in terms of component parameters are included to show that the measured characteristics are realistic in terms of device parameters.

Table 2-2

Components Used in the Gated Amplifier

Use	Transistors	Diodes	Resistors	Capacitors	Thermistors	Total
Basic Operational Amplifier	11	9	5	0	0	25
Additional Components for Gating	2	14	8	4	0	28
Additional Components to Improve Performance	2	6	19	19	2	48
Total	15	29	32	23	2	101

CHAPTER III

AMPLIFIER PERFORMANCE CHARACTERISTICS

This chapter presents several items which, taken as a whole, indicate the performance of the six gated amplifiers that were built as part of the research program.

Simply presenting results of experimental measurements is insufficient to demonstrate all the important concepts related to a particular performance characteristic. In general four items relating to each performance characteristic are discussed. The characteristic is first defined for the benefit of readers interested in exact performance specification since there is no established standard definition for many of the characteristics. The techniques used to measure the particular quantity are usually included.(This is required since indirect measurements must be used to determine many characteristics.) The experimental results are presented, and these results are usually compared either with the analysis of Chapter II or with brief derivations included in this chapter to show that the measured characteristics are realistic in terms of device parameters.

A section is included in which comparisons between the ON-state performance of the gated amplifier and several commercially-available operational amplifiers are made. This section illustrates the performance differences which are attributable to the unique design of the gated amplifier.

A brief discussion of the reliability of the gated amplifier is also presented.

The construction technique used for the experimental gated-amplifier circuits is illustrated in Fig. 3-1. This photograph shows a top view of an assembled circuit together with the bottom view of an unassembled printed circuit board. The details of this construction technique, as well as the methods used for parts selection and the adjustments made to the amplifiers prior to measurement of performance characteristics, are described in the Appendix I.

Figure 3-2 shows one example of how gated amplifiers are interconnected to form systems. This photograph is included here since the

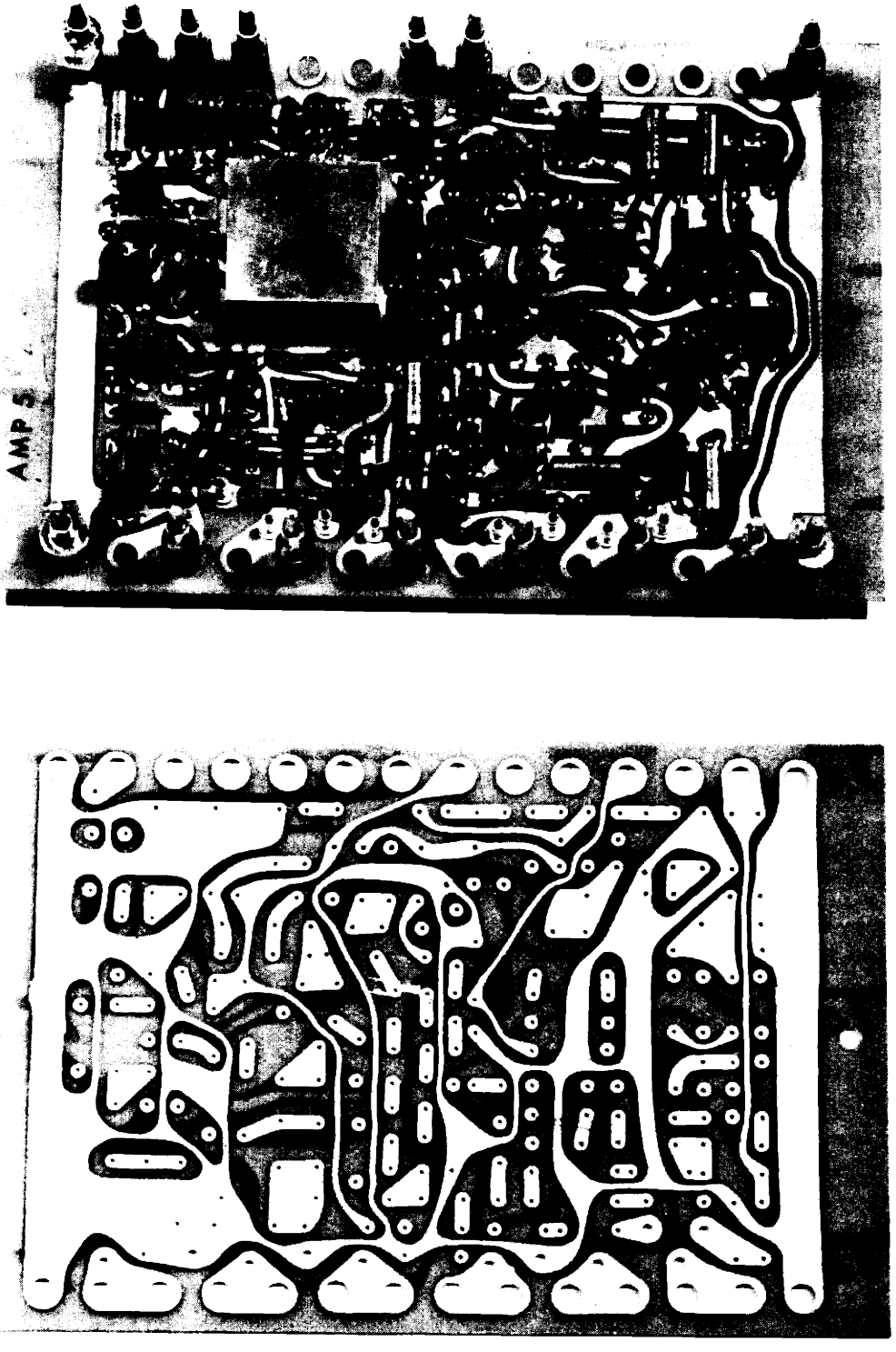


Fig. 3-1 Gated-Amplifier Circuit and Circuit Board

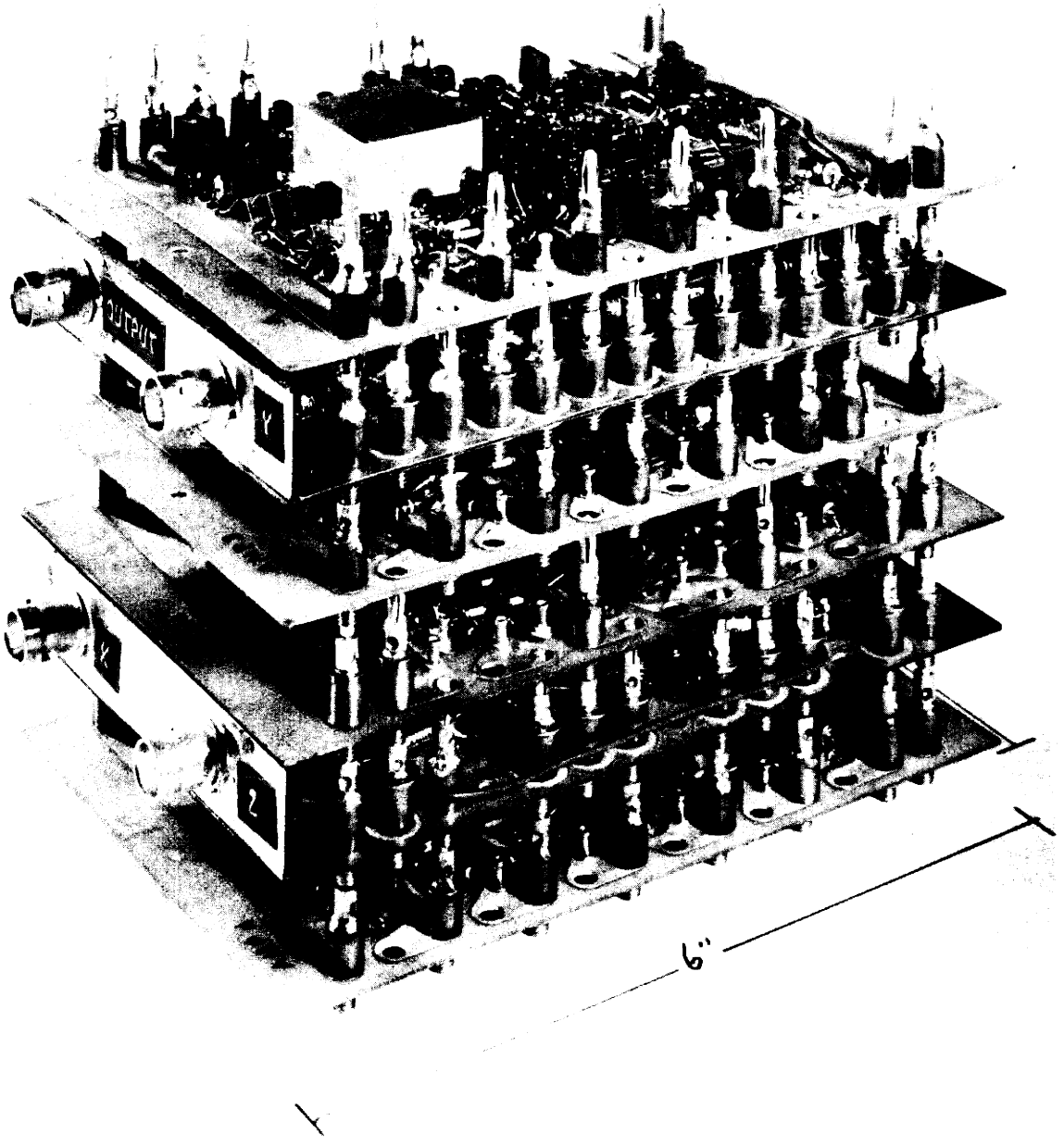


Fig. 3-2 Multiplier-Divider System

same technique was used to couple gated amplifiers to test circuits in order to measure performance characteristics. This interconnection method minimizes undesired effects such as stray capacitance, lead inductance, thermally induced voltages, and improper grounding which could lead to measurement errors.

The most important results and conclusions of this chapter are summarized in Table 3-1. This table lists measured performance characteristics of the gated amplifier. In some cases the results of several measurements made on different amplifiers are included, while in other cases typical and /or extreme values are listed. The latter method is used when inherent measurement errors preclude precise measurements. The column labeled "comments" usually indicates absolute extremes which should be achievable if a large number of the amplifiers are constructed. These predictions are based on analysis and general experience with the amplifier as well as on the measurements described in this chapter.

A. METHODS USED TO ESTIMATE THE TRANSFER FUNCTION

The ON-state transfer function of the gated amplifier for two types of loading has been predicted in Chapter II. Ideally, the transfer function should be measured by direct evaluation of open-loop gain and phase shift as a function of frequency, and the experimentally-determined transfer function compared with predicted results. Unfortunately, direct measurement is impossible (not only for the gated amplifier but in general in almost any high-gain feedback system) for several fundamental reasons:

1. Except for the simplest types of d-c inputs, open-loop measurements fail since the amplifier will not remain in its linear operating region without feedback.

2. It sould be possible to obtain open-loop gain vs. frequency by operating the amplifier closed loop and measuring the ratio of output voltage to input voltage. This approach also fails because of noise and distortion from amplifier nonlinearities.

3. The problem is also complicated by the fact that loading and noise injection inherent with many measurement techniques further distort the signals.

Table 3-1 Gated-Amplifier Characteristics

Note: All values at 25°C and with no load unless specified otherwise.

PARAMETERS	MEASURED VALUES	COMMENTS
ON-STATE CHARACTERISTICS		
D-c open-loop gain (3 amplifiers tested)	7×10^4 9×10^4 9×10^4	Component selection procedures insure minimum value of 6×10^4
Output voltage and common-mode input voltage (All amplifiers tested as part of system tests)	Minimum ± 4 volts	Insured by design parameters
Output current (All amplifiers tested)	Minimum ±200 mA Typical +450 mA, -300 mA	Component selection procedures insure minimum value of ±200 mA
Frequency of first open-loop pole, no compensation (3 amplifiers tested)	10^4 radians per second 8×10^3 radians per second 8×10^3 radians per second	
Open-loop gain at frequency at which open-loop phase shift is 180°, no compensation (4 amplifiers tested)	17 dB to 23 dB	Device characteristics insure that these are the extremes
-3 dB frequency as unity-gain, non-inverting amplifier, compensated for 3 dB resonant peak (All amplifiers tested as part of system tests)	Typical 12 Mc	Device characteristics insure extremes of 9 Mc to 16 Mc
Open-loop unity-gain frequency, no compensation (All amplifiers tested indirectly as part of system tests)	Typical 30 Mc	Extrapolated from closed-loop measurements - accuracy ± 25 percent
Common-mode rejection ratio (4 amplifiers tested)	5×10^3:1 $\quad 1.5 \times 10^4$:1 10^4:1 $\quad 10^5$:1	Device characteristics insure minimum value of 3×10^3:1
Drift referred to input (All amplifiers temperature tested as part of initial adjustment) 0°C to +50°C -25°C to +75°C vs. supply voltage variations (any voltage) vs. equal percentage change in all supply voltages	Typical / Maximum ±100 µV / ±250 µV ±300 µV / ±750 µV Maximum 0.05 volt/volt Typical 300 µV/percent	Conservative maximum values
Input current at zero input voltage, either input (3 amplifiers tested) 0°C to +50°C -25°C to +75°C vs. supply voltage	Typical / Maximum ± 5 nA / ± 10 nA ±15 nA / ±30 nA Typical 0.1 nA/mV	Conservative maximum values
Input resistance (3 amplifiers tested) Differential Common-mode	Typical 400 K Typical 200 M	Selection insures minimum differential value of 300 K Device Characteristics insure minimum common-mode value of 100 M
Equivalent input noise voltage (3 amplifiers tested)	Maximum 0.03 µV rms per root cycle per second	Conservative maximum value
Slewing rate, no compensation (All amplifiers tested as part of system tests)	Typical +15 V/µs, -60 V/µs	Circuit parameters insure typical value within ± 25 percent
Power consumption (all amplifiers tested)	Typical 15 mW Maximum 16.5 mW	Circuit parameters insure maximum value of 16.5 mW
GATING AND OFF-STATE CHARACTERISTICS		
Turn-on time (All amplifiers tested as part of system tests)	Typical 0.7 µs Maximum 1.0 µs	Depends on conditions at turn-on time Device characteristics insure maximum value of 1.1 µs
OFF-state leakage currents (All amplifiers tested as part of initial adjustment) - input + input output	Typical / Maximum 15×10^{-12}A / 5×10^{-11}A 15×10^{-12}A / 5×10^{-11}A 5×10^{-12}A / 10^{-11}A	Approximately double every 10°C above 25°C. Maximum can be reduced further by better matching
OFF-state terminal resistance (3 amplifiers tested) - input + input output	Minimum $10^{11}\ \Omega$ $10^{11}\ \Omega$ $5 \times 10^{11}\ \Omega$	Conservative minimum values
Charge dump at turn OFF (All amplifiers tested indirectly as part of system tests) - input + input output	Maximum 2.5×10^{-11} coulomb 4×10^{-11} coulomb 1.6×10^{-11} coulomb	Conservative maximum values
OFF-state power consumption (All amplifiers tested)	Maximum 60 µW	Conservative maximum value

The approach used to determine the transfer function of the gated amplifier involves the measurement of certain performance characteristics which can be related to the open-loop gain and phase over specific frequency ranges. Measurements of this type permit approximate determination of the complete transfer function as the combination of characteristics in the various ranges. Some of the more important measurement techniques are described in the following paragraphs.

The drift referred to the input of the amplifier is low enough so that d-c open-loop gain can be measured directly if these measurements are completed over a short time interval. The location of the first pole in the transfer function can also be determined by direct measurement. The compensated curves of Fig. 2-14 show that the separation between the first two poles in the transfer function is more than three and one half decades. Therefore, the rise time of the open-loop step response is controlled by the frequency of the first pole.

The frequency at which the amplifier open-loop phase shift equals -180° and the gain at this frequency can be obtained using frequency-independent, attenuative feedback. In order to make this measurement, the amplifier is connected with feedback and the feedback ratio is decreased to the smallest value that will sustain oscillation. Elementary linear-system theory shows that the frequency of oscillation under these conditions is equal to the frequency at which the open-loop phase shift is -180° and that the open-loop gain at this frequency is equal to the reciprocal of the feedback ratio.

Time- or frequency-domain measurements with various feedback ratios can be used to determine the transfer function of the amplifier in the vicinity of the cross-over frequency. For example, assume that the closed-loop frequency response is measured with a feedback ratio of 0.01. The corresponding open-loop transfer function can be evaluated with the aid of a Nichols chart, but the result is only accurate at frequencies close to that at which the open-loop gain is 100.

These types of measurements can be used to correlate measured and predicted behavior, and the details of this correlation are explained in the following two sections.

B. MEASUREMENTS WITH HIGH-IMPEDANCE LOAD

Four types of measurements which were made on gated amplifiers with high-impedance loads are discussed in this section. The measurements and the reasons for selecting these particular measurements are listed below:

1. The amplifier open-loop gain and the location of the first pole in the uncompensated transfer function were measured directly. These results can be used to estimate the open-loop transfer function at low frequencies.

2. The step response of the amplifier connected for a non-inverting gain of 100 was measured. These results can be used to estimate the uncompensated transfer function near the frequency at which the open-loop gain is 100. A further reason for discussing this connection is that it is used for several other tests.

3. The frequency at which the uncompensated open-loop phase shift equals -180° was measured. This measurement yields information about the transfer function near the frequency at which the open-loop gain is 10.

4. The frequency response of a compensated amplifier connected for a non-inverting gain of one was also measured. These results show how compensation modifies the open-loop transfer function of the gated amplifier. This connection is often used in the applications described in Chapter IV.

The predicted transfer function with a high-impedance load and no external compensation is shown as the curves labeled "compensated" in Fig. 2-14. (These curves include the effects of the 1.5-pF stray compensating capacitance that is present in the prototype circuits). These curves show that the dominant pole in the transfer function is located at approximately 9×10^3 radians per second and that all other singularities are located at least three and one half decades beyond this frequency. The d-c gain predicted by this figure is 7.5×10^4. Therefore, the predicted open-loop response to a step of amplitude A_o is $7.5 \times 10^4 A_o (1 - e^{-t/1.08 \times 10^{-4}})$.

Three amplifiers were tested by applying 50-μV steps. The measured responses are tabulated below.

Amplifier	One-time-constant rise time (seconds)	Gain
1	10^{-4}	7×10^4
2	1.2×10^{-4}	9×10^4
3	1.2×10^{-4}	9×10^4

Three amplifiers were also tested with feedback that provides a non-inverting gain of 100. Figure 3-3 illustrates this connection and also shows the notation used for all circuits that include gated amplifiers.* Positive-and negative-gain input terminals are indicated by plus and minus signs. The compensating terminals are located toward the top of the amplifier, and are left open but not omitted if no compensation is used. The gate lead is indicated by the symbol Γ enclosed by the amplifier, and is grounded to turn the amplifier ON.

The gain-of-100 amplifier is realized with a feedback network which provides 40 dB of frequency-independent attenuation. No compensating capacitor is used in this application. An approximate block diagram for this connection is shown in Fig. 3-4. There is a second forward path (not shown) because of coupling from the positive-gain input of the amplifier directly to the base of Q_5 through the collector-to-base capacitance of transistor Q_1. (Fig. 2-18). It can be shown, however, that the effect of this path is negligible for the particular configuration illustrated in Fig. 3-3.

The Bode plot of Fig. 2-14 shows that with -40 dB of gain in a feedback network, the cross-over (or unity-gain) frequency for the amplifier-feedback network combination should be 7×10^6 radians per second. The slope of the gain curve at crossover is -6 dB per octave, and this slope is maintained at frequencies from $\frac{1}{700}$ of the cross-over frequency

*Capitol E's are used for voltages in the block diagrams of this chapter and Chapter IV. These variables maybe either functions of time or of complex frequency. All system voltages are referenced to the amplifier power-supply ground unless indicated otherwise.

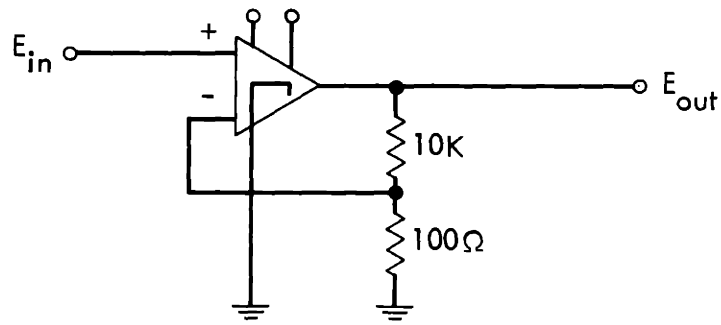


Fig. 3-3 Gated Amplifier Connected as Gain-of-100, Non-Inverting Amplifier

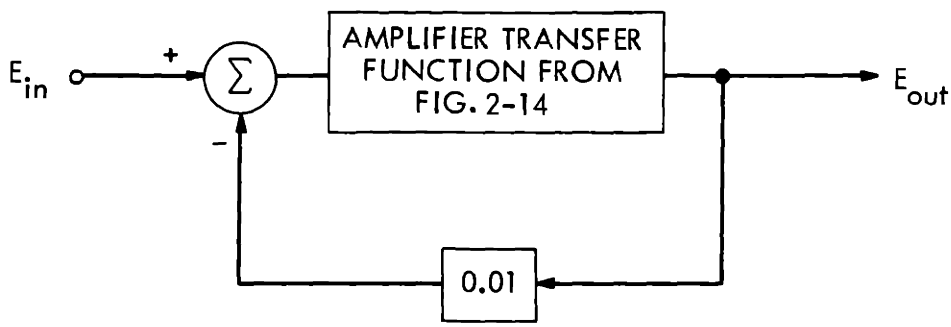


Fig. 3-4 Block Diagram for Gain-of-100, Non-Inverting Amplifier

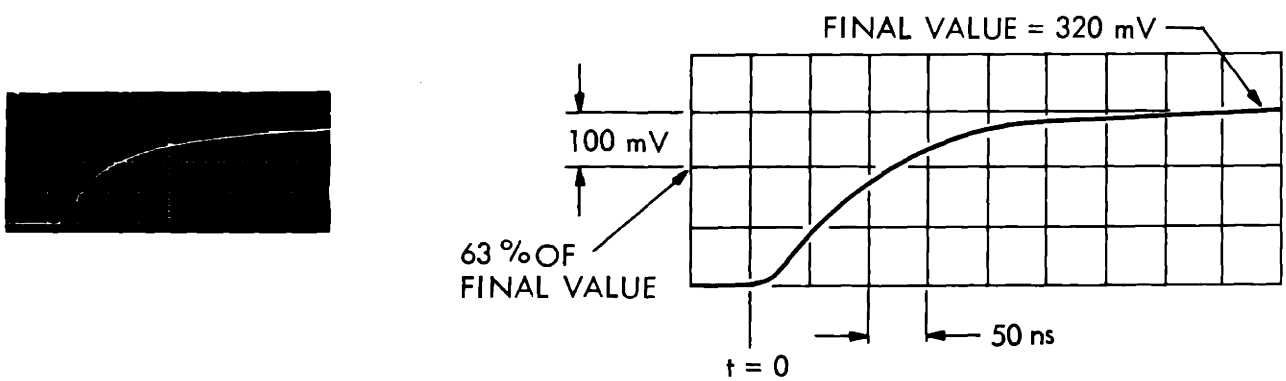


Fig. 3-5 Step Response for Non-Inverting gain-of-100 Amplifier – Input = 3.2 mV

to 8 times the cross-over frequency. Furthermore, the phase margin at crossover exceeds 75°. Linear-system theory shows that the step response of the amplifier under these conditions should be indistinguishable from that of a similarly connected amplifier with an open-loop transfer function equal to $\frac{7 \times 10^6}{s}$.

The transfer function of the non-inverting gain-of-100 amplifier is $\frac{100}{1.4 \times 10^{-7} s+1}$ if this approximation is used for the open-loop gain. The amplifier should therefore exhibit a step response which is a first order with a one-time-constant rise time of 140 ns. The three amplifiers which were tested with this type of feedback all displayed essentially identical responses typified by the oscilloscope photograph shown as Fig. 3-5. The photograph shows a somewhat delayed start compared to a true exponential because of additional poles in the transfer function. The one-time-constant rise time from this photograph is 120 ns.

Another test was performed to determine the frequency at which the open-loop phase shift is -180° and the gain at this frequency. Figure 2-14 shows that the amplifier phase curve passes through -180° at $\omega = 6 \times 10^7$ radians per second, and that the amplifier open-loop gain at this frequency is 20 dB. Thus, if frequency-independent attenuative feedback is used, the amplifier should oscillate at 6×10^7 radians per second with a -20-dB feedback network.

In order to verify this oscillation condition, two compensated attenuators were constructed with attenuations of 17 dB and 23 dB. These attenuators are resistive dividers which are padded with capacitors (taking into consideration the amplifier input capacitance) in order to yield frequency-independent attenuation when connected to the amplifier. Four amplifiers were tested. All oscillated at frequencies from 5×10^7 radians per second to 6×10^7 radians per second with the 17-dB network; none oscillated with the 23-dB network.

The unity-gain non-inverting connection, shown in Fig. 3-6 is of particular interest because of frequent use in applications. In order to obtain a well-damped transient response with unity feedback it is necessary to use a 22-pF compensating capacitor. The reason for the 150-pF load capacitor is explained below. The analysis of Chapter II, Section M,

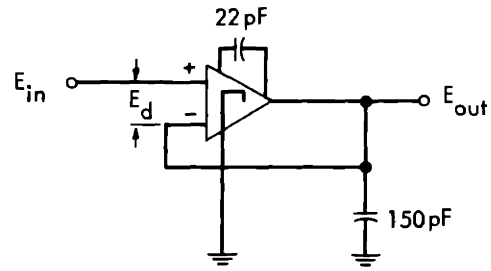


Fig. 3-6 Non-Inverting Gain-of-1 Amplifier

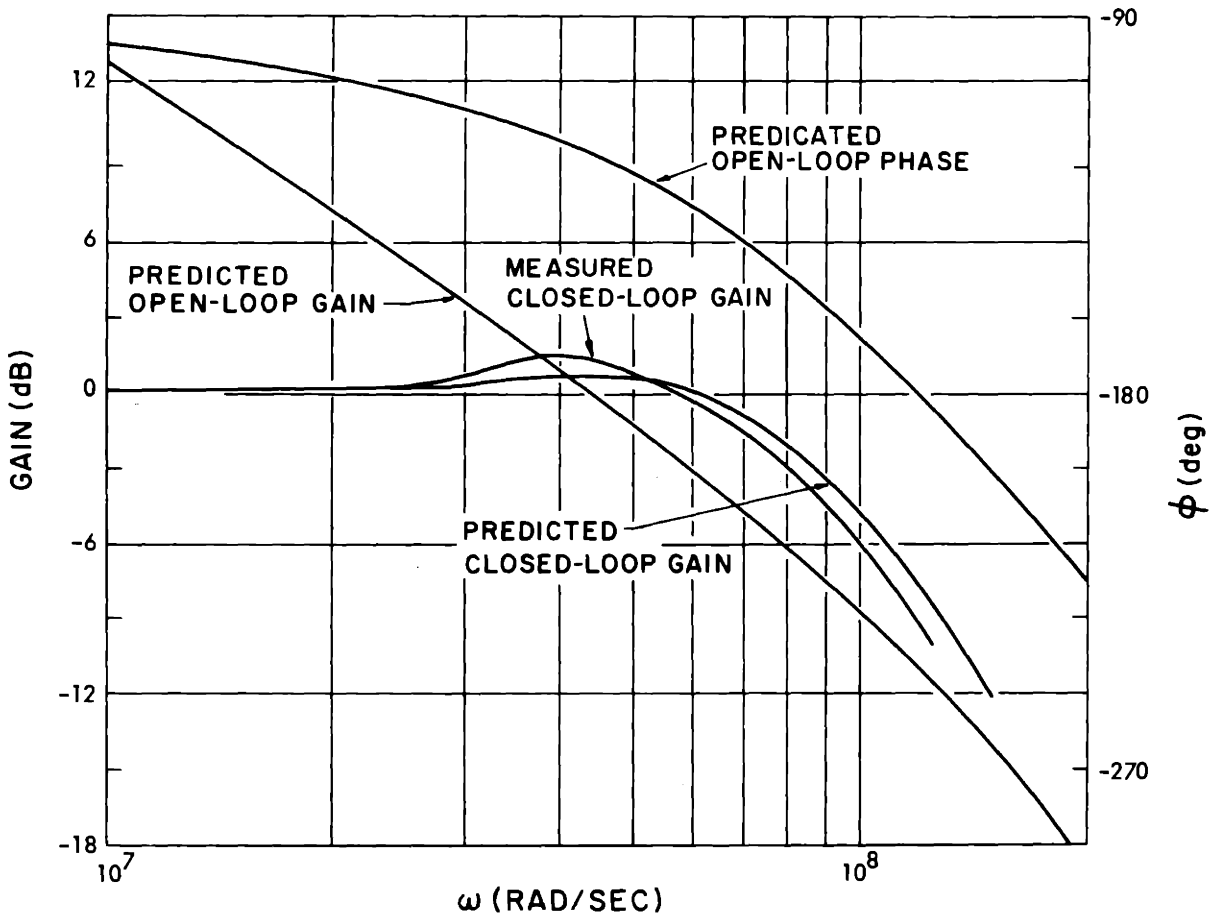


Fig. 3-7 Predicted and Actual Gain vs. Frequency for Non-Inverting Gain of 1 Amplifier

shows that the amplifier open-loop transfer function with a 22-pF compensating capacitor is

$$\frac{E_{out}}{E_d} = \frac{7.5 \times 10^4}{(1.65\times10^{-3}s+1)(2.2\times10^{-9}s+1)^2(5\times10^{-9}s+1)(3.2\times10^{-9}s+1)(8\times10^{-10}s+1)}$$

An accurate Bode plot of this function in the vicinity of the unity-gain frequency is shown in Fig. 3-7 as the curves labeled "predicted open-loop gain." The curve labeled "predicted closed-loop gain," which was obtained with the aid of a Nichols chart, indicates the expected frequency response for the amplifier shown in Fig. 3-6. The measured frequency response for the amplifier illustrated in Fig. 3-6 (including the load capacitor) is also shown in Fig. 3-7. This curve was obtained by direct measurement with a 50-mV peak-to-peak input signal.

If this amplifier is tested without the 150-pF load capacitor connected, a rather strange transient condition is observed. If a step with a rise time of less than 10 ns is applied to the amplifier, the basic structure of the response is consistent with the plotted frequency response, but a high-frequency component is superimposed on the transient. The frequency of this component varies from 30 Mc to 100 Mc depending on the actual test configuration used. The predicted closed-loop response shows that no transient should contain any significant components beyond approximately 10^8 radians per second, since the closed loop-gain should be less than -6 dB at all frequencies above this.

It is not possible to demonstrate the reason for this ringing with the analysis of Chapter II, but additional investigation indicates that several factors contribute to it:

1. The instrumentation is involved. This is quite easy to demonstrate, since the type of ringing present on the transient can be drastically altered by changing ground connections, "hand waving" in the vicinity of the pulse generator (not the amplifier), touching any part of the system ground, etc. Furthermore, the ringing is present between two separate points in the ground system. The ringing becomes smaller if a one-shot multivibrator, constructed on an interface board and

mounted in close proximity to the amplifier, is used as the pulse source, since this reduces the length of ground connections.

2. The output lead inductance is also involved.

3. The ring frequencies are, in many cases, above the gain-bandwidth product of the transistors used in the output stage, and it is known that this leads to modes of operation not predictable from the transistor model used. Furthermore, any transient large enough to be observed changes the emitter resistances of these transistors drastically.

While this ringing causes no severe problems (an actual instability has never been observed), it is somewhat annoying. It can be eliminated by connecting a small capacitor to the output. This capacitor reduces gain at the ringing frequencies, but does not change performance at lower frequencies. A 150-pF capacitor at the amplifier output is used routinely in system design.

This concludes the discussion of tests which were performed on the amplifier with high-impedance load. The measurements indicate that predicted and measured performance agree under all conditions tested.

C. MEASUREMENTS WITH LARGE CAPACITIVE LOAD

Gated amplifiers are frequently used in sampling applications, and a large capacitive load is connected to the amplifier in these applications. The performance of the amplifier with a load consisting of a 1-μF capacitor in series with a 2.7-Ω resistor and with a 15-pF compensating capacitor is predictable from Fig. 2-16, the amplifier open-loop transfer function under these conditions. The amplifier connection which is used is shown in Fig. 3-8.

The open-loop transfer function predicted in Chapter II, Section O, for the amplifier with this load and compensation is

$$\frac{E_{out}}{E_d} = \frac{7.5\times10^{4}(2.7\times10^{-6}s+1)}{(7.5\times10^{-3}s+1)(3.75\times10^{-5}s+1)}$$

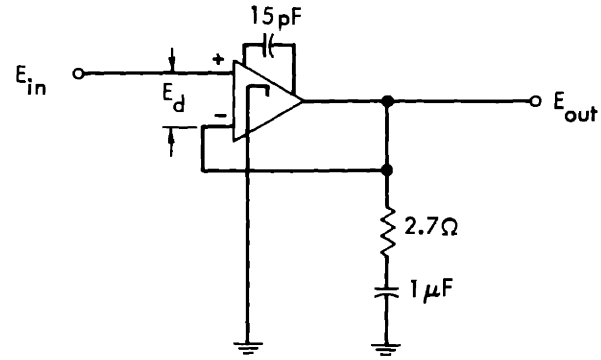


Fig. 3-8 Non-Inverting Unity-Gain Amplifier with Large Capacitive Load

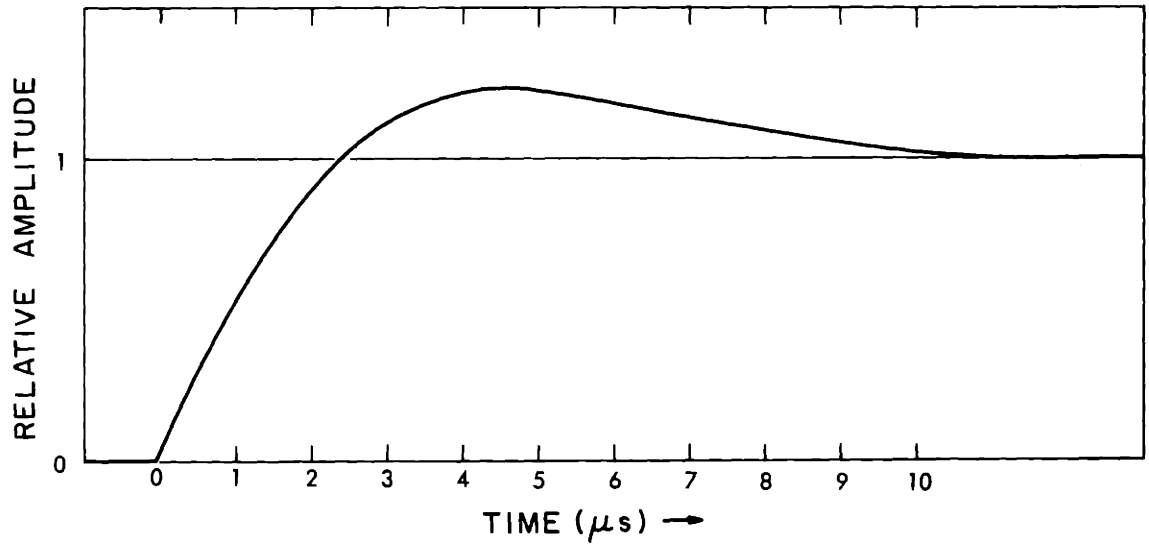


Fig. 3-9 Predicted Step Response for the Circuit of Fig. 3-8

With unity feedback as shown in Fig. 3-8, the corresponding closed-loop transfer function is

$$\frac{E_{out}}{E_{in}} = \frac{2.7 \times 10^{-6}s+1}{3.75 \times 10^{-12}s^2 + 2.8 \times 10^{-6}s+1}$$

The characteristic equation is second order with a natural frequency of 5.15×10^5 radians per second and a damping ratio of 0.7. This transfer function is easily evaluated in the time domain, and the predicted response to a unit step is shown in Fig. 3-9.

The oscilloscope photograph of Fig. 3-10 shows the measured response of the amplifier to a 400-μV step input. This input amplitude is small enough to insure linear-region operation, and it can be seen that Fig. 3-10 agrees with the predicted step response.

Figures 3-11a through 3-11d indicate the variations in step response as the signal amplitude is increased, and these follow the general relationship predicted in Chapter II. The step response of the amplifier displays a shorter rise time and better damping as a result of the gain increase (in a describing-function sense) associated with large signals. Note that the amplifier rise time decreases from 4 μs at small signal levels to less than 200 ns when a 0.4-volt step is applied.

Figure 3-11d shows the response of the amplifier to a 4-volt step input. Current limiting is evident in this figure. The amplifier output voltage increases rapidly to approximately 1.5 volts, and during this time interval the capacitor voltage remains zero. Therefore the output current is 1.5 volts divided by 2.7 Ω or 500 mA. This value is consistent with the slope of the curve (0.5 volt per microsecond) following the initial rise. The output current decreases slightly as the output voltage approaches +4 volts since the current gain of the output transistors decreases as the collector-to-emitter voltage becomes smaller. Under similar drive conditions, a negative step input results in somewhat lower output current (300 mA) as predicted in Chapter II.

The photographs shown in Figs. 3-10 and 3-11 indicate that the amplifier response remains well damped for inputs which cause the current in the output transistors to increase as much as three and one

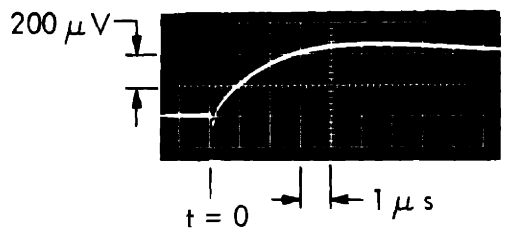


Fig. 3-10 Measured Response of Circuit of Fig. 3-8 to 400- μV Step

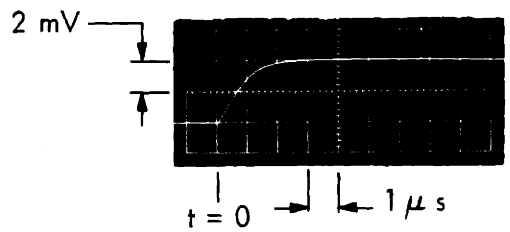


Fig. 3-11a 4-mV Step Input

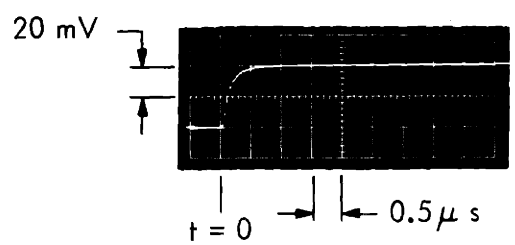


Fig. 3-11b 40-mV Step Input

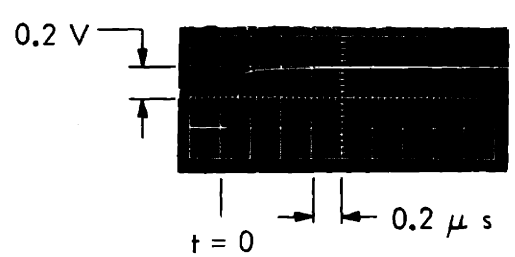


Fig. 3-11c 0.4-V Step Input

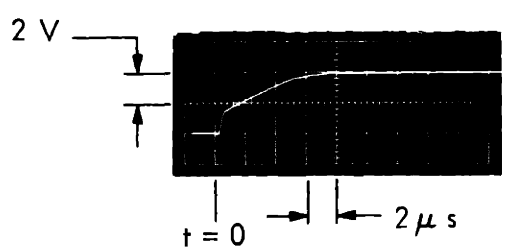


Fig. 3-11d 4-V Step Input

Fig. 3-11 Measured Response of Circuit of Fig. 3-8 to Large Steps

half decades from its quiescent value. This type of response to any possible input signal is the reason for choosing the particular form of compensation used with large capacitive loads.

The measurements presented in the photographs are somewhat difficult to make because step inputs in excess of 500 μV cause significant deviation from linear-region behavior. The only high-gain oscilloscope preamplifier available at the time of the tests had a maximum sensitivity of 1 mV per cm, and at this sensitivity the bandwidth is only 0.3 Mc, a value insufficient for required measurements. This problem was circumvented by using a gated amplifier connected for a non-inverting gain of 100 as a preamplifier. The bandwidth in this connection exceeds 1 Mc which is adequate.

There is some leading-edge ringing evident in Fig. 3-11b, and this arises from grounding problems. The ringing is also present for the lower level inputs, but the limited bandwidth of the gain-of-100 amplifier prevents its observation. For Fig. 3-11b and subsequent photographs, the signal amplitude was large enough so that the gain-of-100 amplifier could be eliminated.

The last two sections of this chapter have indicated the results of tests which were used to determine the gain vs. frequency characteristics of the gated amplifier under certain conditions. Two important results are evident from these experiments:

1. The measured and predicted amplifier characteristics agree, at least under the conditions tested. It is concluded that the method of analysis used, which admittedly involved a number of approximations, adequately models the amplifier in the ON state and can be used as an aid to selecting compensation for varying conditions of load and amplifier closed-loop gain.

2. The amplifier can be compensated to provide stable, well-damped performance under varying conditions of load and closed-loop gain. This feature is of paramount importance so that the amplifier can be easily tailored for use in many applications.

D. DRIFT REFERRED TO THE INPUT

The voltage drift referred to the input limits the accuracy of any d-c amplifier. The drift referred to the input of the gated amplifier in the ON state is defined in terms of the following experiment. The amplifier is operated open loop with both inputs grounded, and is initially balanced so that the output is also at ground potential. Some operating condition such as temperature or supply voltage is changed and as a result of this perturbation the output voltage changes. A d-c signal is applied to either input, and the magnitude of this signal adjusted until the output is again equal to zero volts. The magnitude of the input signal is then by definition the drift referred to the input.

A more practical technique which can be shown to yield an identical value involves operating the amplifier at some high closed-loop gain (the non-inverting gain-of-100 connection shown in Fig. 3-3 was used for tests). The drift referred to the input is obtained by dividing the measured change in output voltage by the closed-loop gain.

Manufacturers often specify drift referred to the input vs. temperature on a per-degree-centigrade basis, but such specification is somewhat ambiguous. The actual variation cannot be measured accurately for small temperature variations, and for this reason the specified figure is obtained by dividing the difference in drift at two temperatures which differ by a large amount by the temperature change. This measurement procedure is questionable, since drift and temperature are not necessarily linearly related over the temperature range used for the measurement.

A measurement technique which circumvents this shortcoming is used for stating gated-amplifier drift. The temperature is slowly changed from $-25^{\circ}C$ to $+75^{\circ}C$, and the maximum drift referred to the input measured for the two temperature ranges of $-25^{\circ}C$ to $+75^{\circ}C$ and $0^{\circ}C$ to $+50^{\circ}C$. These two values are presented directly and assure the system designer of a maximum drift figure over a particular temperature range.

The drift referred to the input vs. temperature was measured for all six of the amplifiers, since this measurement is necessary for temperature compensation. All amplifiers displayed a curve with the general characteristics shown in Fig. 3-12. The curve is symmetrical

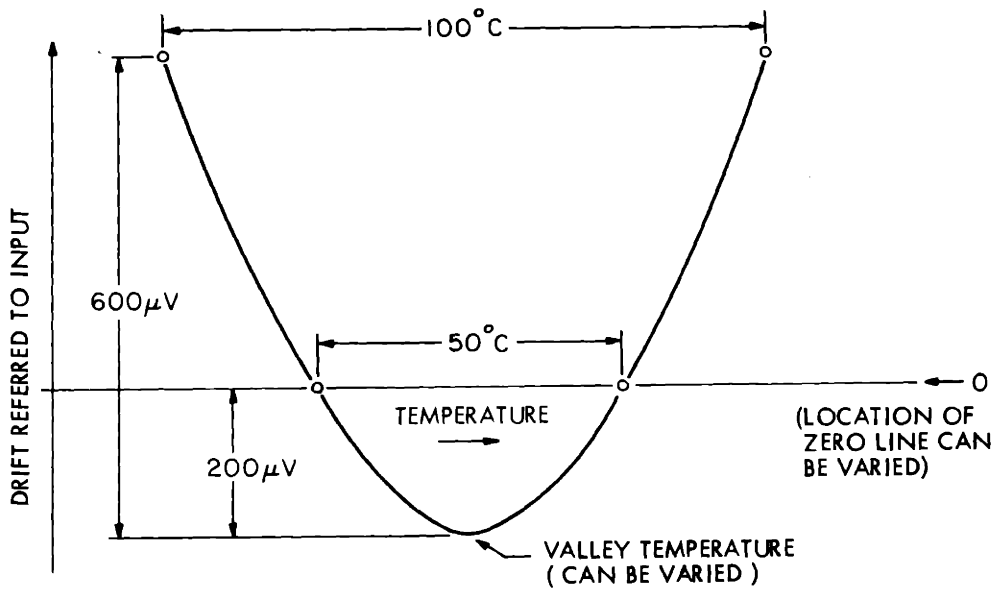


Fig. 3-12 Typical Gated-Amplified Drift Referred to the Input vs. Temperature

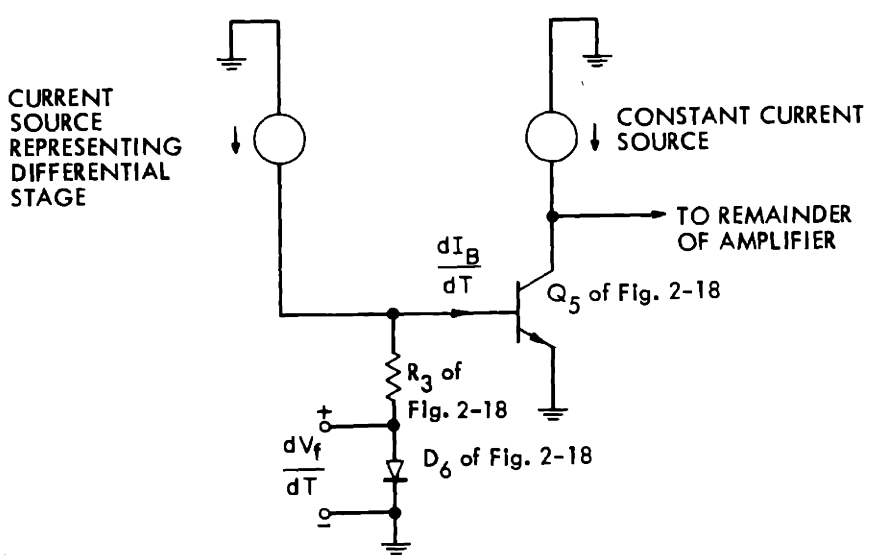


Fig. 3-13 Model for Drift Mechanism

and approximately parabolic about a temperature which I call the valley temperature, and this type of variation results from the temperature compensation used in the amplifier. This curve is explained with reference to Fig. 2-18. Because of the balancing technique used with the first stage, nearly all of the amplifier drift arises from variations in operating point of transistor Q_5 with temperature. Assume that the voltage across diode D_5 in Fig. 2-18 is exactly matched to the base-to-emitter voltage of Q_5. As a result, the temperature coefficient of these junctions will be matched, since the temperature coefficient of a silicon junction operating at constant current is related to the forward voltage by

$$\frac{dV_f}{dT} = \frac{V_f - 1.2}{T} \quad \text{at}$$

temperatures of interest. In this equation, V_f is the forward voltage of the diode or transistor junction and T is the absolute temperature. (The assumption of equality of diode and transistor junction voltage is not essential but does simplify the development without altering any essential features.)

With this simplification, the drift mechanism can be modeled as shown in Fig. 3-13. Since it has been assumed that variations in base-to-emitter voltage of Q_5 are matched by those of D_5, the transistor shown in Fig. 3-13 is assumed to have zero base-to-emitter voltage. The resistor shown in Fig. 3-13 represents $R_{3A} + R_{3B} + R_{3C}$ in Fig. 2-18. It can be seen from Fig. 3-13 that the condition for zero drift is that

$$\frac{1}{R} \frac{dV_f}{dT} = \frac{dI_B}{dT}$$

If the gain of the first stage is considered, the rate of change of drift with temperature is

$$\frac{dE_{drift}}{dT} = -1000 \left(\frac{1}{R} \frac{dV_f}{dT} - \frac{dI_B}{dT}\right)$$

The characteristic drift curve shown in Fig. 3-12 can be explained from this equation. The value of R is typically 30 K and the temperature

coefficient of the diode is typically -1.6 mV/°C, and this coefficient is temperature independent. This combination results in perfect temperature compensation if $\frac{dI_B}{dT} \approx -0.054$ μA per degree centigrade.

The variation in base current with temperature for a transistor operating at constant collector current cannot be easily predicted from transistor parameters, but measurements indicate that $\frac{dI_B}{dT}$ is always negative and that the magnitude of this quantity generally decreases with increasing temperature. In the example illustrated by Fig. 3-12, the valley temperature is the temperature at which $\frac{dI_B}{dT} = 0.054$ μA/°C. At higher temperatures, the magnitude of $\frac{dI_B}{dT}$ becomes smaller, resulting in a positive slope for the drift vs. temperature curve shown in Fig. 3-12, while at lower temperatures the magnitude of $\frac{dI_B}{dT}$ becomes larger, resulting in a negative slope.

For a particular transistor, the valley temperature can be changed by changing the diode forward voltage and thus its temperature coefficient. A diode with a lower temperature coefficient yields a higher valley temperature. In practice, the valley temperature is adjusted to equal the expected operating temperature, so that variations in temperature cause minimum drift variation.

The actual value of drift referred to the input at any temperature can also be varied by changing R_3 in Fig. 2-18, and this is adjusted so that equal positive and negative drifts are obtained over the expected operating temperature range.

The six amplifiers were compensated for valley temperatures close to 25°C. The curve shown in Fig. 3-12 (which is an averaged curve from all six amplifiers) shows that with this valley temperature the maximum magnitude of the drift referred to the input can be limited to less than ±100 μV over a 0°C to +50°C range and to less than ±300 μV over -25°C to +75°C range.

Absolute maximum limits, which include variations in the valley temperatures of the amplifiers, variations from amplifier to amplifier because of differences in transistor characteristics, and an allowance for measurement uncertainties are ±250 μV from 0°C to +50°C and ±750 μV from -25°C to +75°C.

Another important component of input drift arises from changes in supply voltages. The critical changes are the difference between the

-9 volt and -12 volt supplies and the difference between the +7 volt and +9 volt supplies. A change of ΔV_1 in the difference between the -9 volt and -12 volt supplies will result in a change in current through R_3 in Fig. 2-18 of $3 \times 10^{-5} \Delta V_1$. The input voltage change required to compensate for this change is $(4r_{e1})$ $(3 \times 10^{-5} \Delta V_1)$ or $0.03 \Delta V_1$ since $r_{e1} \approx 250\ \Omega$. Therefore, the coefficient relating input drift to individual changes in either the -9 volt or -12 volt supply is 0.03 volt/volt. A similar calculation predicts a sensitivity to changes in either the +7 volt or +9 volt supply of 0.05 volt/volt. These sensitivities have been experimentally verified to within measurement errors.

These figures are higher than might be desired. For example, in order to keep input drift because of power-supply variations equal to typical temperature drift over a $0^{\circ}C$ to $+50^{\circ}C$ temperature range, the power supply voltages must be stable to ±2 mV or less. While designing a supply with this stability is possible, it is somewhat difficult.

There is one additional factor in the gated-amplifier design which relaxes this requirement. Typically, multiple-voltage power supplies are constructed using a single reference element and a number of regulators. The regulators themselves can be made to exhibit very low drift but the reference element (normally, at least in a space system, a zener diode without a temperature-stable enclosure) is relatively unstable.

The usual result of a reference-voltage variation is an equal percentage variation in all output voltages. This type of voltage variation cancels quite effectively in the gated-amplifier circuit. A typical value for drift referred to the input for equal percentage variation in all supply voltages is 300 μV/percent. Thus power supply reference stability to 0.3 percent, which is readily available, reduces input drifts from this cause to less than 100 μV.

E. INPUT CURRENT AND INPUT RESISTANCE

ON-state input current is compensated by transistors Q_3 and Q_4 (Fig. 2-18) and the compensation is varied with temperature by means of a thermistor network. The difference between the current required by the input transistors and that supplied by the compensating transistors is the input current.

Input current at zero input voltage is measured by connecting a large feedback resistor between the amplifier output and the negative-gain input. The current at the positive-gain input can then be measured directly with a low-impedance electronic ammeter. The output voltage is equal to the negative-gain input current multiplied by the feedback resistor.

The input-current variation with temperature was measured for three amplifiers. These measurements show that typical input current at either input is limited to ±5 nA over the temperature range of $0^{\circ}C$ to $+50^{\circ}C$, and to ±15 nA over the $-25^{\circ}C$ to $+75^{\circ}C$ range. Maximum input currents, which include variations from amplifier to amplifier and an allowance for measurement uncertainties, are twice typical values.

Uncompensated input current to Q_1 or Q_2 is approximately 250 nA, and measurements indicate that this value changes from 450 nA at $-25^{\circ}C$ to 150 nA at $+75^{\circ}C$. Thus the temperature compensation reduces the measured variation to approximately 10 percent of its uncompensated value.

Input current also changes because of changes in supply voltage. These changes are on the order of 0.1 nA per mV of supply voltage change, and therefore are negligible in most applications.

One further input-current component arises from finite amplifier input resistance. The input resistance consists of two terms, a resistance between the bases of Q_1 and Q_2 equal to $4\beta_1 r_{e1}$, and a resistance from either base to ground equal to r_{c1}. (Both input transistors are assumed identical.) The inter-base resistance of approximately 400 K contributes negligibly to input current, since the voltage across this resistance must be less than 0.1 mV when the amplifier is operating linearly. The resistance from either base to ground can contribute a significant input current, however, since any input common-mode voltage appears across this resistance. Measured values range from 150 M to 300 M so that an additional input-current component as high as 25 nA can result from this effect.

F. COMMON-MODE REJECTION RATIO

The common-mode rejection ratio is by definition the ratio of the amplifier open-loop gain observed for a differential signal (the two amplifier inputs are supplied with equal-magnitude, opposite-polarity signals) to the amplifier common-mode gain (both inputs are supplied with identical signals). A finite common-mode rejection ratio causes errors when an amplifier is operated with signals applied to both inputs.

The common-mode rejection ratio can be calculated by computing the net change in current introduced at the node including the base of Q_5 as a result of applying a common-mode signal and multiplying this current by $4r_{e1}$ to determine the differential input signal required to offset the common-mode signal. The ratio of common-mode signal to differential signal is the common-mode rejection ratio. Since linearity is assumed for purposes of calculation, any common-mode signal can be chosen, and one volt is used for convenience.

A one-volt common-mode input increases the current into the base of Q_5 by $\frac{1}{r_{c1}}$ amp due to the collector-to-base resistance of Q_1. The collector current of Q_7 is reduced by $\frac{1}{r_{c7}}$ amp and one half this change appears at the node including the base of Q_5. The change related to the reverse generator of Q_7 is negligible. One further source of common-mode gain arises from non-equal reverse generators of transistors Q_1 and Q_2. In the experiment where one volt is applied to the bases of Q_1 and Q_2, the current change introduced at the node including the base of Q_5 is $\frac{(\mu_1 - \mu_2)}{4r_{e1}}$.

The two predominant effects are those related to the collector-to-base resistance of Q_7 and to nonequal magnitudes of the Q_1 and Q_2 reverse generators. The collector-to-base resistance of Q_7 is typically 5 M, and a one-volt positive common-mode input decreases the current at the node including the base of Q_5 by 0.1 μA because of this resistance. The magnitude of the reverse-generator coefficient, μ, for six 2N3799's was measured under conditions approximating those of the gated-amplifier circuit. The minimum and maximum values observed were 2×10^{-4} and 4×10^{-4}. This range of values contributes a current change of either polarity of at most 0.2 μA for a one-volt common-mode input signal.

It is concluded that the minimum ratio of differential gain to common-mode gain should be 3×10^3 (since $4r_{el} = 1$ K). Four amplifiers were tested by first measuring differential open-loop gain (as explained earlier in this chapter), and then dividing by the common-mode open-loop gain (measured by an analogous method). The measured rejection ratios were 5×10^3:1, 10^4:1, 1.5×10^4:1 and 10^5:1.

G. EQUIVALENT INPUT NOISE VOLTAGE

The noise inherent to an amplifier can be specified in various ways. It will be shown that the most useful quantity in the case of the gated amplifier is the equivalent input noise voltage.

The noise voltage is defined as follows. Assume that an amplifier with a gain G and an effective noise bandwidth of W is tested with both inputs grounded. A noise-voltage source that produces white, gaussian noise with an amplitude equal to A_o volts rms per root cycle per second is connected to the input, and the amplitude is adjusted until the noise at the output of the amplifier increases by 3 dB. The magnitude of A_o is then the equivalent input noise voltage.

It can be shown that the value can also be obtained as $A_o = \frac{N_o}{G\sqrt{W}}$, where N_o is the rms voltage measured at the amplifier output with the inputs grounded. Noise measurements were made operating the amplifier open loop, and under these conditions the transfer function of the amplifier is approximately $\frac{8 \times 10^4}{10^{-4}s+1}$ (see Section B of this chapter). The effective noise bandwidth for the transfer function $\frac{1}{\tau s+1}$ is $\frac{1}{4\tau}$. Therefore, the equivalent input noise voltage per root cycle per second is the rms output voltage divided by 4×10^6.

The output noise voltage could not be measured directly with an rms volt meter because of a large component located at the power-line frequency. This component results from improper shielding and is obviously not attributable to the amplifier itself. The "quasi" peak-to-peak value, exclusive of the component at the line frequency, was measured by using an oscilloscope triggered from the line and observing the output noise with a rapid time sweep. It is generally agreed that the value measured this way is five to six times the rms value. Based on

this relationship, the equivalent input noise voltage measured for three amplifiers was less than 3×10^{-8} volt rms per root cycle. (This figure includes a factor for measurement uncertainty.)

Actually, this figure is somewhat pessimistic. The noise generated by the amplifier is not flat in the frequency band covered by this experiment. Furthermore, the noise will be lower in any equivalent-width frequency band located at higher frequencies, since transistor 1/f noise predominates in the frequency spectrum covered in this experiment.

The equivalent input noise voltage can be converted to an equivalent noise resistance; that is, the value of an ideal resistor which would supply the same noise voltage at room temperature. The value of this equivalent noise resistance is 50 K for the gated amplifier. Since gated amplifiers are never used with source resistances in excess of 5 K in normal applications, the equivalent input noise voltage of the amplifier will always predominate over any noise voltage contribution from source impedances. Therefore it is possible to state that in any intended gated-amplifier application the equivalent input noise voltage will be less than 3×10^{-8} volt rms per root cycle.

H. GATING CHARACTERISTICS

Three characteristics related to gating are discussed in this section. These include:

1. Turn-on time
2. Turn-off time and charge dump
3. OFF-state terminal currents and resistances.

A gating pulse that switches from +9 volts to ground (ON) or ground to +9 (OFF) in less than 10 ns was used for all tests.

A maximum turn-on time (time for the amplifier to become active following application of a turn-on pulse) of 1.1 μs was predicted in Chapter II. This estimation involved calculation of the charge required to bring certain amplifier nodes to the voltages necessary for active operation, and indicated that the turn-on time should be a function of applied voltages at the time of gating. The amplifiers have been tested

in many configurations as part of system tests, and observed turn-on times never exceed 1 μs, with a typical value of 0.7 μs. Furthermore, a high degree of uniformity in this parameter exists among various amplifiers. With identical feedback networks and initial conditions, the turn-on times of any two amplifiers are matched within 10 percent. This feature can be used to advantage in the design of certain systems, as will be shown in the following chapter.

In contrast to turn ON, turn OFF is an essentially instantaneous process. If any of the three amplifier terminals are monitored during the turn-off transient, a low level (≈10 mV) noisy signal lasting for less than 20 ns is observed and the amplifier is OFF immediately after this time. This same type of signal is present on ground because of the application of the rapid pulse to the amplifier. Charge dump at a particular terminal, defined as the integral of the terminal current during the turn-off transient, is the only meaningful parameter in this case. The accurate measurement of this quantity is difficult. The basic technique used involves connecting a capacitor to the terminal of interest and measuring the voltage change at turn OFF. Since the net charge supplied by any terminal during the turn-off transient is small, these capacitors must be small (≈1000 pF) and errors due to leakage paths and dielectric absorption tend to mask any voltages caused by amplifier charge dump. These measurements show that the maximum charge which leaves any terminal at turn OFF must be less than 5×10^{-11} coulomb, and that the values predicted in the last chapter (2.5×10^{-11} coulomb at the negative-gain input, 4×10^{-11} coulomb at the positive-gain input, and 1.6×10^{-11} coulomb at the output) are probably conservative maximum values.

The magnitudes of OFF-state leakage currents present at the various terminals, at least at room temperature, are related to the closeness to which components are matched. The output current is the difference between the leakage current of D_{16} and D_{17} (Fig. 2-18). Both of these diodes are selected for room-temperature leakage current under 10^{-11}A. By matching it should be possible to reduce the difference to less than 10^{-12}A, but matching to this level becomes somewhat academic, since leakage paths present on the circuit board contribute currents of this

magnitude. Accordingly, no particular attention was given to matching leakages for diodes D_{16} and D_{17}. Direct measurements show that the output leakage current of all of the amplifiers is less than 5×10^{-12}A.

In the case of OFF-state input current, matching is important because of the relatively high leakage current (typically 10^{-10}A) of the input transistors. There is also a leakage-current contribution from Q_3 and Q_4, but this is negligible. Diodes D_3 and D_4 are selected to compensate the OFF-state input current, and the resultant value is typically reduced to less than 2×10^{-11}A at either input.

Theory predicts that leakage current of a silicon junction should approximately double every 10°C, and thus OFF-state currents (which are differences between leakage currents) should follow this relationship. The three OFF-state currents were measured for two amplifiers as a function of temperature. The output-current variations were somewhat less than those predicted by the exponential relationship, and this probably reflects the fact some significant fraction of output current is a result of stray leakage paths. Input currents followed the predicted relationship from 10°C to 60°C. Below 10°C input currents became too small to permit accurate measurement, and tended to assume fixed values of less than 10^{-11}A, again probably because of board leakages. Above 60°C the input currents increased more rapidly, averaging a factor of 50 increase from the 25°C value at 75°C.

The shunt resistance to ground at the three amplifier terminals with the amplifier OFF was also measured. This represents the dynamic resistance of the reverse-biased diodes connected to the particular terminal, in parallel with any resistance due to board leakage. These measurements showed resistances greater than $10^{11}\Omega$ from either input to ground, and greater than $5 \times 10^{11}\Omega$ from the output to ground.

I. NONLINEAR PERFORMANCE

The two characteristics discussed in this section are maximum output current and maximum slewing rate.

All amplifiers were tested for maximum output current by measuring step response with large capacitive loads. Maximum (either negative or positive) output current exceeds 200 mA at any output voltage between ±4 volts. Typical maximum positive output current is 450 mA,

while maximum negative output current averages 300 mA. These values are consistent with operating current levels and transistor current gains.

Maximum slewing rate is defined as the maximum time rate of change of output voltage for a large differential input signal. This value determines the limits of linear-region performance under conditions of high-impedance load.

Capacitors in the amplifier limit slewing rate. In many applications the compensating capacitor dominates and the rate limit can be predicted with the aid of Fig. 2-18. Note that the maximum change from the quiescent operating current level that can be caused at base Q_5 as a result of a large differential input signal is ±100 μA. If a compensating capacitor is used, equilibrium is reached when the rate of change of output voltage (which appears across the compensating capacitor) causes a capacitor current equal to the ±100 μA supplied to the base of Q_5. Thus, maximum output slewing rate should be $\frac{10^{-4}}{C_c}$ volts per second where C_c is the value of the compensating capacitor expressed in farads. For example, a 20-pF compensating capacitor (a value typically used in low-gain applications) should limit slewing rate to five volts per microsecond. Measured values average 10 percent to 15 percent lower than predicted values because of current requirements at nodes other than the base of Q_5.

This relationship is valid for negative-going output voltages even for no external compensating capacitor, in which case slewing rates of 50 to 70 volts per microsecond are obtained. These approximate the predicted value for a 1.5-pF compensating capacitor and such a capacitor is always present because of stray capacitance.

Positive-going output slewing rate is limited to approximately 15 volts per microsecond by current limiting at the node including the base of Q_9. The maximum current available at this node for positive-going outputs is 160 μA (the collector current of Q_8), and the total node capacitance is 11 pF.

J. POWER REQUIREMENTS

A primary objective of the amplifier design is minimization of amplifier power requirements. While it is true that the flexibility of the gated amplifier allows significant power economy on a system level

through operation in a mode with amplifiers OFF most of the time, this type of operation at best yields an average power requirement for a particular amplifier which is the amplifier ON-state power multiplied by the amplifier duty factor. The advantages of minimum ON-state power consumption are evident.

Table 3-2 summarizes both ON- and OFF-state measured power requirements of the gated amplifier. A column is included which relates the ON-state currents required from the various power supplies to quiescent currents in different parts of the circuit. The values shown in this table are average values for all six amplifiers, and ON-state currents are all within ±20 percent of the values shown. Total ON-state power is within ±10 percent of 15 mW for all six amplifiers. There is somewhat greater variability of OFF-state currents, but in all cases OFF-state power is less than 60 μW and this value averages less than 50 μW.

OFF-state current from the +9 volt, +7 volt, and -7 volt supplies consists mainly of electrolytic decoupling-capacitor leakage current. This current is larger for the ±7 volt supplies (typically 0.5 μA) than for the +9 volt supply (typically less than 0.1 μA) since two capacitors are used on each 7-volt supply and these capacitors are larger value and are operating closer to rated voltage than other capacitors in the circuit.

The OFF-state current provided by the -12 volt supply, which re-enters the -9 volt supply in such a direction as to deliver power to this supply, is the current flowing through the temperature-compensating network including the two thermistors. Note that the validity of algebraically summing OFF-state power consumption at various voltages is determined by system considerations. This approach is valid only if the average power required from the -9 volt supply is positive. In most systems, amplifier ON-state power consumption or ancillary-circuit requirements insure this situation.

While the OFF-state power consumption is low enough to contribute negligibly to average power consumption in most cases, it is possible to find certain applications where it is objectionable. In these cases the input-current compensating network can be removed if the resulting increase in ON-state input current is tolerable. This results in typical

Table 3-2

Measured Quiescent Power and
Current of the Gated Amplifier

ON-STATE				OFF-STATE	
Supply Voltage	Current (mA)	Power (mW)	Breakdown of Current (mA) (Refer to Fig. 2-18 for a circuit diagram)	Current (μA)	Power (μW)
+9	0.62	5.58	Q_7 emitter current ≈ 0.20 Q_8 emitter current ≈ 0.16 Q_9 collector current ≈ 0.26	< 1	< 9
+7	0.38	2.66	Current through 27-K gating resistor ≈ 0.26 Q_{10}, Q_{11} collector current ≈ 0.12	< 1	< 7
-7	0.12	0.84	Q_{12}, Q_{13} collector current ≈ 0.12	< 1	< 7
-9	0.52	4.68	Q_5 emitter current ≈ 0.42 Q_2 collector current ≈ 0.10	-12*	-108*
-12	0.1	1.20	Q_1 collector current ≈ 0.10	12	144
Total ON-state power ≈ 15 mW				Total OFF-state power < 60 μW	

*Minus sign indicates circuit is supplying power to the -9 volt supply

OFF-state power consumption under 15 μW. Another approach is to increase the resistor and thermistor values used in the temperature-compensating network. This was not done in the amplifier discussed here, primarily because thermistors with appropriate characteristics were not available. However, it should be possible to have special units designed if necessary. Gating the thermistor network is still another possibility.

It is emphasized that the ON-state supply currents listed in Table 3-2 represent quiescent (or no-load) values. If any current is delivered to a load, the current required from either the +7 volt or -7 volt supply increases by an amount equal to the magnitude of the output current and the currents required from other supplies are altered slightly. For this reason the calculation of average power consumption becomes somewhat more involved when gated operation is used, particularly when high peak output currents are required for capacitor charging. Methods for calculating average power under these conditions are developed in Chapter IV.

The gated amplifier ON-state power requirements represent a significant improvement in state-of-the-art in themselves. It is shown in the next section that this represents at least an order of magnitude improvement in power consumption compared with commercially-available operational amplifiers which have performance characteristics similar to those of the gated amplifier in the ON-state. In this sense the compromises made in the gated-amplifier design, particularly those which increased the number of components in order to lower power consumption, are justified for an amplifier intended for use in space.

K. COMPARISON WITH OTHER AMPLIFIERS

The gated amplifier is a highly specialized circuit in the sense that the design procedure was tailored toward minimizing power consumption and toward enhancing the versatility of the circuit when used as a system component. While the basic amplifier structure incorporates several design techniques which are valuable for the design of general-purpose operational amplifiers, certain parts of the circuit would be modified if the design were intended only for use as an operational

amplifier. The design procedure described in Chapter II can be used to effect appropriate modification as required in other applications.

The question can be raised as to whether the design compromises necessary for realization of the gated amplifier being described deteriorate performance to the point where the ON-state characteristics are unacceptable for normally encountered operational-amplifier applications. One way to answer this question is through the comparison of gated-amplifier ON-state performance with that of commercially-available operational amplifiers which are representative of state-of-the-art. There is a large number of such amplifiers available, and certain basic constraints must be applied to determine which among them can logically be compared with the gated amplifier. The following constraints were used. Only those amplifiers are considered which are solid-state amplifiers, can be used differentially at maximum frequency, have low output voltage (±15 volts or less), and have small-signal unity-gain frequencies in excess of 1 Mc.

While these constraints narrow the field somewhat, many amplifiers still remain, and further reduction is somewhat arbitrary. The problem is further complicated by the fact that most manufacturers offer a large number of operational amplifiers which differ from each other in one or more characteristics, and which indicate the design compromises made in the case of the particular amplifier.

With these reservations, the following five amplifiers were selected as representative of high-quality operational amplifiers which adhere to the constraints mentioned above:

1. Analog Devices, Inc., Model 102C
2. Burr-Brown Research Corporation, Model 1506
3. Nexus Research Laboratory, Inc., Model CLA-12
4. Philbrick Researches Inc., Model P35A
5. Zeltex, Inc., Model 115

The specifications supplied by the manufacturers for these five amplifiers are presented in Table 3-3. Corresponding characteristics for the gated amplifier (see Table 3-1) are included. Comparisons between these amplifiers and the ON-state gated amplifier on the basis

Table 3-3

Specifications for Several Amplifiers

Note: All values typical unless specified otherwise

	Analog Devices Model 102/C	Burr-Brown Model 1506	Nexus Model CLA-12	Philbrick Model P35A	Zeltex Model 115	ON-state Gated-Amplifier
D-c open-loop gain (unloaded unless specified)	2×10^6 (rated load)	2×10^5	1.2×10^5 (10-K load)	10^5 (rated load)	5×10^4	8×10^4
Output voltage (volts)	±11	±10	±10	±11	±10	±4
Output current (mA)	±20	±20	±3	±2.2	±4	+450, -300
Common-mode rejection ratio	2×10^4:1	Not specified	Not specified	2×10^4:1	Not specified	10^4:1
Drift referred to input (temp. variation)	5 μV/°C Avg.vs.temp. (-25 to 85°C), max.	5 μV/°C typ. (-25 to+85°C)	3 μV/°C	3 mV max. vs.temp. (-25°C to +85°C)	50 μV/°C	±300 μV (-25°C to +75°C)
Input current (temp. variation)	0.4 nA/°C Avg.vs.temp. (-25 to 85°C), max.	0.2 nA/°C typ. (-25 to + 85°C)	0.2 nA/°C	45 nA max. vs. temp. (-25°C to +85°C)	5 nA/°C	±15 nA (-25°C to +75°C)
Input resistance (differential)	6 M	500 K	200 K	1.5 M, min.	100 K	400 K
Input resistance (common-mode)	500 M	25 M	20 M	100 M, min.	10 M	200 M
Small-signal unity-gain frequency (Mc)	10	1.5	1.5	4	2	30
Slewing rate (volts per microsecond)	30	2	Not specified (10 Kc typ. freq. for full output)	0.5 (worst case)	10	+15, -60 (no external compensation)
Power consumption (unloaded unless specified)	1.05 watt (rated load)	150 mW	300 mW	180 mW	120 mW	15 mW

of specifications are somewhat questionable because the basic question of interest to a systems designer, namely, "What amplifier will yield the best performance in my system?" is certainly left unanswered. It is felt, however, that the specifications show a continuously ON gated amplifier could be used interchangeably with the other amplifiers in many applications where the lower output voltage of the gated amplifier is tolerable. The power consumption advantage ranging from a factor of 8 to 70 of the gated amplifier is evident.

Two possible disadvantages of the gated-amplifier circuit are not apparent from the table. One is that the gated amplifier requires five separate supply voltages for operation, while all of the other amplifiers listed in Table 3-3 require only two voltages. This complicates the design of a power supply intended for use with gated amplifiers. On the other hand, the lower power requirements of the gated amplifier might simplify the supply somewhat in special applications.

A second possible disadvantage is the relatively large number of components used in the gated-amplifier circuit. Since manufacturers are understandably reluctant to disclose amplifier schematics, no method (other than possibly x-raying an encapsulated unit which was not done) is available to determine accurately the number of components used in the amplifiers listed in Table 3-3. However, a reasonable estimate is between 25 and 75 components for most of the amplifiers, leading to the conclusion that the gated amplifier contains approximately twice as many components as an operational amplifier with comparable characteristics. The gated-amplifier circuit may cost more to build than other operational amplifiers because of this increased component count.

L. RELIABILITY CONSIDERATIONS

Insuring reliability for any circuit intended for use in space is normally given almost overriding consideration. Since the gated amplifier uses approximately twice as many components as an operational amplifier with performance characteristics comparable to those of the gated amplifier in the ON-state, the reliability of gated-amplifier data-processing systems compared with other types of systems which perform similar functions merits discussion.

A complete reliability analysis for the gated-amplifier circuit is beyond the scope of this research, and would constitute a separate research project in itself. The purpose here is only to show that some features of the gated amplifier may compensate, at least in part, for the decrease in reliability which may accompany increases in the total number of components used in the circuit.

The amplifier alone is considered first. For the purpose of reliability estimates, it is convenient to divide components into two broad categories:

1. Passive components, exclusive of diodes, including interconnections between all components.
2. Transistors and diodes.

Reliability investigations to date indicate that the reliability of components in the first category exceeds that of components in the second category. This situation may not be true, however, in the future. For example, high-quality transistors, particularly planar devices, have not been in existence long enough for tests with anywhere near the confidence level of experience gained with carbon resistors. If current estimates of the relative reliability of components in the two categories are accepted, however, the conclusion that circuit failure rates must be almost entirely related to diode and transistor failure is inevitable for the following reasons:

1. Failure rates for resistors are vanishingly small. For example, a resistor manufacturer states that none of their composition resistors have ever failed in applications where specified operating limits were observed.
2. Failure rates of 0.001 percent per 1000 hours have been demonstrated for ceramic capacitors of the type used in the gated-amplifier circuit, and these rates were measured under conditions of 100 volts applied to the capacitor and at 125°C ambient temperature, values which are far in excess of those anticipated in even the most demanding space applications.

3. Sprague Electric Company[8] has demonstrated failure rates of 0.0004 percent per 1000 hours on solid electrolytic tantalum capacitors of the type which could be used in the construction of final circuits (type 350D). These tests were conducted under conditions approximating those which are present with the gated-amplifier circuit.

4. The reliability of interconnections depends on the packaging technique used. Printed-circuit cordwood construction is mentioned in Appendix I as a possible method for the construction of final circuits. Failure rates of less than 0.00003 percent per 1000 hours[9] have been demonstrated with this technique.

5. In contrast to the failure rates for components in the above categories, diodes and transistors exhibit typical failure rates on the order of 0.005 percent per 1000 hours at rated operating conditions.

There are several factors which influence semiconductor failure rates in space. One often-publicized cause is radiation damage. However, all tests indicate that radiation damage is a "go-no go" type phenomenon. Essentially all transistors of a given type will fail after a certain exposure level, while none fail for a certain lower level. This indicates a reliability penalty from this cause is not attributable to increased numbers of semiconductor devices. Radiation susceptibility as a function of the type of device used, and tests to date indicate that high-frequency silicon planar devices (which are used exclusively in the gated-amplifier design) are the most resistant types.

A major consideration is how power dissipation affects the reliability of semiconductor devices. The operating power levels used in the gated-amplifier circuit are significantly lower than those of conventional analog circuits. The highest ON-state unloaded power dissipation in any device occurs in Q_6 (Fig. 2-18) for maximum positive output voltage. Under this condition 4.5 mW, or approximately 2 percent of rated power, is dissipated in the device. Gating further reduces average power dissipation to a small fraction of the ON-state value in most applications. Peak power in the output transistors, of course,

exceeds this figure during a charging transient. In this case, however, the maximum energy which contributes to junction heating is the only significant factor, since the high-power state lasts for only a short period of time. Calculations involving the junction thermal capacity and the charging waveform show that charging a 1-μF capacitor the maximum value of 8 volts raises the junction temperature of an output transistor by less than 0.05°C, and this temperature increase is negligible.

While all sources seem to agree that operation at reduced power level leads to reduced semiconductor failure rates, none are specific about the relationship, particularly at power levels which are a small fraction of rated power. Gordy[10] does present generalized curves for diodes and transistors which relate failure rates to ambient temperature with fraction of rated power as a parameter. These curves cover the range from 0.1 to 1.0 times rated power, and the curves for both classes of devices are similar. At low temperatures (probably near room temperature) failure rates for either transistors or diodes increase by a factor of approximately 1.3 as power level is increased from 0.1 to 0.2 times rated power. Failure rates increase by a factor of 3 if relative operating power is increased from 0.1 to 0.5. The dependence on operating power level is more severe at higher temperatures. At these temperatures (which might be approximately 75°C for the types of devices used in the gated amplifier) failure rates increase by a factor of 7 for a change in operating power level from 0.1 to 0.2 times rated power.

While no information is given as to how the curves could be extrapolated to lower power levels, it seems reasonable to expect a further failure-rate decrease by a factor of from 1.3 at low temperature to 7 at high temperature if relative power is decreased one or two orders of magnitude from 0.1 times rated power.

If it is assumed that semiconductors in commercially-available operational amplifiers are operating at 0.2 times rated power (which is reasonable in view of circuit power consumption), the individual semiconductors used in the gated amplifier should display failure rates which vary from 0.6 to 0.02 times those of the semiconductors in other operational amplifiers. Since the number of semiconductors

used in the gated amplifier is probably twice that of typical operational-amplifier circuits, gated-amplifier failure rates should vary from 1.2 to 0.04 times those of other operational-amplifier designs depending on ambient temperature. While it is realized that these predictions and the semiconductor failure curves on which they are based are general, the indication is that at least a large part of the possible reliability disadvantage of the gated-amplifier circuit which arises from increased component count is recovered because of operation at lower power levels.

In addition to the reliability advantages of low-power operation at the circuit level, several possible reliability advantages exist on a system level. It is shown in Chapter IV that, at least in some typical applications, a gated-amplifier data-processing system is less complex in terms of total component count than systems which do not use gated amplifiers. This complexity reduction is possible in some cases because fewer gated amplifiers are required and/or because a smaller number of ancillary circuits are required.

A further reliability advantage should be attributable to gated-amplifier data processors when the entire spacecraft system is considered. The number of components such as solar cells and storage-battery cells used in the power system can be reduced because of the lower power requirements of the gated amplifier. This becomes particularly significant in view of the fact that power reductions of two to three orders of magnitude are often possible when gated amplifiers are used.

Other considerations also enter the picture. For example, attitude-control systems are at times included in a spacecraft only to permit orientation of solar cells, in order to reduce the required solar-cell area. The elimination of need for an active attitude-control system because of more efficient use of solar cells would certainly increase overall system reliability. Similarly, temperature-control systems are at times included only to handle the heat generated by spacecraft electronics and elimination of the need for such a system would aid overall reliability.

Another possible reliability benefit stems indirectly from the versatility of the gated amplifier. It is shown in Chapter IV that many

typical data-processing operations can be accomplished using only gated amplifiers and a small number of auxiliary circuits, primarily logic circuits. This general-purpose applicability is a feature unmatched by other analog circuits, which often have to be modified through use of extensive auxiliary circuitry. Reliability advantages arise from the fact that the smaller number of circuit types required for gated-amplifier systems can be more thoroughly tested, and this provides a means for eliminating potentially unreliable features of the designs.

While the factors discussed above undoubtedly influence the reliability of gated-amplifier systems favorably, the extent of the reliability improvement expected in a specific application can be determined only in the context of a particular experimental program.

Two examples from personal experience are also relevant to this reliability discussion. The M.I.T. Gamma-Ray Telescope[11] experiment was designed and built at Lincoln Laboratory in 1963-64. This experiment required approximately 8000 components including 1300 transistors. Low-power design techniques were used exclusively, with the result that the total power consumption was 500 mW. (This represents an average power of 0.4 mW per transistor, approximately equivalent to a gated-amplifier system operating at the extremely high average duty factor of 40 percent).

Two flight systems were constructed, and a total test time of more than one system year has been completed, with much of this time under simulated stress conditions such as thermal vacuum. No failures have been experienced during testing. Unfortunately, the first launch vehicle failed so that no reliability data under actual space conditions is available.

The second example is with the gated amplifier itself. I estimate that over 5000 amplifier-hours of operation have been accumulated to date with this circuit. A small percentage of this time has been at temperatures other than room temperature. One unusual stress mechanism has been applied in that probably every node in every amplifier has been shorted to ground at one time or another during testing. (A power supply which is current limited at 10 mA has been used for all tests). No failures have been experienced. Also, a board containing a power supply of the type which would probably be used for gated-amplifier

systems and five logic circuits similar to those which are used with gated amplifiers has been operated continuously for more than one and one-half years. The single circuit failure experienced during this time was caused by an error in test procedure.

CHAPTER IV

APPLICATIONS

The purpose of this chapter is to show how gated amplifiers are used to perform typical data-processing operations. The circuits which are developed to perform linear operations such as integration, and nonlinear operations including multiplication, division, and analog-to-digital conversion require only gated amplifiers, passive elements, timing or logic circuits, and a simple shunt switch for realization.

A major advantage of gated-amplifier data-processing systems compared with conventional analog systems is greatly reduced average power consumption. Hence, they are particularly attractive for space applications. The approach used for power minimization with gated amplifiers is threefold:

1. Use the versatility of the gated amplifier to full advantage in order to minimize the number of amplifiers required to perform a given operation. This approach generally minimizes the number of ancillary circuits required also.

2. Use gating so that all amplifiers are ON a minimum fraction of the time.

3. Use a gated-amplifier circuit which requires minimum power when ON.

The third item has been described in Chapters II and III; this chapter illustrates the implementation of the first two.

Applications are presented in the form of a series of systems which use gated amplifiers as the active devices and which are capable of performing both linear and nonlinear operations. While the list of applications developed in this chapter is far from complete, it does serve to illustrate the approach to system design which is used with gated amplifiers, and how this approach differs from that used with conventional operational amplifiers.

Several basic operations, including sampling, a passive voltage transfer between capacitors that I call leak back, and gated integration, are described in the initial sections of the chapter. Some deviations from ideal performance caused by nonideal amplifier characteristics are calculated.

More complex operations are developed as combinations of the basic operations. The error predictions for the basic operations are used to calculate expected errors for the more complex systems.

Two systems, a multiplier-divider and an 8-bit digital-to-analog converter, have been built and test results are presented for these systems.

A. DEFINITION OF SYMBOLS

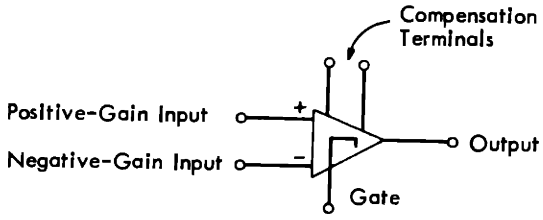
The symbols which are used for the representation of gated-amplifier systems are shown in Fig. 4-1.

The symbol used for the gated amplifier (4-1a) was introduced in the previous chapter. The gate lead is grounded to turn the amplifier ON and is switched to +9 volts to turn the amplifier OFF. The compensation terminals are always shown, even in cases where no compensating capacitor is used.

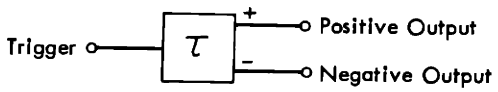
The designs used for the ancillary circuits (Figs. 4-1b through 4-1f) are presented in Chapter V. The following introduction of these circuits lists only those characteristics required to illustrate their functions in systems. In order to predict system performance, certain ancillary circuit specifications such as power consumption are necessary, and these parameters are included in the discussion of systems as required. The verification of these specifications is reserved for Chapter V.

One-shot multivibrators (Fig. 4-1b) are used with gated amplifiers to generate gating signals or to provide time delays. The one-shot multivibrator provides a +7 volt pulse of duration τ at the terminal marked by a plus sign following application of a positive-going (0 to +7 volt) trigger signal. The value of τ can be adjusted to any duration normally required in gated-amplifier systems. A simultaneous 0 volt signal is available at the terminal marked by a minus sign. Following the time interval τ, the circuit returns to its quiescent state, with the + terminal at ground and the - terminal at +7 volts. The trigger circuitry of the one-shot multivibrator is transition sensitive but not level sensitive; that is it is a-c coupled.

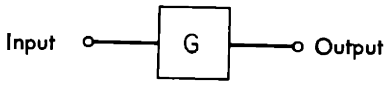
The gate-driver circuit (Fig. 4-1c) is used to provide amplifier gating signals. This circuit inverts the input so that a logical 1 (+7 volts) turns ON a gated amplifier connected to it. The gate driver



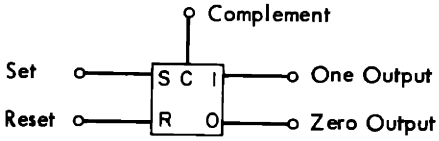
a) Gated Amplifier



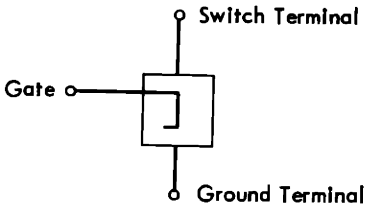
b) One-Shot Multivabrator



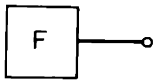
c) Gate Driver



d) Flip-Flop



e) Shunt Switch



f) Clock

Fig. 4-1 Definition of Symbols

also performs the required level shifting between logic levels and gate-drive levels.

The flip-flop (Fig. 4-1d) is used to generate gating-interval pulses in certain applications such as analog-to-digital conversion. The set and reset terminals may be either a-c or d-c coupled, and no symbolic distinction is made between these two cases. The logic is such that either a positive transition or a +7 volt level (depending on whether the terminal is a-c or d-c coupled) applied to the set terminal forces the output terminal marked 1 to +7 volts, and simultaneously forces the terminal marked 0 to ground. A positive transition applied to the complementing input causes the flip-flop to change state.

The shunt switch (Fig. 4-1e) differs from a floating switch (as typified by a relay) in one important way. A logical 1 applied to the switch gate lead short circuits the switch terminal to the ground terminal. However, the current leaving the ground terminal is the sum of the currents entering the gate lead and the switch terminal. The switch terminal is effectively isolated from the gate terminal but the ground terminal is not, and therefore the ground terminal may only be connected to low-impedance points. Switches used in gated-amplifier systems are restricted to this type, since they are very simple to realize compared with a floating switch.

The clock (Fig. 4-1f) supplies pulses which may be used to trigger either one-shot multivibrators or flip-flops at a frequency F. The trigger frequency is adjustable over the range normally required in gated-amplifier systems.

The circuits shown in Fig. 4-1 are essentially the only circuits (aside from passive feedback networks) required for the realization of a large class of functions by means of gated amplifiers. This reduction of the large number of ancillary circuits typically required to adapt conventional operational amplifiers to specific applications is a consequence of the inherent versatility of the gated-amplifier circuit.

B. SAMPLING WITH THE GATED AMPLIFIER

Sampling is of fundamental importance in many data-processing systems using gated amplifiers, and in these systems gating is directly responsible for the expected power economy.

A sample-and-hold circuit is a circuit which exhibits the following property. An input signal, $E_{in}(t)$, is sampled for a short time interval, during which time the signal does not change value by a significant amount. The value of $E_{in}(t)$ during the sample interval is then maintained for some time period (usually much longer than the sample period) following the sampling operation.

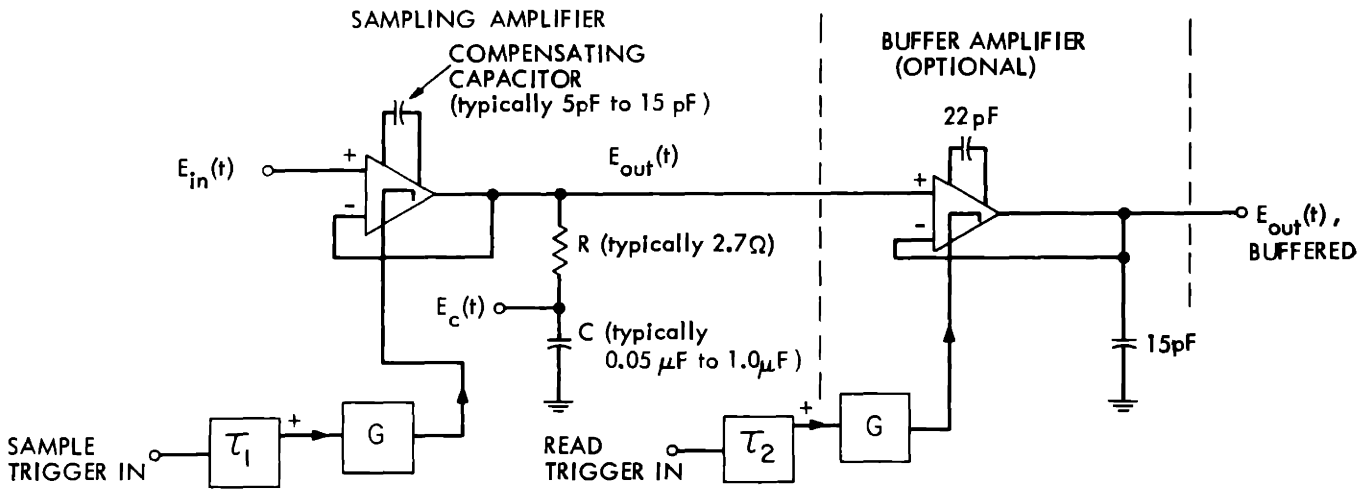
By its very nature, sampling implies some type of configuration switching to convert from the sample mode to the hold mode, and high-quality sample-and-hold circuits usually are quite complex. The required circuitry is greatly simplified by the inherent switching capability of the gated-amplifier circuit.

The gated-amplifier sampler offers a combination of characteristics unmatched by other sampling circuits. Samples can be acquired in less than 5 μs, and the accuracy of a gated-amplifier sampler is limited by dielectric absorption in the hold capacitor rather than by amplifier errors. The ratio of hold time to sample time for a one percent of maximum output error is typically 4×10^7.

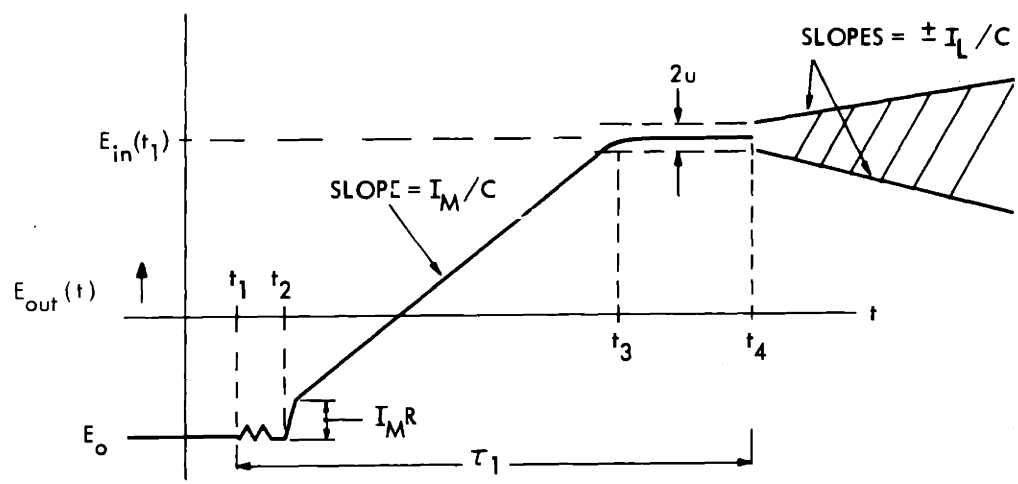
One possible sample-and-hold circuit is shown in Fig. 4-2. The purpose of the optional buffer amplifier is explained later in the development. The sampling capacitor C is connected to the output of a gated amplifier and unity feedback is applied around the amplifier. With the amplifier ON, its output voltage, and therefore the voltage on the capacitor, is forced to be equal to the input voltage. The capacitor is isolated when the amplifier is OFF, and this is the hold mode.

Details of the process are illustrated with reference to Fig. 4-2b. At time t_1 a trigger pulse is applied to the one-shot multivibrator, initiating the sampling operation. At this time the value of the input voltage is $E_{in}(t_1)$, and it is assumed that this value remains constant during the sampling interval. The initial voltage stored on the capacitor is E_o.

The time interval t_1 to t_2 represents amplifier turn-on time. Following this time interval, the amplifier will generally supply maximum output current (it is assumed that there is a large difference between E_o and $E_{in}(t_1)$ so that the amplifier saturates). This forces a rapid change in output voltage equal to $I_M R$, where I_M is the maximum amplifier output current. The output voltage then becomes a linear



a) Sample-and-Hold Circuit with Buffer



b) $E_{out}(t)$

Fig. 4-2 Sampling with the Gated Amplifier

ramp with a slope equal to I_M/C because of capacitor charging. At time t_3 the amplifier enters its linear operating region with a small error existing between input and output voltages. It is not sufficient that only the output voltage reach final value, since the voltage stored during the hold interval is that on the capacitor, and the capacitor voltage lags the amplifier output voltage because of the resistor R. The time interval t_3 and t_4 is required for capacitor voltage E_c to reach final value. At time t_4 the amplifier is gated OFF and the circuit enters the hold mode.

The maximum sampling time determines the minimum value of τ_1, and the required time can be calculated from amplifier characteristics. The turn-on time of the amplifier is normally less than 1 μs. The time interval t_2 to t_3 has a maximum value $\frac{E_M C}{I_M}$, where E_M is the maximum change in capacitor voltage. Since E_M must be less than or equal to 8 volts and since I_M is greater than 200 mA, the time interval t_2 and t_3 has a maximum value equal to 40C seconds when C is expressed in farads.

The total time for the capacitor voltage to settle to final value, t_3 to t_4, is related to the amplifier transfer function and the R-C time constant. The stabilization used with the amplifier is important since this affects the transfer function. An extension of the analysis of Chapter II, Section O, indicates that the amplifier can always be stabilized with typical load capacitor values (0.05 μF to 1 μF) if a 2.7-Ω resistor is used for R, and if the load capacitor and compensating capacitor are related as shown below.

Load Capacitor	Compensating Capacitor
0.05 μF	3 pF
0.1 μF	5 pF
0.3 μF	10 pF
1.0 μF	15 pF

With this type of compensation, the time required for settling is determined primarily by the R-C time constant, and it can be shown that 7 R-C time constants are sufficient to permit settling to within 1 mV under all conditions. Therefore, the time interval t_3 to t_4 has a maximum value of 20C seconds.

The maximum required sampling time τ_1 is 1 μs + 60C seconds, the sum of the terms listed above. This relationship predicts typical sampling times ranging from 4 μs with a 0.05-μF load capacitor to 60 μs with a 1-μF capacitor.

The actual output voltage at any time following t_4 lies within the shaded region indicated in Fig. 4-2b. The initial uncertainty is represented as a region of width 2 u, and several factors contribute to this incertainty. Those related to the amplifier are:

1. Errors from insufficient settling time should be less than 1 mV if the expression developed above is used to determine sampling time.

2. Amplifier voltage drift introduces an error equal to the drift. This error is less than 750 μV at any temperature from -25°C to +75°C.

3. The error from finite common-mode rejection ratio equals the maximum voltage (4 volts) divided by the rejection ratio (typically 10^4) and is typically less than 500 μV.

4. Charge dump from the output and negative-gain input terminals at turn OFF contributes a maximum error of less than 1 mV if a hold capacitor larger than 0.05 μF is used.

These relations lead to the conclusion that the maximum initial sampling error attributable to the amplifier is limited to approximately 3 mV.

A further initial error is introduced by dielectric absorption in the hold capacitor. This effect results in an error equal to the magnitude of the change in capacitor voltage during the sampling interval multiplied by the dielectric absorption coefficient.

The dielectric absorption coefficient is dependent primarily on the dielectric material used in a particular capacitor. Ceramic capacitors, particularly those which use ceramics with high dielectric constants, are notoriously poor from an absorption point of view. Absorption coefficients in excess of 10 percent are typical for some types, and this feature generally precludes the use of ceramic capacitors as storage capacitors. Mylar is somewhat better with a typical absorption

coefficient of 0.5 percent. Polystyrene is a material which is often used because of its low absorption coefficient (typical values are 0.05 percent to 0.1 percent). Teflon, although inefficient in the sense that teflon capacitors are generally much larger than equivalent-value capacitors constructed with other dielectric materials, exhibits the lowest value of dielectric absorption coefficient known, typically 0.03 percent.

It is interesting to note that teflon would contribute a 2.4-mV sampling error for an 8-volt change in voltage. This error is nearly as large as the maximum sampling error expected from all other causes, and it exceeds typical errors. Thus, the basic limitation to sampling accuracy is imposed by the storage capacitor rather than the gated-amplifier circuit, even in the case where teflon is used as the dielectric material.

Mylar capacitors are generally used for storage in the experimental systems described later in the chapter. The errors from dielectric absorption can often be compensated for since they are repeatable, and the methods used for this compensation are explained later. No such possiblity exists, however, in sampling applications where an arbitrary sequence of input voltages is assumed.

The error increases with time from its initial value because of leakage current into the hold capacitor. This effect is illustrated by the bounding lines on the region of uncertainty shown in Fig. 4-1b. The slope of these lines is $\pm\frac{I_L}{C}$, where I_L is the leakage current into the capacitor. If no load is connected to the capacitor and if its insulation resistance is sufficiently high, I_L is equal to the sum of the OFF-state currents at the output and negative-gain input terminals of the amplifier. The magnitude of this current is typically 1.5×10^{-11} A.

One figure of merit for the gated-amplifier sample-and-hold circuit without load is the ratio of sample time to hold time for a given error, and this ratio can be predicted from amplifier parameters. The equation developed earlier shows that the required sampling time is approximately 60C seconds for any expected capacitor size. The leakage rate is $\frac{I_L}{C}$, and errors from this term predominate in any applications which require long hold times. The time for a given error is then $\frac{\Delta EC}{I_L}$, where ΔE is the maximum permissible error

voltage. With the aid of these two relationships, the ratio of hold time to sample time can be expressed as $\frac{\Delta E}{60I_L}$. If a ΔE of 40 mV (1 percent of maximum output) is assumed, the typical sample time to hold time ratio is 4×10^7. This compares with values of 10^4 to 10^6 for commercially-available sample-and-hold circuits.

Larger ratios of sample time to hold time can be obtained by cascading two sampling circuits. The first sampler uses a small capacitor to permit rapid acquisition. The output of this first sampler is sampled with a second circuit that uses a large capacitor to permit long hold time. Hold time to sample time ratios in excess of 10^{10} should be possible with realistic component values if this approach is used.

Until this point the problem of loading has been ignored. It is evident that loading must be considered, since the stored voltage is of little value unless it can be observed. Several methods are available to provide buffering, and these methods permit readout with a low-impedance circuit. A very simple method is to use a continuously ON gated amplifier connected as a unity-gain, non-inverting amplifier (Fig. 3-6) as a buffer. Two problems are inherent to this approach. The sampling-system power consumption is increased by 15 mW because of the continuously ON amplifier. Furthermore, the ratio of hold time to sample time is decreased by a factor of 300 because of ON-state input current to the buffer.

A more attractive option is the use of a gated buffer amplifier shown as the optional buffer amplifier in Fig. 4-2a. In many long-hold applications it is not necessary to monitor data continuously, and in such cases a gated buffer amplifier can be used. For example, a voltage representing some experimental variable is sampled and then held for some long time period until it can be accepted by telemetry. Observation of the variable is necessary only at the end of the hold-time interval.

The need for a separate buffer amplifier is normally not present in more complex systems which incorporate sampling because loads applied to the sampler usually consist of other gated amplifiers. Typical examples are included in following sections.

The method used to compute average power for the gated-amplifier sampler illustrates a method used for more complex systems. Only the

sampling amplifier is considered. Assume that the amplifier operates with a 1-μF load capacitor (60 μs sampling interval) at a 100 c/s trigger rate. Further assume that the average voltage change required at each sampling interval is 1 volt. The average amplifier power is then computed as follows. The amplifier circuit, exclusive of load, requires 150 μW (50 μW from OFF-state power consumption plus 100 μW from the duty factor, 0.006, multiplied by ON-state power). Charging the capacitor 1 volt requires 1 microcoulomb, and this charge is supplied from 7 volts, so that a net average energy of 7 microjoules is required per cycle for capacitor charging. This adds an average power of 700 μW at the operating frequency for a total of 850 μW.

C. EXPERIMENTAL SAMPLE-AND-HOLD CIRCUIT

The sampling circuit shown in Fig. 4-2b (exclusive of buffer amplifier) was constructed with a 15-pF compensating capacitor and an output network that consisted of a 2.7-Ω resistor in series with a 1.0-μF polystyrene capacitor. The nominal sampling time used was 60 μs.

Input and output voltages to the sampling circuit were compared using a Keithley model 610B Electrometer as a preamplifier to prevent storage capacitor loading in the hold mode, and the Keithley output was read with a digital voltmeter. The resolution of this system (though not absolute accuracy) is sufficient to determine sampling errors of approximately 1 mV at any voltage level between ±4 volts.

Errors from amplifier drift, common-mode rejection, and charge dump were isolated by applying a constant input voltage and sampling this voltage several times. This procedure eliminates errors from insufficient settling time and dielectric absorption. A number of input voltages from -4 volts to +4 volts were used. No errors larger than 2 mV were ever observed, with a typical error figure of 1 mV.

The circuit was next tested by sampling a voltage at one level, and then changing the input voltage and applying one sampling pulse. Errors of approximately 0.12 percent of the voltage change were measured consistently. It seems unlikely that if this error were related to amplifier settling time it would be consistent for both positive and negative changes, since the output waveform differs in the two directions. However, since 0.12 percent is somewhat higher

than the typical specified dielectric absorption coefficient of polystyrene, one further test was conducted. The sampling time was increased to 200 μs. If the error resulted from insufficient settling time it should be reduced by increasing sampling time. The same 0.12 percent error was again measured and it is concluded that this must be a consequence of dielectric absorption. Detailed tests were not conducted with smaller hold capacitors, but lower values are used in the larger system described later in this chapter and every indication is that the results are equally good.

The predicted typical ratio of hold time to sample time of 4×10^7 was verified.

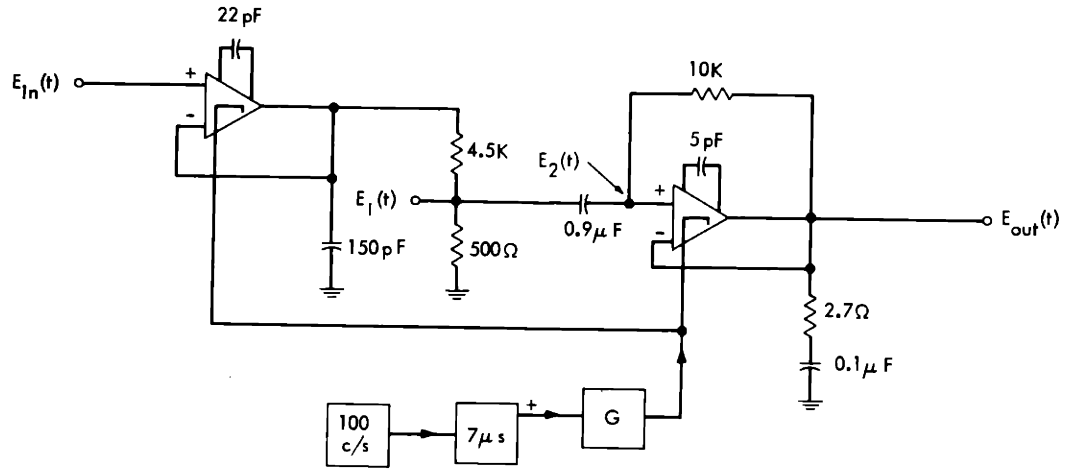
The power consumption of the sampling circuit was tested for conditions approximating those used for the calculation made in the preceding section. The input supplied to the sampler was one volt. The circuit was triggered at a 100 c/s rate, and the hold capacitor was loaded with a 2.2-K resistor. This resistor discharged the capacitor between samples so the voltage change was one volt during each sampling interval. The measured power consumption agreed with the predicted value (850 μW) within experimental errors.

D. LEAK BACK

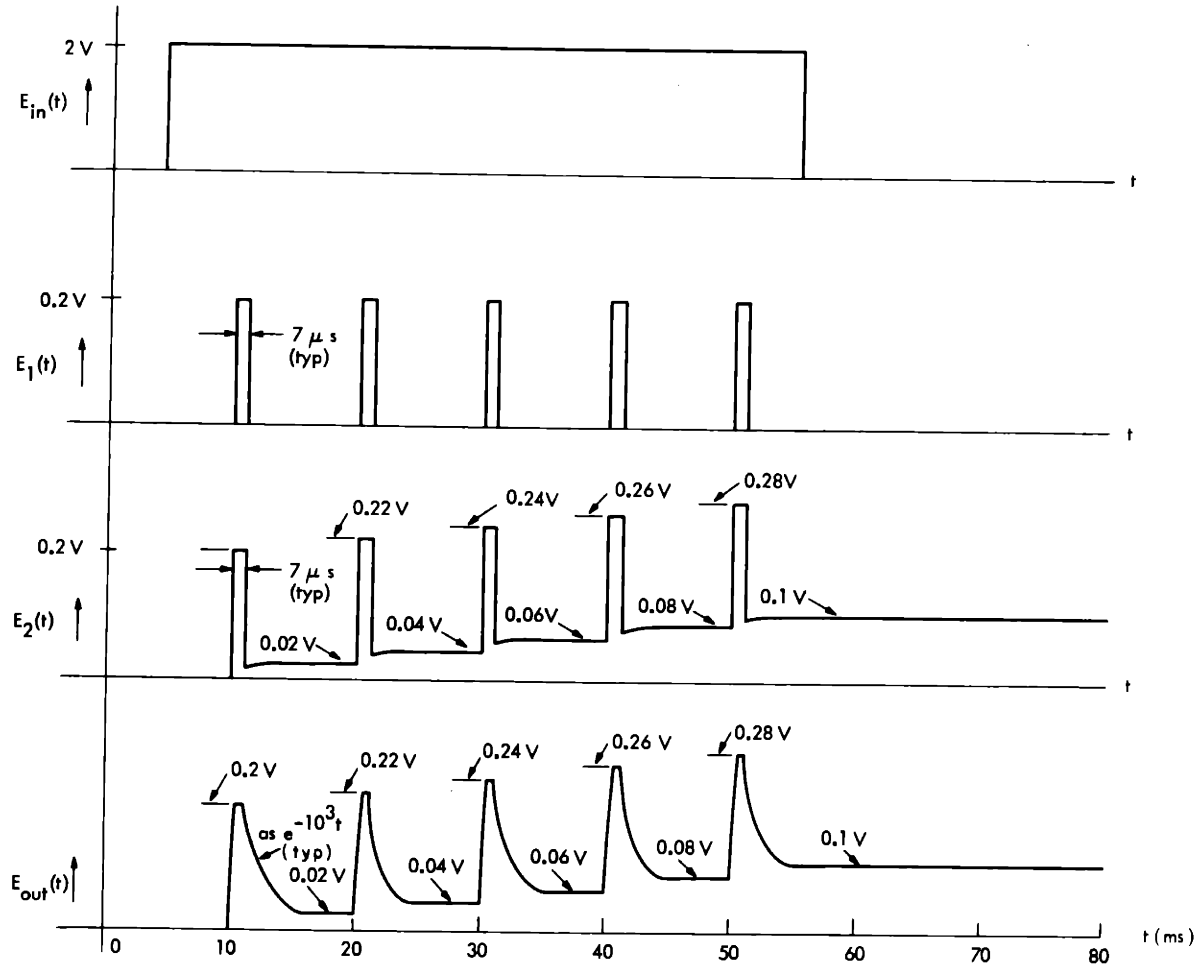
A second fundamental technique used in gated-amplifier systems is leak back. Leak back consists of a passive charge transfer from one capacitor to another during the time when a gated amplifier is OFF, and it provides a very simple form of data modification as well as storage during the OFF interval.

One simple system which uses leak back and which serves to illustrate the concept is shown in Fig. 4-3. This system is postulated for the following application. Assume that a low-frequency signal (all frequency components under 10 c/s) is to be integrated with unity gain (the desired transfer function is 1/s). One method would be to use the gated amplifier as an analog integrator. This would provide the required transfer function, but since the amplifier would be ON continuously, operating power would be at least 15 mW.

Note that an integrator constructed in this way would be useful to frequencies above one megacycle per second, but this type of performance



a) Sampling-Mode Integrator



b) Waveforms

Fig. 4-3 Sampling-Mode Integration Using Leak Back

is wasted on the postulated input. The question is raised as to whether it is possible to use gating in some form to trade bandwidth for power.

It will be seen that this is a commonly recurring tradeoff with gated-amplifier systems. Gating does not offer a method to get something for nothing. If high-frequency processing is required, full operating power must be supplied since in any high-bandwidth application information is lost when an amplifier is OFF. However, when only low-bandwidth information is to be processed (and this is a very common situation in space applications), gating offers a method for dramatic power-consumption reduction.

The system shown in Fig. 4-3 is one method for effecting a bandwidth-power tradeoff, and the operation of this circuit is explained with the aid of the waveforms shown in Fig. 4-3b. The time axis is distorted in these waveforms; the intervals between sampling instants would be much longer if the figure were drawn to scale. Also, the input waveform, a 50-ms, 2-volt pulse, obviously violates the postulated bandwidth condition, but this input is shown only for purposes of illustration.

All capacitors in the circuit are assumed initially discharged, and the input is zero until some time after $t = 0$. The clock supplies pulses every 10 ms, and these pulses are used to gate ON both amplifiers for a period of 7 μs. The gating interval is selected to insure completion of various charging transients.

The first gated amplifier is used only as a switch and in certain more complex applications its function can be combined with that of a preceding amplifier. This amplifier is connected to provide non-inverting unity gain and its output is attenuated by a factor of 10:1 with a resistive divider network. At all sampling intervals prior to $t = 10$ ms the input to this amplifier is zero, and therefore the voltage out of the attenuator $E_1(t)$ is zero whether the first amplifier is ON or OFF. At some time between $t = 0$ and $t = 10$ ms, the input $E_{in}(t)$ changes to +2 volts. Thus, at $t = 10$ ms, $E_1(t)$ assumes a value of +0.2 volt. The loading of the 0.9-μF capacitor can be neglected, since it will be shown that at equilibrium there is no current flow through this capacitor. The voltage across the 0.9-μF capacitor is initially zero, so that +0.2 volt must appear at the positive-gain input terminal of the second gated amplifier. This second amplifier is connected as

a sampler with leak back. The output of the second amplifier $E_{out}(t)$ is driven to within several millivolts of 0.2 volt within 2 μs. The capacitor voltage reaches 0.2 volt during the remaining ON time. Since equilibrium is reached within 2 μs, the change in voltage across the 0.9-μF capacitor during the sampling interval is negligible. At equilibrium, the current through the 0.9-μF capacitor must be zero (since there is no voltage across the 10-K resistor) and therefore $E_1(t)$ must be equal to $\frac{E_{in}(t)}{10}$ when equilibrium is reached.

The amplifiers gate OFF at t = 10.007 ms, and at this time 0.2 volt is stored on the 0.1-μF capacitor and zero volt is stored on the 0.9-μF capacitor. With the amplifiers OFF, the charge stored on the 0.1-μF capacitor starts to leak back to the 0.9-μF capacitor and, aside from gated-amplifier OFF-state currents, total capacitor charge must be conserved during this operation. The time constant associated with this transient is approximately 1 ms, and at its completion a voltage of 0.02 volt equal to 0.01 E_{in}(10ms) is stored on both capacitors.

The cycle repeats in identical fashion at t = 20 ms, with the single exception that the new initial conditions are 20 mV on both capacitors. This results in a final value after completion of the second sampling and leak-back cycle of 40 mV on both capacitors. This process repeats for three more cycles, after which the input returns to zero. No further changes in stored voltage occur for t > 50 ms and the final voltage stored on both capacitors is 100 mV.

In general, the voltage stored on both capacitors, at least during time intervals when the leak-back transient is not in progress, is

$$E_{out}(t) = 0.01 \sum_{k=0}^{n} E_{in}(k\ 10\ ms)$$

This expressions is an approximating sum to $\int_0^{n(10\ ms)} E_{in}(t)dt$. The approximation is valid for sufficiently slow variations of $E_{in}(t)$. Low-pass filtering can be used to remove the exponential spikes from $E_{out}(t)$ so that it more closely approximates the true integral. Details of this

type of filtering are described later in connection with the multiplier-divider system. It is shown that filtering can be incorporated into the leak-back network without additional amplifiers.

Many variations which yield essentially the same results are possible. For example, the capacitor at the output of the second amplifier could be made equal in size to the capacitor at its input. This would result in an attenuation by a factor of 2 rather than 10 during the leak-back interval. However, this approach would result in higher integrator drift rates, as indicated by the following analysis.

Integrator drift is defined as the average rate of change of $E_{out}(t)$ for zero $E_{in}(t)$. With $E_{in}(t)$ equal to zero, $E_1(t)$ will be non-zero at sample intervals because of drift referred to the input of the first amplifier. The voltage $E_1(t)$ will be the drift of the first amplifier divided by 10 when the first amplifier is ON. This error is negligible compared to errors from drift of the second amplifier.

The errors due to drift of the second amplifier are reduced to 10 percent of initial value because of the 10:1 attenuation of the leak-back circuit. In general, all sampling errors will be attenuated by the same amount, and such sampling errors were shown to be typically 1 mV in the last section. (Errors from dielectric absorption are ignored, since they enter only as scale-factor change and therefore can be eliminated by slight modification of the ratio of the two capacitors.) Since the sampling errors are reduced by a factor of 10 as a consequence of leak back, typical errors are less than 100 μV per cycle resulting in an expected 10 mV per second drift rate from this cause.

Drift rate also results from any average current flowing into the total 1-μF (0.1 μF + 0.9 μF) storage capacitor. One current component is OFF-state current from the output and negative-gain input terminals of the second amplifier. This contributes an average drift rate of less than 50 μV per second, which is negligible. Another average current is a result of charge dump from the second amplifier and this should result in typical drift rates of less than 5 mV per second. Another source of average current is the ON-state input current of the second amplifier, but because of low duty factor this contributes negligibly to drift rate.

Even with no input signal, charge is supplied to the 0.9-μF capacitor through the 10-K resistor during the turn-on transient of the second amplifier. This transient should typically supply a charge of less than 5×10^{-11} coulombs per cycle of operation, leading to an expected drift rate of less than 5 mV per second from this cause. Thus overall drift rates of less than 20 mV per second are expected. Most of the drift is relatively fixed, and it should be possible to compensate drift rate (for example, by supplying bias current to the 500-Ω resistor in Fig. 4-3) to less than 2 mV per second over the $0^{\circ}C$ to $+50^{\circ}C$ temperature range, and to less than 6 mV per second over the $-25^{\circ}C$ to $+75^{\circ}C$ range.

The power requirements for the circuit shown in Fig. 4-3 are predicted as follows. There is a total power consumption of 100 μW for the two amplifiers because of OFF-state power. ON-state power requirements are only 20 μW because of the low duty factor used in this application. The power consumed by the load resistor of the first amplifier and for capacitor charging must also be included. The current supplied to the 5-K load of the first amplifier must be less than 1 mA when this amplifier is ON, since the input voltage is limited to four volts. The maximum average power required by this resistor is therefore less than 5 μW. The maximum capacitor charging rate is four volts per second (since the integrator is unity gain and the maximum input voltage is four volts). This results in a maximum average current into the total 1-μF load capacitance of 4 μA and therefore a maximum average power requirement of 28 μW. It will be shown in Chapter V that the clock, one-shot multivibrator, and gate driver require a total power of 100 μW under these conditions. The sum of these terms shows that the total power requirement for the sampling-mode integrator should be approximately 250 μW. Approximately 40 percent of this total represents gated-amplifier quiescent power consumption, and so this is one application where elimination of the network that compensates amplifier input current would result in significant average-power reduction.

The system shown in Fig. 4-3 has not been tested. However, experience with several similar connections used in other applications indicates that the predicted performance is realistic.

The advantages and disadvantages of sampling-mode integration compared with conventional analog integration are summarized as follows:

1. The versatility of the sampling-mode integrator is greater. For example, a hold mode (the output maintains a fixed value independent of input) can be introduced without any switching of analog signals by eliminating sampling pulses. The integrator scale factor can be changed by changing sampling rate, and this feature introduces additional flexibility since it permits time scaling. The integrator can also be pulsed ON non-periodically, in which case it functions as a time summation circuit (the value of a variable at selected time instants can be totalized over any number of instants). It will be seen that this versatility is used in more complex operations.

2. If only integration is required, the complexity of the sampling-mode integrator is greater than that on conventional analog integrator. Some simplification is possible if the function of the first amplifier (Fig. 4-3) can be incorporated into the circuitry supplying the signal for integration.

3. Bandwidth is significantly reduced by sampling-mode operation.

4. Drift rate is increased to possibly three times that of a conventional analog integrator.

5. With the values used in this section, the power is reduced by at least a factor of 50 compared with even a continuously ON gated-amplifier integrator. This represents a reduction by approximately three orders of magnitude compared with other operational amplifiers which consume more power than a continuously ON gated amplifier.

E. ANALOG-TO-DIGITAL CONVERSION

Analog-to-digital (A-D) conversion is a common requirement in space data-processing systems, for the basic reason that most sensor signals are analog quantities while telemetry of experimental variables

uses digital coding techniques. It is evident that a conversion is required at some point in the data-processing system.

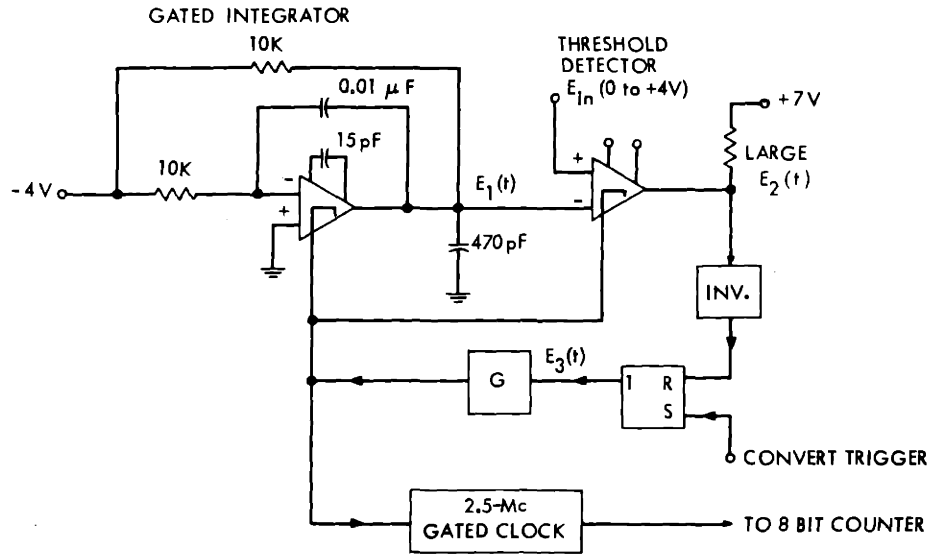
Several methods for A-D conversion can be implemented with gated amplifiers. For example, the sampling-mode integrator described in the last section can be used as a staircase generator. The number of steps required to equalize the value of the staircase and the value of the variable being converted can be counted to provide A-D conversion. A system of this type was tried with an early breadboard gated-amplifier circuit and, while no detailed measurements were performed, 8-bit accuracy was demonstrated.

An improved method, in the sense that more rapid and accurate conversions are possible, is illustrated in this chapter. Two basic techniques, gated (as opposed to sampling-mode) integration and voltage-to-time conversion, are used to implement A-D conversion, and these techniques are also discussed. The method involves generation of a ramp with a known slope and measurement of the time required for this ramp to reach the level of the variable being converted. A clock is counted for this time interval to accomplish conversion. The system used for purposes of illustration is shown in Fig. 4-4.

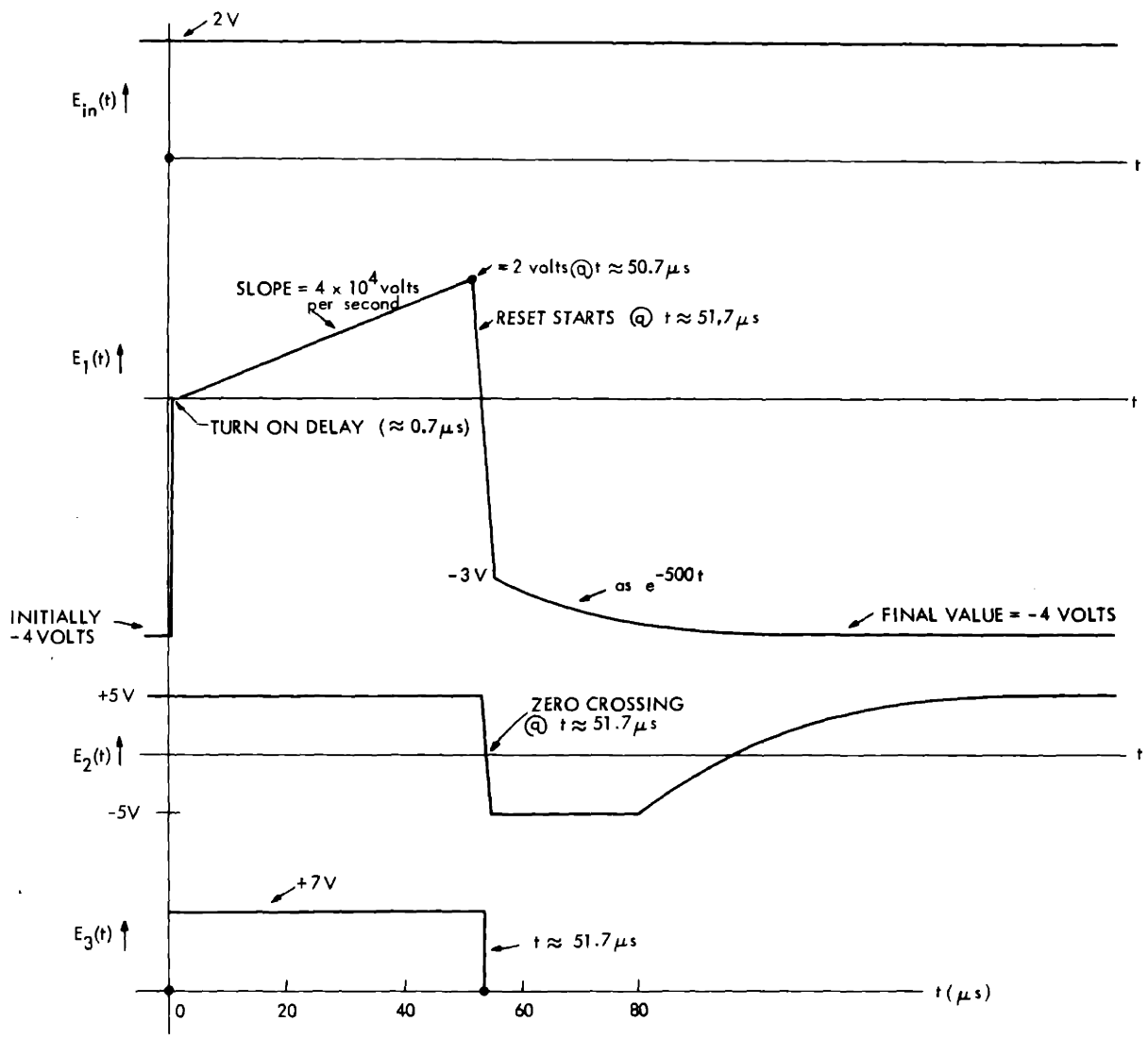
The first gated amplifier is connected so that it functions as an integrator when ON. With this amplifier ON, the 10-K resistor connected between the amplifier output and the -4 volt reference is a load resistor and does not influence the amplifier transfer function. The 0.01-μF feedback capacitor and the 10-K input resistor connected to the -4 volt reference produce an output voltage with a rate of change equal to 4×10^4 volts per second when the amplifier is ON. (The transfer function relating output to input with this feedback network is $-\frac{10^4}{s}$).

A convenient method for stabilizing a gated amplifier connected as an integrator is to use a 15-pF compensating capacitor and a 470-pF load capacitor to ground. This combination has not been investigated analytically, but experimentally it provides absolute stability with any integrator connection which has been tried.

The two 10-K resistors are used to provide the correct initial conditions (in this case zero integrating-capacitor voltage) when the



a) A-D Converter Circuit



b) Waveforms

Fig. 4-4 A-D Conversion with Gated Amplifiers

amplifier is OFF. The application of initial conditions is generally simplified with gated-amplifiers as compared to operational amplifiers because the need for external switching is eliminated.

It is assumed in Fig. 4-4 that the system is initially at rest, with zero voltage across the 0.01-μF integrating capacitor. At time $t = 0$, a voltage level $E_{in}(t)$ of +2 volts is present, and it is assumed that this value remains fixed during the conversion interval. A signal initiates the conversion cycle at $t = 0$ by setting the flip-flop, thus gating both amplifiers ON. The output of the first amplifier is a ramp with a slope of 4×10^4 volts per second, and this ramp starts at approximately $t = 0.7$ μs because of the turn-on delay of the first amplifier.

The second gated amplifier is used open loop as a threshold detector, and the output is initially biased positive through the large resistor connected to +7 volts. The amplifier output maintains this state until the signal applied to its negative-gain input terminal (the ramp) exceeds that applied to its positive-gain terminal (the voltage being converted). This event occurs at time $t = E_{in} \times 25$ μs + 0.7 μs, or 50.7 μs in this example. The second amplifier then starts to change state and, because of time delays in the amplifier, its output passes through zero voltage 1 μs after the two inputs are equal. This zero crossing is applied to a single transistor inverter that is used to sharpen up the amplifier transition, and the inverter output is used to reset the flip-flop. The time the flip-flop spends in the 1 state is equal to $E_{in} \times 25$ μs + 1.7 μs or 51.7 μs for the postulated two-volt input. Since the flip-flop signal gates both amplifiers, this system is self-optimizing in that the amplifiers are ON (and thus consuming maximum power) only for the time interval required to convert a particular voltage level.

In the example shown, the flip-flop signal also controls a clock which supplies pulses at a 2.5-Mc rate to an 8-bit counter. Thus, the count stored at the end of a conversion cycle should be equal to $2.5 \times [E_{in} \times 25 + 1.7]$, ±1 count. An error of four counts is introduced because of amplifier delays, but these delays are repeatable. It is possible to compensate for delays by initially resetting the counter to -4 rather than to zero.

The clock-pulse burst can be generated in a number of ways. For example, a 2.5-Mc clock followed by a two-input AND gate could be

used. This would add to system average power consumption since a 2.5-Mc clock might require as much as 5 mW of power. Another approach is to gate the supply voltage to a clock circuit in such a way that the clock requires power only when the conversion is in progress. It is even possible to introduce a variable turn-on delay with such a clock, and the delay can be adjusted to compensate for the 1.7-μs circuit delay. Clock circuit details are presented in Chapter V.

After both amplifiers turn OFF, the voltage across the 0.01-μF capacitor discharges to zero through the two 10-K resistors with a 0.2 ms time constant. The capacitor voltage is reduced to zero within 2 ms, and the system is ready to perform a new conversion at any later time.

Power requirements for this system are computed as follows. Assume conversions are performed at the maximum allowable rate of 500 complete 8-bit conversions per second. Amplifier ON time is determined by input voltage and an expected value of two volts is assumed. The ON-state power for both amplifiers is 30 mW multiplied by the 0.025 duty factor under these conditions, or 750 μW. An assumed clock power requirement of 5 mW when this circuit is ON adds another 125 μW. Power requirements are increased because of current in the two 10-K resistors, and it is assumed that this current as well as capacitor current is supplied from 7 volts, since the -4 volt reference supply would probably be generated from a 7-volt supply. These elements contribute an average power consumption of less than 200 μW. The requirements of the flip-flop, gate driver, and inverter should be less than 200 μW. The sum of these terms yields a total expected power consumption of approximately 1.25 mW.

This circuit was not tested specifically, but an identical voltage-to-time conversion technique is used in a multiplier-divider system described later in this chapter. The results of the multiplier-divider tests indicate that rms errors of less than one bit should be possible in the case of 10-bit conversions with this basic system simply by increasing the clock frequency.

This basic conversion technique is not new; in fact, it is used in several commercially-available digital volt meters. I have also built an essentially identical converter employing conventional operational amplifiers for use in a prototype space system. The complexity of a

system using conventional circuitry is greater than that of a system using gated amplifiers since accurate analog switches must be constructed to perform the required switching. The power consumption of conventional systems is at least a factor of 100 higher.

This system also illustrates gated integration and voltage-to-time conversion, and these basic operations are often used in more complex systems. A gated integrator simply implies the use of a gated amplifier as an analog integrator. The advantages include ease of reset to specific initial conditions and the power economy made possible by gating.

The duration of the logical 1 output of the flip-flop is proportional to E_{in}. A pulse with duration proportional to the ratio of two variables can be generated if the input to the gated integrator (shown as a constant -4 volts in Fig. 4-4) is made a second analog variable. This is the general case of voltage-to-time conversion.

F. LOG A-D CONVERSION

The system described in the preceding section provides linear A-D conversion; the binary number stored in the counter at the end of a cycle is linearly related to the value of the voltage being converted. Log conversion, where the final binary number is proportional to the log of the voltage being converted, is preferable in certain applications. Consider, for example, a situation where an input variable with a range of 0.4 volt to 4 volts is present and where a conversion which yields a round-off error of less than 10 percent of the magnitude of the variable is required. Since the minimum value of the variable is 0.4 volt, a linear conversion resolution of 40 mV is required, and 7 bits are necessary to represent the variable.

Conversion of the form

$$n = 13 \ln \frac{E_{in}}{0.4}$$, where n is the binary number and E_{in} is the voltage being converted, permits a 5-bit representation with a round-off error of less than 8 percent. The reduction in the number of required bits is significant, particularly in deep-space probes where power considerations limit telemetry rates to several bits per second.

Log conversion can be realized with a system similar to that shown in Fig. 4-4 if the gated integrator is replaced with a gated amplifier used to generate an exponential that increases with time. In order to provide the conversion mentioned above, a 1-Mc clock could be substituted for the 2.5-Mc clock shown in Fig. 4-4, and the ramp generator replaced with a circuit which generates the voltage

$$E_{out} = 0.4\, e^{7.7 \times 10^4 t}, \quad t \geq 0$$

It is possible to generate this type of increasing exponential with the gated-amplifier circuit shown in Fig. 4-5. The amplifier itself is connected as a non-inverting gain-of-2 amplifier from the positive-gain input terminal to the output. On the assumption of an ideal amplifier, the relationships are

$$0.01\,\mu F \times \frac{dE_1(t)}{dt} = \frac{E_{out}(t) - E_1(t)}{1.3\ K} \quad \text{and} \quad E_{out}(t) = 2E_1(t)$$ with the amplifier ON, yielding

$$\frac{dE_1}{dt} = 7.7 \times 10^4 E_1, \text{ or } E_1 = k e^{7.7 \times 10^4 t},$$

where k is the initial voltage on the capacitor at the time of gating. These equations neglect slight loading from the 220-K resistor used for initial-condition biasing.

This is a rather interesting feedback connection, in that negative feedback is used to control accurately the gain from the positive-gain input terminal to the output, and then positive feedback is used around the resultant stable-gain amplifier to generate a growing exponential.

The circuit shown in Fig. 4-5 was constructed. No particular care was taken to select component values, and 10-percent tolerance passive components were used for a quick test. A 32-μs gating pulse was used, and the bias voltage varied until an output of 4 volts was obtained 30 μs after amplifier turn ON. The resultant output waveform is shown in the photograph of Fig. 4-6.

There seems to be no easy way to determine how closely this waveform approximates the desired exponential, other than building the entire log A-D converter and measuring accuracy. However, the oscilloscope photograph indicates agreement to within the tolerance of the components used in the experiment.

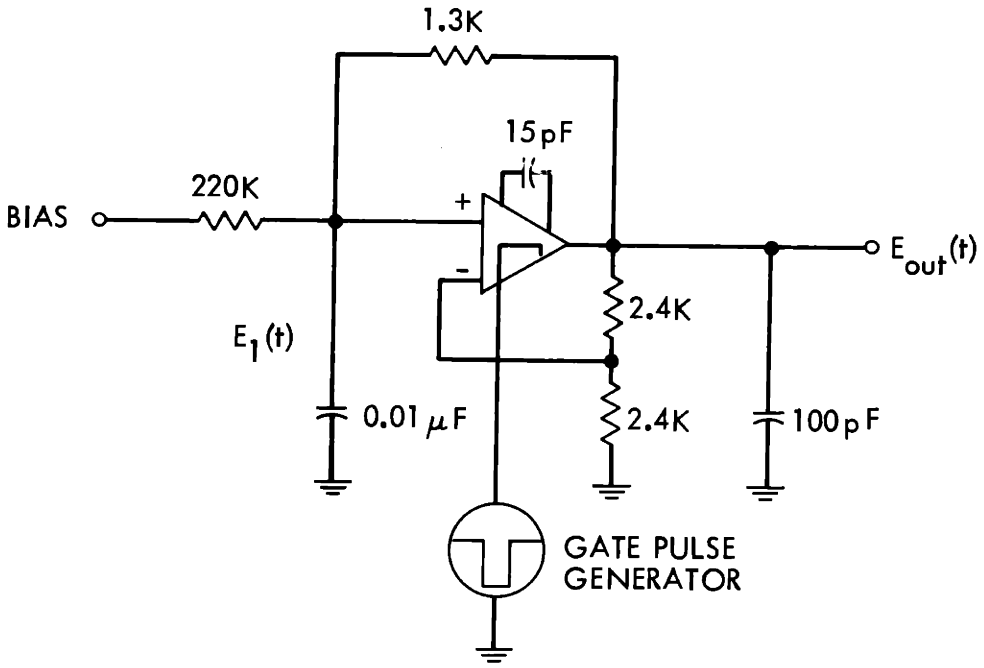


Fig. 4-5 Increasing Exponential Generator

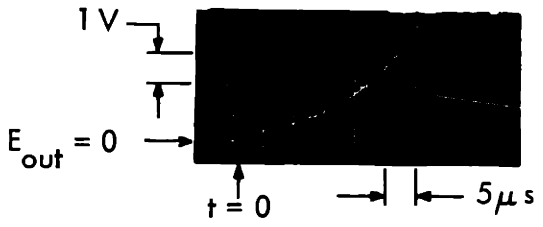


Fig. 4-6 Output of Circuit Shown in Fig. 4-5

G. FUNCTION GENERATION

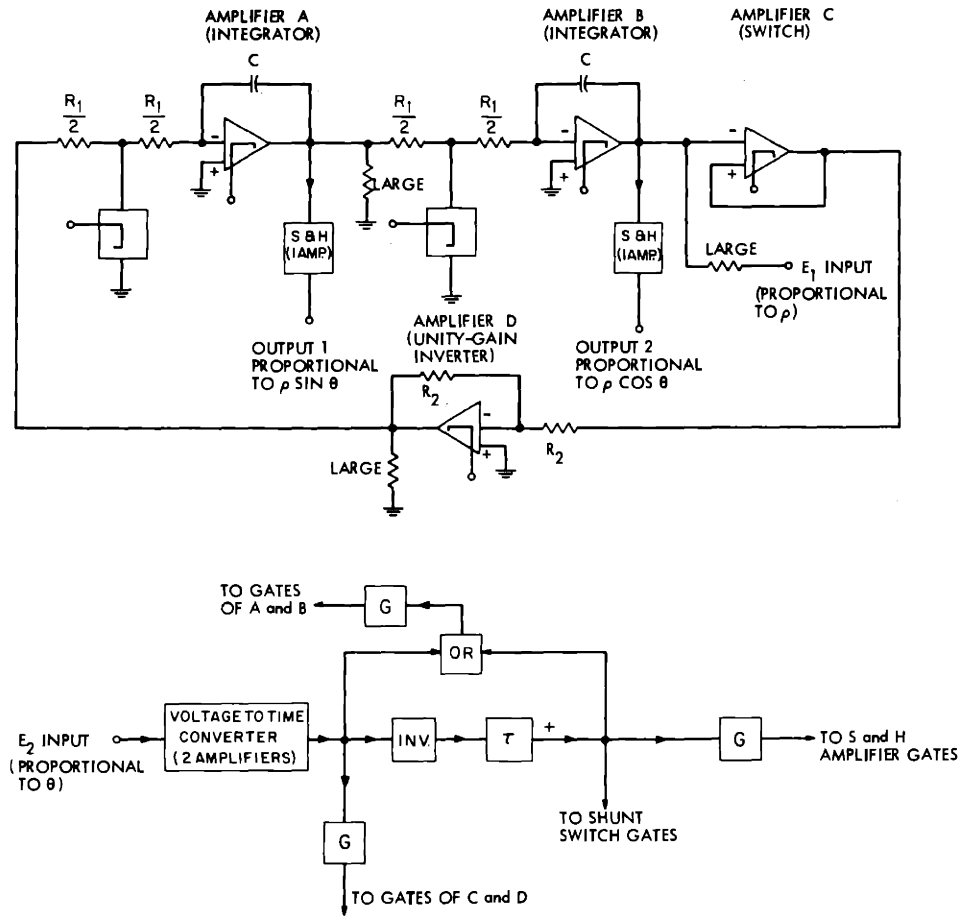
Generation of functions of the form $Y = F(X)$ is a common data-processing problem, and gated amplifiers offer at least two methods for the generation of most functions where Y is a single-valued function of X. One involves the use of cascaded gated integrators to generate outputs proportional to t, t^2, t^3, ... A linear combination of these outputs provides a Taylor-series expansion of the required function with time as the independent variable. The expansion is sampled at a time proportional to X (determined by a voltage-to-time converter) in order to accomplish function generation.

A second possibility exists if a differential equation with a solution $Y = F(kt)$ can be found. The equation is simulated with gated amplifiers using essentially standard analog simulation techniques, and the solution is sampled at a time proportional to X. The choice between these two methods is made on the basis of the relative ease of expansion of the required function. Only the second method is illustrated with examples in this section.

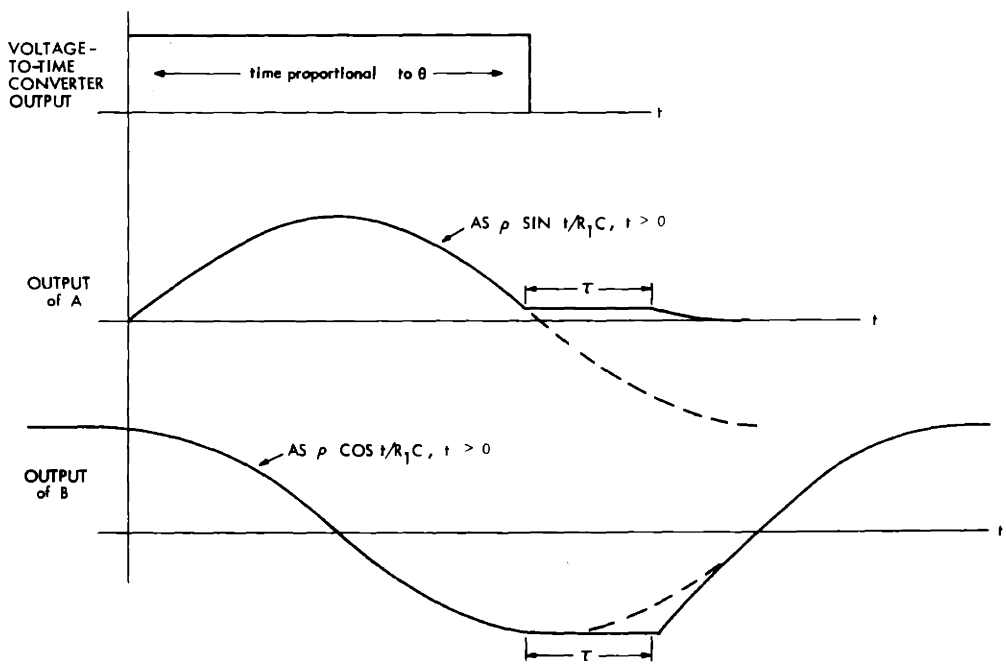
Either method can also be used to generate functions of the form $Y = F(\frac{X}{Z})$, since it is possible to generate a pulse with time duration proportional to the ratio of two variables. Functions of negative arguments can be generated if some additional logic is included.

One simple case occurs when the desired function is $Y = k_1 e^{k_2 X}$. In this case a four-amplifier system is sufficient. Two amplifiers are used for voltage-to-time conversion, one as an exponential generator similar to that shown in Fig. 4-5, and one as a sample-and-hold circuit. A somewhat more interesting example is the frequently encountered guidance problem of conversion from polar to rectangular coordinates. Given ρ and Θ, $X = \rho \sin \Theta$ and $Y = \rho \cos \Theta$ are required. While the simulation of this function using gated amplifiers has not been investigated in detail, an abbreviated block diagram of a resolver which performs these operations is shown in Fig. 4-7. In this figure, the details of stabilization for the four gated amplifiers are omitted for simplicity.

Operation is described with the aid of the waveforms shown in Fig. 4-7b. Initially, all amplifiers are OFF, and the two shunt switches are open. Equilibrium is reached with a voltage proportional to the ρ



a) SYSTEM FOR GENERATING ρ SIN θ AND ρ COS θ FROM ρ AND θ



b) WAVEFORMS

Fig. 4-7 Resolver Using Gated Amplifiers

input across the capacitor in the feedback path of integrator B, and with zero voltage across the capacitor in the feedback path of integrator A. These voltages are the initial conditions for the system when the amplifiers turn ON.

At time $t = 0$, the voltage-to-time converter is triggered so that its output becomes +7 volts. (The circuit shown as part of Fig. 4-4, with appropriate time-scale adjustment, can be used for the voltage-to-time conversion.) At this time all four amplifiers gate ON and the shunt switches remain open. The differential equation simulated by the four amplifiers is $\frac{d^2X}{dt^2} + \left(\frac{1}{R_1C}\right)^2 X = 0$. With initial conditions as shown, the output of amplifier A is proportional to $\rho \sin \frac{t}{R_1C}$, while the output of amplifier B is proportional to $\rho \cos \frac{t}{R_1C}$. It should be mentioned that amplifier C, which operates as a switch, can be eliminated if solutions of the form $\rho \sin (\frac{t}{R_1C} + \frac{\pi}{4})$ are acceptable.

All amplifiers remain ON until a time proportional to the input variable Θ. At this time amplifiers C and D are gated OFF. These amplifiers are no longer required and turning them OFF reduces average power requirements. Amplifiers A and B remain ON, but shunt switches in the input networks of these amplifiers reduce the current into the feedback capacitors to zero. This causes the integrators to maintain the voltages present at the time the switches close, which are proportional to $\rho \sin \Theta$ and $\rho \cos \Theta$. The values are sampled by two sample-and-hold circuits and these circuits are assumed to require a time interval τ to obtain samples. At the end of the interval τ, all amplifiers are turned OFF and the two switches are opened. The circuit then starts a transient which generates new initial conditions for the next cycle of operation.

The circuit can be used in either of two ways. If ρ and Θ are continuously varying, the circuit can be triggered periodically at some frequency at least 10 times higher than any frequency components of the ρ and Θ variables. The outputs can be low-pass filtered to provide continuous resolution.

A second method is used when new values for $\rho \sin \Theta$ and $\rho \cos \Theta$ are required only at certain specific times, for example when trajectory

corrections are attempted. In this case the circuit is triggered when required on a single-cycle basis.

Accuracy and power requirements are largely dependent on the amount of time spent in one cycle of computation. While this system has not been built, it is similar to other systems which have been tested such as the multiplier-divider described later in this chapter. Experience with the multiplier-divider and other similar systems indicates that errors of less than 10 mV should be possible for time-invariant inputs, and that the power consumption should be on the order of 1 mW for low-frequency operation.

This is an example of a gated-amplifier system which is less complex than a system using conventional analog techniques. One commonly used resolver implementation performs the sine-cosine expansion with nonlinear diode networks, and uses quarter-square multipliers to provide multiplication by ρ. This approach requires at least 9 operational amplifiers (loading considerations can increase this number to 15) and 6 nonlinear diode networks (2 for the sine-cosine expansion and 2 in each of the multipliers). The gated-amplifier realization requires 8 amplifiers, and the required ancillary circuitry is less complex and more stable than diode networks.

One reason for the simplification afforded by the gated-amplifier method is that the two multiplications required for resolution are accomplished by control of initial conditions. It is evident that this approach can be used to generate any function of the form $Z = YF(X)$ if $F(X)$ can be represented as the homogeneous solution of a linear differential equation.

H. DIGITAL-TO-ANALOG CONVERSION

Two of the more complex systems, a digital-to-analog (D-A) converter and a multiplier-divider, were constructed and tested as part of the experimental program. These systems were selected for testing for the following reasons:

1. They include all the basic techniques described earlier in this chapter such as sampling, leak back, voltage-to-time conversion, integration, and switching, and thus serve to demonstrate

the feasibility of these methods as well as that of the particular overall system.

2. These two operations are representative of the degree of difficulty associated with typically encountered data-processing requirements.

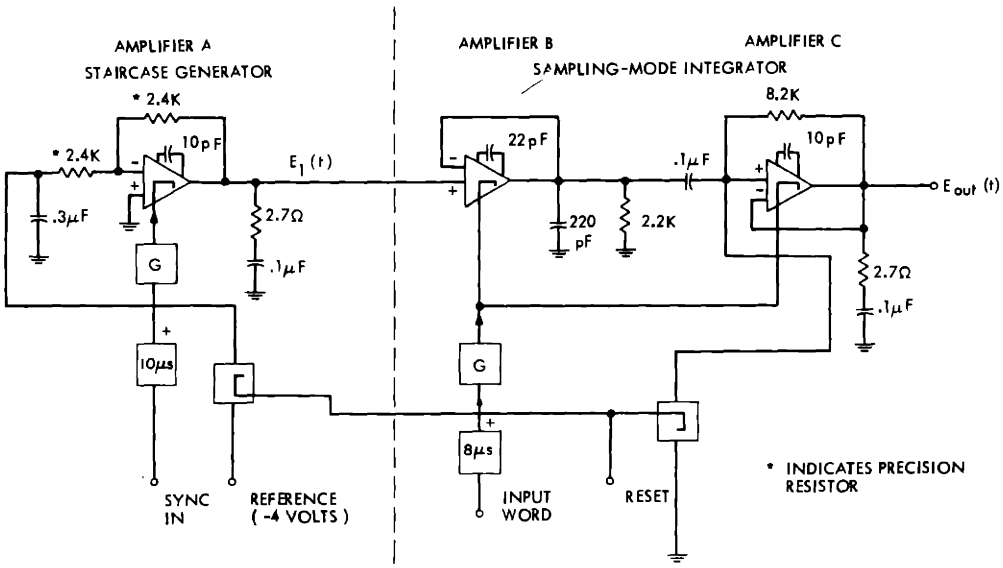
3. These systems provide adequate testing of most ancillary circuits required for system realization with gated amplifiers.

4. Both systems can be constricted with the number of amplifiers built for the experimental program.

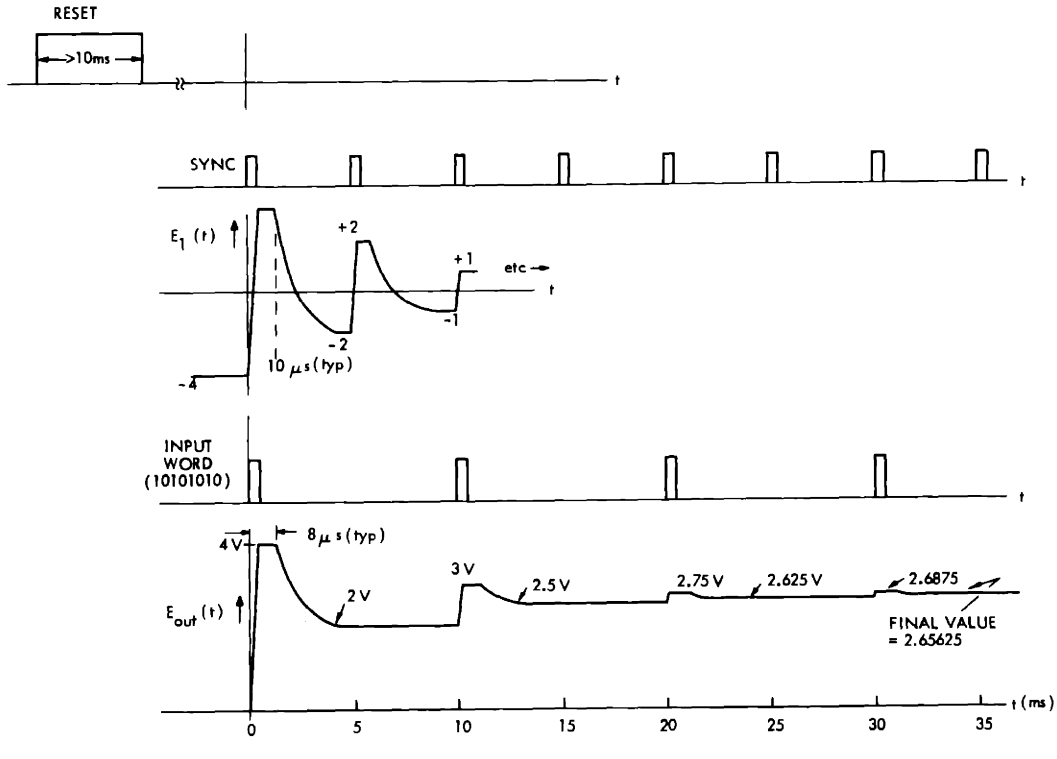
The D-A converter described in this and the following section has several interesting features. It provides direct conversion of sequential digital data, which is the form generally provided by telemetry transmissions. No temporary flip-flop storage is required and this results in a less complex realization than other methods. The actual time spacing between subsequent bits is unimportant. However, a simultaneous synchronizing pulse train which provides pulses at every possible bit location is required. No circuit modifications whatever are required to change the number of bits which the system converts. If four synchronizing pulses are supplied to the system it functions as a 4-bit converter; if 10 synchronizing pulses are applied it functions as a 10-bit converter.

The interconnection used for this system is shown in Fig. 4-8. Circuit operation depends on the generation of a waveform which has values of 4, 2, 1, 0.5, ... volts at the times when a bit in the input word is present. A connection similar to the sampling-mode integrator described in Section D totalizes the values of the waveform at all times when a logical 1 is present in the input word. Leak back in the totalizing circuit provides a gain of one half, with the result that the most significant bit has a value of 2 volts, a level compatible with maximum gated-amplifier output voltage.

Details of the process are described with the aid of the waveforms included in Fig. 4-8. (The time axis is distorted in these waveforms to show clearly details of operation during the ON time.) An 8-bit conversion is used as an example and therefore 8 sync pulses are



a) SYSTEM FOR D-A CONVERSION



b) WAVEFORMS

Fig. 4-8 D-A Converter Using Gated Amplifiers

shown. A reset pulse is applied to the system at some arbitrary time prior to the start of the conversion cycle. This reset pulse charges the two capacitors connected to amplifier A to the -4 volt reference through a shunt switch. The two capacitors connected to amplifier C are discharged simultaneously through a second shunt switch. The reset pulse is applied for an interval greater than 10 ms to insure completion of the reset transient.

Amplifier A is considered first. This amplifier is gated ON for a 10-μs interval following the application of each sync pulse, and is connected as an inverting unity-gain amplifier with leak back. Minus 4 volts is stored on both capacitors at the time the first sync pulse is applied. Since the amplifier is connected as a unity-gain inverter, its output is forced to +4 volts, and the 0.1-μF capacitor charges toward this value when the amplifier is ON. The ON state is maintained for 10 μs in order to complete charging of the 0.1-μF capacitor and to insure the correct output voltage for the summing circuit. There is some decay of the -4 volts held on the input capacitor during the time that amplifier A is ON because of current supplied to the 2.4-K input resistor, and this decay causes a 1.5-percent change in the voltage on the input capacitor. The output of the amplifier tracks this change. However, this voltage decay is controlled only by an r-c time constant and the time that A is ON, and is therefore repeatable. The decay can be compensated for by slight modification of the reference voltage and thus introduces negligible error.

Amplifier A gates OFF 10 μs after the leading edge of the first sync pulse, and at this time -4 volts is stored on the 0.3-μF capacitor and +4 volts is stored on the 0.1-μF capacitor. A leak-back process reaches equilibrium with -2 volts stored on both capacitors. The time constant associated with leak back is 0.36 ms, so that the leak-back transient is completed before the second sync pulse is applied.

When amplifier A gates ON in response to the second sync pulse its output is driven to +2 volts. The leak back following this cycle reaches equilibrium with -1 volt stored on both capacitors. The pattern repeats for 8 cycles, (at least in the case of 8 sync pulses as shown) with successive voltages of +4, +2, +1, +0.5, ... present at the output of amplifier A during the times this amplifier is ON.

Amplifiers B and C are operated in a modified sampling-mode integrator connection, similar to that shown in Fig. 4-3. These two amplifiers are gated ON only following application of a 1 pulse in the input-word pulse train, and this pulse train is assumed to be supplied in natural-binary code with the most significant bit first.

The two storage capacitors associated with amplifier C are discharged during reset. The first binary digit is 1 in the example shown (101010), and therefore amplifiers B and C are gated ON with the first sync pulse. At this time the output of amplifier A is +4 volts, and this value is transferred to the positive-gain input of amplifier C forcing the amplifier to store +4 volts on the 0.1-μF capacitor connected to its output.

Amplifiers B and C are gated OFF 8 μs after application of the first pulse (this time is purposely less than the ON time of amplifier A to insure that the output of A is the desired value when B and C turn OFF), and at this time 4 volts is stored on the capacitor connected to the output of amplifier C, while zero is stored across the capacitor at the input of this amplifier. Leak back between these two capacitors results in a final voltage of +2 volts on both capacitors. The time constant of this leak-back transient is 0.52 ms.

Amplifiers B and C are not gated ON at the time of the second sync pulse (the second binary digit is 0), but are gated ON with the third sync pulse. At this time the voltage across the capacitor at the input of amplifier C is +2 volts while the output of amplifier A (and thus B) is +1 volt. Therefore, +3 volts is stored on the capacitor connected to the output of amplifier C. Leak back during the interval between the third and fourth sync pulses results in a final value of 2.5 volts stored on both capacitors. The process continues, adding a voltage equal to $4(1/2)^n$ volts to the output for a logical 1 value of the n^{th} bit in the input word. In the example shown, the final value is 2.65625 volts.

I. TEST RESULTS WITH THE DIGITAL-TO-ANALOG CONVERTER

The system shown in Fig. 4-8 was constructed with ancillary circuits and feedback components for the gated amplifiers located on two special-purpose interface boards. Simple grounded-emitter transistors were used as the shunt switches.

The three amplifiers used were balanced for zero drift referred to the input prior to connection to the system. Only two adjustments were performed on the completed system. The 0.3-μF capacitor located at the input terminal of amplifier A was trimmed so that successive sync pulses provided reduction of the voltage stored on the capacitors by exactly a factor of one half. The system was then operated normally with a 00000000 digital input word applied. Any output in this case should be a result of offsets in the switch which discharges the output capacitor. An offset of 6 mV was noted and this value is consistent with the saturation voltage of the transistor used as the switch. It should be possible to reduce this offset to less than 100 μV through use of an improved switch as described in Chapter V.

A 11111111 digital input word was applied to the system and the reference voltage adjusted to produce an output of 3.990 volts. This corresponds to the desired output for this input (3.984 volts) plus the 6-mV switch offset. This technique permits elimination of the switch offset from the experimental results, since this offset appears as a 6-mV term added to every output voltage.

The instrumentation used to measure output voltage was identical to that used for the sample-and-hold circuit, a Keithley model 610B electrometer used as a preamplifier for a digital voltmeter. In contrast to the case of the sample-and-hold circuit where comparisons between input and output were made and therefore only repeatability was important, the accurate measurement of errors of the D-A converter requires linearity of the measuring equipment. No standard was available to permit calibration, but experience with the test equipment indicates that the errors inherent to the measurement method are 2 mV to 3 mV.

The system was then tested for 29 different digital input words. (These were the only possible input words which could be generated with the available test equipment.) The maximum deviation from a +6 mV error (expected because of switch offsets) was 5 mV, and the rms deviation was 2 mV. The tests were repeated after one week of continuous operation (with no readjustment of any kind) and identical error statistics were obtained.

The results indicate that the system shown in Fig. 4-8 is sufficiently accurate for 8-bit conversion even with the 6-mV switch offset, since the least significant bit in this case corresponds to a voltage of 15.6 mV. If a better switch were used, the expected conversion error would be less than the value of the least significant bit of a 10-bit conversion.

The reason for this type of accuracy is that most system errors show up only as scale-factor changes and are therefore eliminated by adjustment of the reference supply voltage. Examples of errors included in the category are:

1. Deviations from the ideal gain of -1 for amplifier A.
2. Discharge of the 0.3-μF capacitor connected to amplifier A during the ON time.
3. Dielectric absorption in all capacitors.
4. Finite common-mode rejection ratio of amplifiers B and C.
5. Changes in the voltage across the capacitor connected to the input of amplifier C as a consequence of current through the 8.2-K resistor during the ON time.
6. Capacitor voltage changes because of charge dump at turn OFF are at least partially compensated.

The only significant source of error which cannot be compensated for is drift referred to the input of the amplifiers. Assume that all amplifiers have an input drift equal to E_d. This is a realistic assumption since the drift performance of all amplifiers is similar for either variations in temperature or variations in supply voltage. This drift causes a deviation from the ideal output voltage in the case of amplifier A of $1.5E_d + 0.5\,nE_d$ on the n^{th} cycle. Amplifiers B and C each contribute a direct error equal to E_d on each cycle. The expected error is predicted by summing the magnitudes of these errors for every cycle with a logical 1 present in the input word, and the resultant sum is reduced by a factor of two because of the leak-back attenuation associated with amplifier C. Maximum error will occur for a 11111111 input, and the magnitude of this error should be approximately $25E_d$ for this input. This calculation predicts a maximum error of ±2.5 mV for an amplifier drift of ±100 μV, the typical drift expected over a $0^{\circ}C$

to +50°C temperature range. While this system was not temperature tested, the supply voltage was changed in order to cause a 100-μV drift. No measurable change in the error statistics was observed.

In addition to the errors listed above, there is another error which increases proportionally to the time that the output is held following completion of conversion. This drift rate is 0.4 mV per second for the maximum room-temperature OFF-state leakage current of 5×10^{-11} A.

Power consumption for the system is a function of the input word, since the voltage change across the capacitors connected to amplifier C and the time this amplifier is ON depend on the input. Worst-case power consumption occurs for a 11111111 digital input word. The system was tested by repeatedly applying a 11111111 input during a 40-ms interval and then resetting for a 40-ms interval. This results in an average conversion rate of 100 bits per second. In the experimental configuration the power required to reset the capacitors associated with amplifier A to the reference voltage and the power required to activate the switches was supplied by test equipment and is not included in the following calculation. This power is less than 25 percent of the total.

The remaining system power consumption is calculated by first deriving the energy required during one complete 80-ms conversion cycle as follows:

1. The total amplifier ON time for all three amplifiers is 210 μs per cycle, and this results in an energy requirement of 3.5 microjoules.

2. OFF-state power requirements for the 3 amplifiers add 12 microjoules per cycle.

3. The total charge supplied to capacitors is 2.4 microcoulombs (0.6 μF x 4 volts). This requires 16.8 microjoules from the +7 volt supply.

4. Approximately 1 microjoule per cycle is dissipated in various resistors.

5. The logic circuits require 12 microjoules per cycle.

The total energy per 80-ms cycle from the sources listed above is 45 microjoules so that the average predicted system power requirement is 560 μW.

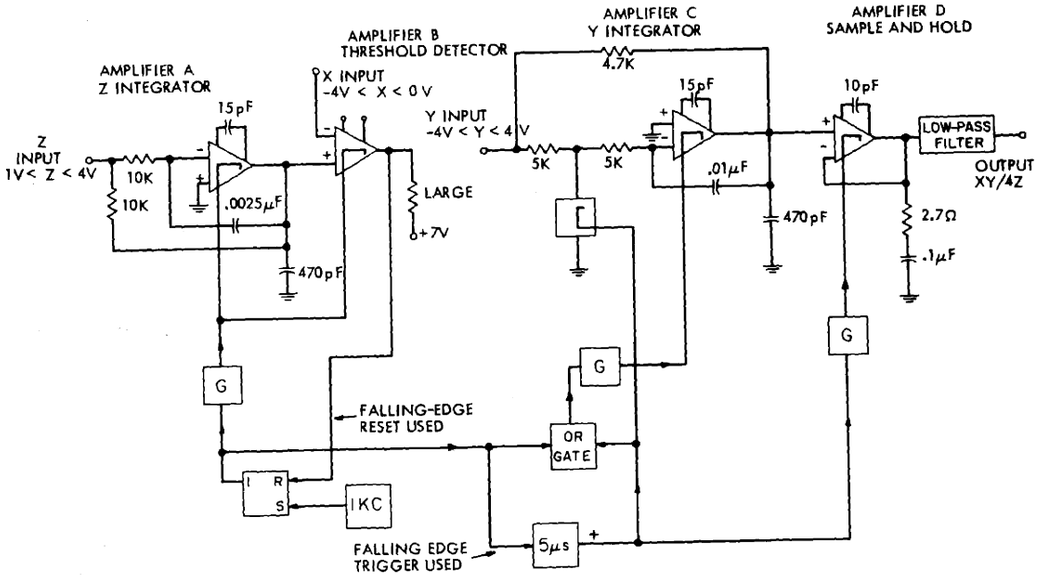
The measured power consumption under these conditions was 700 μW, and the difference between these two figures has never been completely resolved. Some of the difference is probably a consequence of moderate overshot on various amplifier outputs which increases power because of increased average output current.

J. MULTIPLIER-DIVIDER

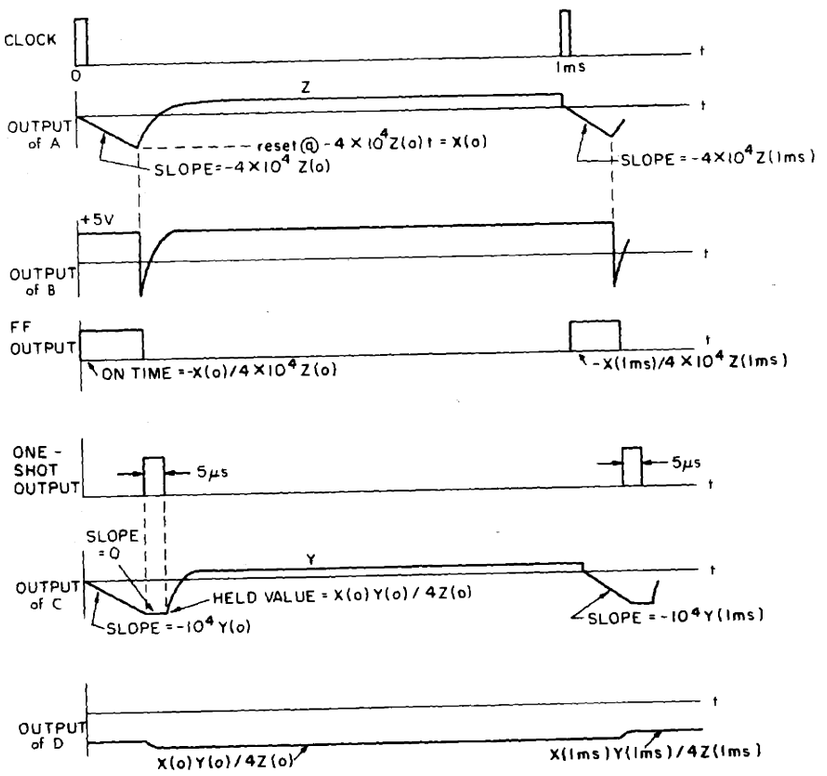
The second gated-amplifier system which was tested is a multiplier-divider. The system is shown diagramatically in Fig. 4-9. This system provides ratios of the form $\frac{XY}{Z}$, where X, Y, and Z are all analog variables and is a type which is commonly known as a two-quadrant multiplier-divider. In this system, Y can have any value between ±4 volts, but the X variable is limited to a single polarity. The range of the Z variable is restricted to the range of 1 volt to 4 volts in order to prevent saturation because of division by too small a number. The restriction to single polarity of the X variable can be circumvented with additional circuitry, and details of one method for accomplishing this are presented later in this chapter.

The basic operation of this circuit is as follows. A voltage-to-time conversion is performed and this conversion is essentially identical to that shown in Fig. 4-4, except that the integrator is supplied with a variable input rather than the constant -4 volts shown in Fig. 4-4. The result is that a pulse with a duration proportional to the ratio $\frac{X}{Z}$ is generated. A second integrator with an input equal to Y is gated ON for a period proportional to $\frac{X}{Z}$. This integrator provides a final output proportional $\frac{XY}{Z}$ and this output is sampled. The system is operated repetitively at a frequency approximately 10 times higher than expected input frequencies and the sampled signal is filtered to provide continuous multiplication-division.

Details of system operation are explained with reference to the waveforms included in Fig. 4-9b. The circuit is triggered periodically at a 1-Kc rate. This rate was selected as a compromise between average power consumption and maximum allowable input frequencies. The first clock pulse shown in Fig. 4-9 occurs at time $t = 0$. At this time the three input variables are assumed to have values of X(0),



a) BLOCK DIAGRAM



b) WAVEFORMS

Fig. 4-9 Multiplier-Divider Using Gated Amplifiers

Y(0), and Z(0), and it is further assumed that the three inputs remain constant from $t = 0$ to at least $t = 100\ \mu s$.

Gated amplifiers A and B are combined with a flip-flop in a voltage-to-time conversion loop. With the element values indicated in Fig. 4-9 it can be shown that, aside from circuit delays, the length of time that the flip-flop remains in the logical 1 state is $\frac{-X(0)}{4 \times 10^4 Z(0)}$. The element values are selected with the assumption that the X and Z variables are limited to the ranges $1V < Z < 4V$, and $-4V < X < 0$. The maximum length of the flip-flop output pulse is thus limited to 100 μs.

Gated amplifier C is connected as a gated integrator. At time $t = 0$ this amplifier is gated ON and at this time the voltage across the feedback capacitor is zero because of the resistors connected around the amplifier. The switch included in the input network of this integrator is open at $t = 0$ so the output of amplifier C becomes a ramp with a slope equal to $-10^4\ Y(0)$ volts per second. At time $t = \frac{-X(0)}{4 \times 10^4 Z(0)}$, amplifiers A and B are gated OFF since they are controlled by the flip-flop in the voltage-to-time converter. These amplifiers are no longer required and gating them OFF reduces power consumption. The flip-flop transition from 1 to 0 triggers a 5-μs one-shot multivibrator. The gate of amplifier C is controlled by the logical combination of a flip-flop 1 OR a 1 from the one-shot and thus amplifier C remains ON until $t = \frac{-X(0)}{4 \times 10^4 Z(0)} + 5\ \mu s$. However, the shunt switch in the input network of amplifier C shorts out with the one-shot pulse so that a voltage equal to $\frac{X(0)\ Y(0)}{4Z(0)}$ is held at the output of amplifier C during the 5-μs interval. This value is sampled by gated amplifier D, which is gated directly from the one-shot.

At the end of the first cycle of operation the voltage stored on the 0.1-μF hold capacitor connected to amplifier D is $\frac{X(0)\ Y(0)}{4Z(0)}$. It should be noted that while a time interval of 7 μs has been suggested for sampling with a 0.1-μF capacitor, this time is required only if a full 8-volt change is expected across the hold capacitor. The allowable frequency of input signals limits the maximum voltage change across the 0.1-μF capacitor to less than 3 volts in this application, and this permits the shorter sampling interval.

The entire cycle is repeated in response to the second clock pulse which occurs at $t = 1$ ms, so that the voltage stored at the output of the sample-and-hold circuit becomes $\frac{X(1\text{ ms})\ Y(1\text{ ms})}{4Z(1\text{ ms})}$ at this time. The process continues, and a new value is computed at 1-ms intervals.

There are obviously a number of possible modifications of the basic system. For example, scale factor can be changed at will by changing the integrating networks. The nominal scale factor of $\frac{1}{4}\frac{XY}{Z}$ was selected in conjunction with the minimum assumed value for Z of 1 volt in order to yield a 4-volt output with $X = -4$ volts, $Y = 4$ volts, $Z = 1$ volt. The frequency of operation can be varied, with frequency increases leading to higher-bandwidth operation at the expense of power dissipation. Similarly, the time interval corresponding to the maximum allowable ratio of $\frac{X}{Z}$ (100 μs in the system of Fig. 4-9) can be changed. Decreasing this time interval leads to lower power dissipation (providing operating frequency is not changed) but increases the errors associated with fixed switching delays.

The technique illustrated in Fig. 4-9 is not the only method that can be used to perform multiplication and division using gated amplifiers. A rather interesting technique involves the use of the log voltage-to-time converter discussed in Section F. Suppose that ratios of the form $Z = \frac{X_1 X_2 \cdots X_n}{Y_1 Y_2 \cdots Y_m}$ are required. A separate log voltage-to-time converter could be used for each variable, and logic circuits arranged so that a pulse is obtained with a time duration proportional to the log of the X's minus the log of the Y's. An exponential generator as shown in Fig. 4-5 would be operated for this time interval and its output sampled at the end of the interval to provide a value proportional to the desired ratio. This method should save amplifiers compared with the method shown in Fig. 4-9 for certain types of ratios. (For example, when some of the terms appear to powers greater than unity, adjustment of relative time scales will provide some of the required products. This method can also be used to generate non-integral powers of a variable.) In the case of a ratio of the form $\frac{XY}{Z}$, however, the method shown in Fig. 4-9 provides a simpler realization.

K. FILTERING TO PROVIDE A CONTINUOUS OUTPUT

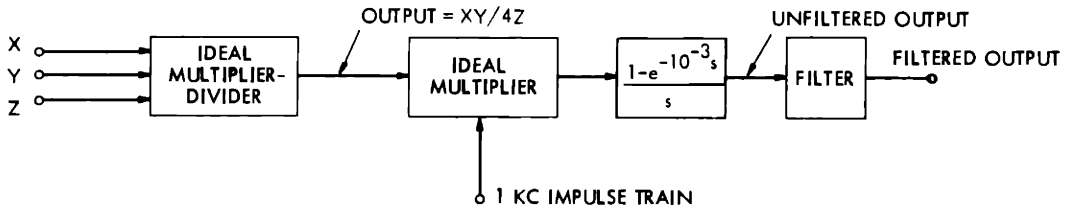
A low-pass filter is shown in Fig. 4-9 and this filter is used to smooth the sampled output. Since one cycle of operation lasts a maximum of 100 μs, the system can be approximately modeled as shown in Fig. 4-10a. In this representation, an ideal multiplier-divider is followed by a sample-and-hold circuit. The sample-and-hold circuit can be represented as an impulse modulator operating at the sampling rate (1 Kc) followed by a network with an impulse response which is a rectangular pulse with a duration equal to the inter-sample interval.

The output of the system prior to filtering for one possible set of inputs that yield an ideal ratio $\frac{XY}{Z} = \sin \omega t$ is shown in Fig. 4-10b. It is assumed that ω is much lower than $2\pi \times 10^3$ radians per second. The sampled output in this case can be represented as the ideal output delayed by an amount equal to one half the inter-sample interval (0.5 ms). In addition to this fundamental there is sampling noise with major components located at the sampling frequency plus and minus ω. It can be shown in general that the sampling operation characteristic of gated-amplifier systems can be represented (at least for any signal with all frequency components low compared to the sampling frequency) as a delay equal to one half the inter-sample interval plus additive sampling noise which is dependent on the exact nature of the input.

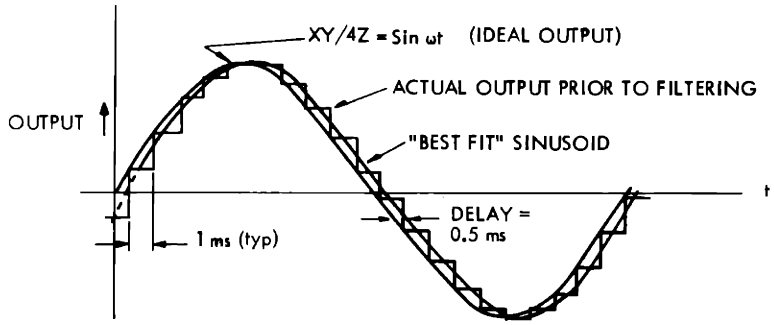
An evident question is what type of filter should be used to best recover the ideal signal. It should be possible to find a physically-realizable filter which (at least if delay is tolerable) completely recovers the ideal ratio providing this ratio contains no frequency components greater than one half the sampling frequency, and a filter transfer function which accomplishes this is shown in Fig. 4-10c.

Realization of the exact filter transfer function shown in Fig. 4-10c is impossible without infinite delay, and furthermore, close approximation of this function is complex. However, one transfer function which has the same general shape as that shown in Fig. 4-10c and which is easily realizable without any active devices is a two-pole filter with a transfer function of the form

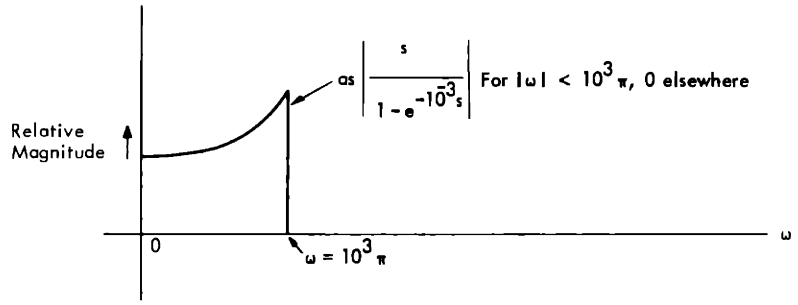
$$\frac{1}{\frac{s^2}{\omega_n^2} + \frac{2\zeta s}{\omega_n} + 1}$$



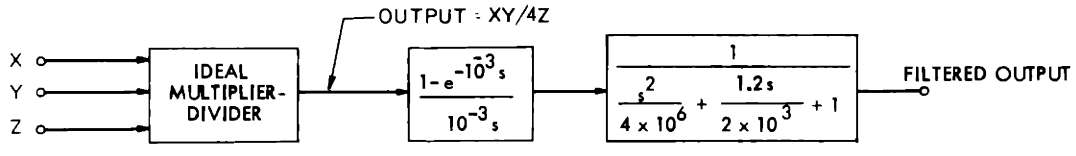
a) Model for System of Fig. 4-9



b) Unfiltered Output, Ideal Output, and "Best Fit" Sinusoid for XY/4Z = Sin ωt



c) Filter which Permits Exact Recovery for all Ratios which contain No Frequencies above $10^3\pi$ Radians Per Second.



d) Model for System of Fig. 4-9 valid for Low Frequencies

Fig. 4-10 Filter Determination for Multiplier-Divider System

This filter can be realized with an r-ℓ-c circuit connected to the output of the sample-and-hold circuit shown in Fig. 4-9. Providing the capacitor used is much smaller than 0.1-μF, no significant loading is introduced. The increase in amplitude at low frequencies which is evident in the ideal transfer function can be approximated by adjusting the damping ratio of the two-pole filter. The attenuation past the natural frequency is proportional to $\frac{1}{s^2}$.

Even better approximations to the ideal-filter characteristics should be possible by cascading several second-order filters. However, since the delay of such a casade filter increases and since loading becomes a greater problem, this approach was not tried.

Selection of ω_n for the two-pole filter involves compromising bandwidth for reduced ripple at the sampling frequency. A value for ω_n of 2×10^3 radians per second was selected as a reasonable compromise. This value insures peak errors from sampling noise of less than 4 percent of the magnitude of a 100-c/s input signal.

After the natural frequency has been selected it is possible to choose a damping ratio in order to match the ideal filter characteristics as follows. The ideal filter characteristics are

$$\frac{10^{-3}s}{1-e^{-10^{-3}s}}$$

(The normalizing factor of 10^{-3} is included to provide a zero-frequency gain of unity.) The magnitude can be approximated by using the series for the exponential, and retaining the first two non-zero terms. The result is that

$$\left| \frac{10^{-3}s}{1-e^{-10^{-3}s}} \right| \approx 1 + \frac{10^{-6}\omega^2}{24}$$

This expression is valid for $\omega < 1.5 \times 10^3$ radians per second. With the aid of this approximation, it can be shown that the amplitude characteristics are matched at low frequencies by a two-pole filter with a natural frequency of 2×10^3 radians per second and a damping ratio of 0.6.

With this type of filter, the function performed by the multiplier-divider can be represented as shown in Fig. 4-10d. This model is

valid only for low frequencies and does not model the high-frequency noise which results from the sampling operation.

The product of the amplitude characteristics of the two frequency-dependent elements is unity within ±3 percent from zero frequency to 10^3 radians per second. The total phase shift in radians is approximately $1.2 \times 10^{-3} \times \omega$, where ω is the frequency into the two frequency-dependent elements, and this expression is also valid to 10^3 radians per second. Thus, for most purposes, it should be possible to model the system of Fig. 4-9 as an ideal multiplier-divider system followed by a pure time delay equal 1.2 ms.

A filter of this type was constructed using a 0.01-μF capacitor, a 25-Hy inductor, and a 56-K resistor. The filter was connected to the output of the multiplier for test purposes. The possibility of using a 25 Hy inductor in a space experiment may seem somewhat remote. However, at least one manufacturer offers a series of variable inductors which are available in values up to 300 Hy. All of these units occupy a volume of less than 1.5 cubic inches. While these inductors cannot be used in high-Q circuits, they seem ideal for heavily-damped filters such as those required for the multiplier-divider. These same inductors could be used as filter elements in any gated-amplifier system where smoothing is required to provide a continuous output, such as the sampling-mode integrator described earlier in this chapter.

L. TEST RESULTS WITH THE MULTIPLIER-DIVIDER

The system shown in Fig. 4-9 was constructed and tested for accuracy and power consumption. The required ancillary circuits were constructed on two interface boards. These boards were interconnected with the four gated amplifiers as shown in Fig. 3-2. No attempt was made to select components, since any variation in feedback-and storage-element values should show up only as changes in scale factor.

The circuit shown in Fig. 4-9 was tested for static accuracy (all inputs time invariant) by applying all 100 possible inputs corresponding to permutations of X = 0, -1, -2, -3, -4 volts, Y = +4, +2, 0, -2, -4 volts and Z = 1, 2, 3, 4 volts. No adjustments of any kind were made prior to testing. The complete results are shown in Table 4-1. If it

Table 4-1

Measured Output Voltages for Multiplier-Divider System

Z (volts) ↓ / X (volts) →	0	-1	-2	-3	-4	Y (volts)
1	-.068	-.990	-1.937	-2.890	-3.848	Y = +4
2	-.058	-.513	-.988	-1.463	-1.939	
3	-.054	-.354	-.670	-.988	-1.304	
4	-.051	-.277	-.511	-.749	-.988	
1	-.032	-.493	-.967	-1.443	-1.918	Y = +2
2	-.029	-.255	-492	-.730	-.967	
3	-.026	-.176	-.333	-.491	-.651	
4	-.023	-.136	-.249	-.371	-.491	
*	ALL VALUES LESS THAN 0.001					Y = 0
1	.035	.493	.967	1.445	1.922	Y = -2
2	.030	.254	.491	.730	.964	
3	.027	.175	.332	.490	.648	
4	.026	.136	.253	.371	.488	
1	.071	.986	1.932	2.886	3.843	Y = -4
2	.062	.512	.985	1.459	1.935	
3	.058	.355	.670	.985	1.302	
4	.055	.275	.511	.748	.985	

is assumed that the scale factor* of the multiplier-divider is such that the output is $\frac{XY}{4.13Z}$, a maximum error of 71 mV occurs for the combination X = 0, Y = -4, Z = 1.

An error analysis for the system of Fig. 4-9 has not been performed. However, the major source of error can be determined from the data shown in Table 4-1. It is highly unlikely that offsets of any kind in amplifiers C or D (Fig. 4-9) are responsible, since these would show up in two ways not evident from the data. First, the output would not be zero for Y = 0, and second there would not be symmetry about Y = 0. The data show excellent symmetry about Y = 0. All outputs for X, Y, Z agree with those for X, -Y, Z within 5 mV. The 5-mV maximum deviation is easily explained in terms of instrumentation errors. The same considerations eliminate shunt-switch offset as a possible cause of the error.

Unless it is assumed that there is some fundamental difference between amplifiers A and C, (highly unlikely because of the extensive testing of all amplifiers) the error cannot be explained in terms of offset in amplifier A. Similarly, d-c offsets in the threshold detector large enough to give errors of the magnitude shown are not substantiated by measurement.

The only realistic possibility is some type of time delay. Experimental evidence excludes the possibility of differences between the turn-on times of amplifiers A and C large enough to cause errors of this magnitude. All logic circuits have transition times and propagation delays under 10 ns, and this could not result in the observed errors. The only remaining possibility is a time delay in the threshold detector, or more accurately, a delay between the time when the two inputs to amplifier B are equal and the time that the flip-flop resets.

The result of such a time delay would be to leave amplifier C integrating for too long a period, so that the system output would be

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* The nominal design-center scale factor for the system shown in Fig. 4-9 is such that the output is $\frac{XY}{4Z}$. The actual scale factor differs from $\frac{1}{4}$ because of the tolerance of the passive feedback components. This difference does not indicate any error, since scale factor can be adjusted at will over a wide range of values.

related to inputs as

$$E_{out} = K_1\left(\frac{X}{Z} + K_2 t_d\right) Y ,$$

where t_d represents the delay time and K_1 and K_2 are constants. In order to explain the measured errors, t_d must have the following properties:

1. The delay time must be a function of the slope of the output of amplifier A, and must vary from approximately 1.0 μs with $Z = 1$ volt to 0.8 μs with $Z = 4$ volts. This is reasonable, since a larger Z input provides greater drive for the threshold detector.

2. An additional term of 0.6 μs is added for $X = 0$ because of the turn-on time of amplifier B. This term does not appear for any value of X that results in amplifier B being active at the time that its two inputs are equal.

Measurements, both in the system and with individual amplifiers operating as threshold detectors, indicate that a delay exists and that it does exhibit these characteristics. Aside from turn-on time, the time delay arises primarily from the time required to charge the capacitance at the base of Q_5 (Fig. 2-18) and the values observed are consistent with circuit parameters.

While no compensating circuits to eliminate these sources of error have been tested in the system, the design of such compensation is not particularly difficult. The effects of amplifier B turn-on delay could be eliminated by gating this amplifier ON several microseconds prior to the start of the cycle. The other component of the delay time could be compensated for by delaying turn ON of amplifier C an equal amount with a one-shot multivibrator. Ideally, the length of this compensating delay should be varied with Z and this could be done by making one-shot timing-capacitor charging current a function of Z. Even if this feature were not included significant error reduction should be possible. Some further investigation shows that the net increase in circuitry required to implement this type of compensation would be two one-shot multivibrators, one OR gate, one gate driver, and the addition of an AND input to the gate shown in Fig. 4-9.

A 0.9-μs fixed delay in the turn ON of amplifier C would result in a correction term equal to 0.009 Y added to all outputs. Similarly, turning ON amplifier B several microseconds early would result in adding another correction term of 0.006 Y for X = 0.

The experimental data presented in Table 4-1 was corrected by the amount given above, and this modified data is presented as the top figure in each box of Table 4-2. The correction terms which would be realized by including the additional logic circuits are the only changes between this part of Table 4-2 and Table 4-1. The second item in each box of Table 4-2 is the ideal ratio, assuming a scale factor such that the output equals $\frac{XY}{4.21Z}$. The third item shows the magnitude of the error expressed in millivolts.

Note that with this very simple compensation it should be possible to reduce maximum error to 12 mV. The average error magnitude is 2.1 mV, while the rms error is 3.1 mV. While these error figures have not been verified experimentally, there is no reason why the suggested modifications should not yield errors of this order.

The implications of this type of accuracy, of course, extend far beyond the use of the gated amplifier in a multiplier-divider system Since the same general method is used in other applications such as A-D conversion and function generation, the low error of the multiplier-divider indicates that related operations should be possible with low error.

The dynamic performance of the multiplier-divider system was tested as follows. The Y input was an 8-volt peak-to-peak sinusoid with variable frequency. The X and Z inputs were adjusted to nominal values of -4 volts and 1 volt respectively, and the magnitude of Z altered slightly to yield an 8-volt peak-to-peak output at low frequency.

The Y input and the system output are shown in Fig. 4-11 for a number of different frequencies. (The Y input has been inverted in these photographs to off set the inversion arising from a negative value of X.) The general behavior predicted in Section K is evident in these photographs. There is little change in relative amplitude until frequencies in excess of 250 c/s are reached. (This is one half of the ultimate limit predicted by the sampling theorem.) For all lower frequencies, the system behaves essentially as a pure delay equal to

Table 4-2

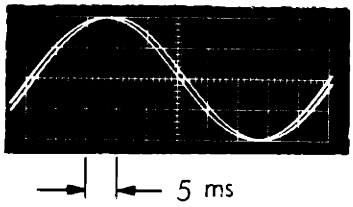
Multiplier-Divider Output Corrected for Time Delay, Ideal Output, and Error

Z (volts) ↓ / X (volts) →	0	-1	-2	-3	-4	
1	-.008	-.954	1.901	-2.854	-3.812	← Actual corrected output (volts)
	0	-.950	-1.900	-2.850	-3.800	← Ideal output, XY/4.21Z (volts)
	8	4	1	4	12	← Error (mV.)
2	+.002	-.477	-.952	-1.427	-1.903	Y (volts)
	0	-.475	-.950	-1.425	-1.900	
	2	2	2	2	3	Y=4
3	+.006	-.318	-.634	-.952	-1.268	
	0	-.317	-.633	-.950	-1.267	
	6	1	1	2	1	
4	+.009	-.241	-.475	-.713	-.952	
	0	-.238	-.475	-.713	-.950	
	9	3	0	0	2	
1	-.002	-.475	-.949	-1.425	-1.900	
	0	-.475	-.950	-1.425	-1.900	
	2	0	1	0	0	
2	+.001	-.237	-.474	-.712	-.949	
	0	-.238	-.475	-.713	.950	
	1	1	1	1	1	Y = 2
3	+.004	-.158	-.315	-.473	-.633	
	0	-.158	-.317	-.475	-.633	
	4	0	2	1	0	
4	+.007	-.118	-.231	-.353	-.473	
	0	-.119	-.238	-.356	-.475	
	7	1	7	3	2	
*	ALL VALUES LESS THAN 1 MV					Y = 0
1	+.005	.475	.949	1.427	1.904	
	0	.475	.950	1.425	1.900	
	5	0	1	2	4	
2	0	.236	.473	.712	.946	
	0	.238	.475	.713	.950	
	0	2	2	1	1	Y = -2
3	-.003	.157	.314	.472	.630	
	0	.158	.317	.475	.633	
	3	1	3	3	3	
4	-.004	.118	.235	.353	.470	
	0	.119	.238	.356	.475	
	4	1	3	3	5	
1	+.011	.950	1.896	2.850	3.807	
	0	.950	1.900	2.850	3.800	
	11	0	4	0	7	
2	+.002	.476	.949	1.423	1.899	
	0	.475	.950	1.425	1.900	
	2	1	1	2	1	Y = -4
3	-.002	.319	.634	.949	1.266	
	0	.317	.633	.950	1.267	
	2	2	1	1	1	
4	-.005	.239	.475	.712	.949	
	0	.238	.475	.713	.950	
	5	1	0	1	1	

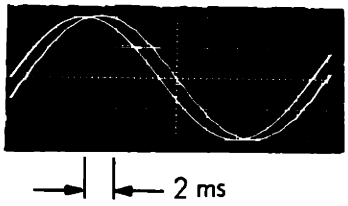
$\overline{|\text{error}|} = 2.01$ mV

$\sqrt{\overline{\text{error}^2}} = 3.07$ mV

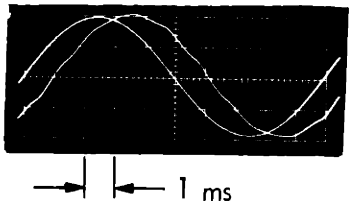
} assuming a value of 1/2 mV for all outputs corresponding to Y = 0



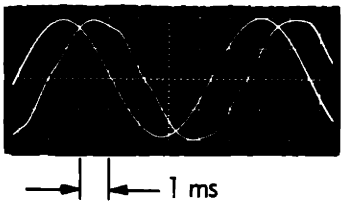
a) 20 c/s



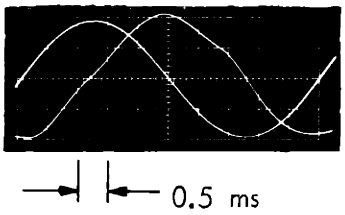
b) 50 c/s



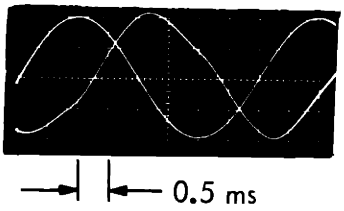
c) 100 c/s



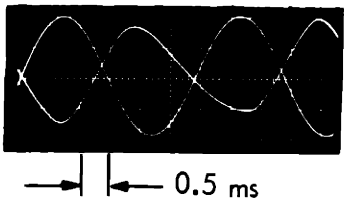
d) 150 c/s



e) 200 c/s



f) 250 c/s



g) 350 c/s

Fig. 4-11 Multiplier-Divider Input and Ouput for X = 4 volts, Z = 1 volt, Y (shown as input) = 4 Sin 2π ft. Vertical Scale is 2 volts per Division in All Cases. Output lags Input in All Cases.

1.1 ms, with the addition of some distortion or noise because of sampling. The magnitude of this noise becomes larger as the frequency is increased. This same general type of behavior is observed if either the X input or the Z input is varied sinusoidally about an operating point.

The frequency to which this multiplier-divider system can be used depends on the required accuracy. Simply from the waveforms shown in Fig. 4-11, however, it seems that operation up to 100 c/s is possible in all but the most critical applications. In many typical space applications the distortion introduced at 200 c/s or 250 c/s is tolerable. In the design of a specific system, of course, sampling rate and the time duration of one cycle would be adjusted to the minimum values which yield acceptable performance at the maximum expected input frequency, and power consumption thus minimized.

The power consumption of the system shown in Fig. 4-9 is strongly dependent on input voltages, since these determine the ON time of amplifiers A, B, and C, as well as the output currents of all amplifiers. The system was designed to operate precisely this way so that amplifiers remain ON no longer than necessary for any combination of inputs.

It is possible to predict power consumption for any inputs, and this has been done for two cases which represent the extremes. The first case considered is that of X = 0, Y = 0, Z = 1 volt. The power requirement for this combination is calculated as follows:

1. Amplifiers A and B are ON only 2 μs per cycle (the delay time of the threshold detector) and therefore are operating at a duty factor of 0.002. The average power consumption of these amplifiers is 80 μW, of which 50 μW represents OFF-state power consumption.

2. Amplifiers C and D are ON for 7 μs and 5 μs respectively, and require 155 μW and 125 μW of power.

3. The logic circuits, including the switch and gate drivers, require approximately 400 μW under these conditions.

The total predicted power consumption from these sources is 840 μW. The measured power consumption for this combination of inputs is approximately 1 mW. The difference, as in the case of the D-A converter, probably arises from some additional power which is dissipated by charging and discharging the capacitor connected to the output of amplifier D because of nonideal turn-on transients.

The worst case power consumption was simulated with X = -4 volts, Z = +1 volt and Y an 8 volt peak-to-peak 100-c/s sinusoid. The predicted power consumption is calculated below:

1. Amplifier A is ON 10 percent of the time. This duty factor plus the current required to charge the feedback capacitor, requires an average power of 1.6 mW.

2. Amplifier B is also ON 10 percent of the time, but most of the ON period is spent in a saturated condition where power consumption is only 5 mW. This amplifier therefore requires 0.55 mW of average power.

3. Amplifier C is ON 10.5 percent of the time and requires an average power of 1.75 mW. This figure includes the power required to charge the capacitor connected to Amplifier C.

4. The power consumption of the logic circuits is approximately 0.6 mW under these conditions.

5. Most of the power requirements of amplifier D arise from the power used to charge the two capacitors connected to its output. The total capacitance is 0.11 μF (a 0.1-μF hold capacitor plus a 0.01-μF filter capacitor) and the total voltage change for a 100 c/s, 8 volt peak-to-peak output is 1600 volts per second. The average current from the 7-volt supplies is 0.175 mA, and therefore the power required for capacitor charging is 1.2 mW. Amplifier ON- and OFF-state power requirements add another 0.125 mW to this figure.

The sum of the power requirements listed above is approximately 5.7 mW, and this predicted value agrees with the measured value within experimental errors. It is therefore concluded that the average power

requirements for the multiplier-divider system are between 1 mW and 6 mW depending on operating conditions.

M. COMPARISONS BETWEEN GATED-AMPLIFIER AND QUARTER-SQUARE MULTIPLIERS

The most commonly used solid-state analog multiplier is the quarter-square multiplier. The operation of this type of multiplier depends on the relationship $(X+Y)^2 - (X-Y)^2 = 4XY$. Diode function generators are used to perform the squaring functions. The minimum realization of this type of multiplier requires three operational amplifiers and two squarers which can be passive. Some manufacturers use 5 or more amplifiers to reduce errors from loading at various points in the circuit.

Multipliers of this type are four-quadrant multipliers; both inputs may be of either polarity. Dividers as such are generally not manufactured since they can be constructed with an operational amplifier and a multiplier as a feedback element.

The best specified accuracy for a commercially-available 10-volt quarter-square multiplier is a 10-mV maximum error. A small-signal bandwidth of 1 Mc, (the -3 dB frequency measured with a small sinusoid as one input and a fixed bias level as the second input) is offered by one manufacturer. Small-signal bandwidths from 20 Kc to 100 Kc are more common. Typical power requirements for commercially-available multipliers exceed one watt.

A multiplier-divider using quarter-square techniques requires at least 7 amplifiers and 4 diode squaring units, and is therefore more complex than the gated-amplifier system. However, the conventional multiplier-divider can accept either polarity for both terms of the product.

The maximum error for a multiplier-divider realized by conventional techniques is twice that of the multiplier alone, and can be considerably larger. Because of the difference in output voltage range, the resolution (maximum output voltage divided by maximum error) should be comparable for conventional and gated-amplifier units. This assumes that the delay correction procedure introduced earlier does improve the gated-amplifier system accuracy as predicted.

Once again the most significant tradeoff is between power and operating frequency. It is doubtful whether input frequencies above 5 Kc could be processed with a gated-amplifier multiplier-divider for any possible increase in sampling frequency and decrease in amplifier ON time. However, the power consumption of the gated-amplifier system is approximately 3 orders of magnitude lower than conventional multiplier-dividers.

N. A METHOD FOR FOUR-QUADRANT MULTIPLICATION

This section discusses a method that can be used to modify a gated-amplifier multiplier-divider for four-quadrant operation. The same general technique is applicable to other gated-amplifier applications such as function generation for arguments of both polarities.

The limitation of negative polarity only for the X input in Fig. 4-9 can be circumvented by adding some additional circuitry as follows. The polarity of X immediately prior to the start of a cycle can be determined with a second threshold detector. If X is negative the system remains unchanged, while if X is positive it is inverted before it is applied to the input of amplifier B, and simultaneously the input to amplifier C (the Y input) is inverted.

There are several methods for accomplishing the inversions. For example, two gated amplifiers can be used with parallel outputs and inputs. One amplifier is connected as a unity-gain inverter and the other is connected for a non-inverting gain of unity. The gain of this combination is either plus or minus one depending on which amplifier is gated ON.

A less complex realization for a switchable inverter is shown in Fig. 4-12. Assume that the gated amplifier is ON, and that the shunt switch is closed. In this case, the gain $\frac{E_{out}}{E_{in}}$ is (assuming perfect amplifier characteristics)

$$\left(\frac{K R_1}{K R_1 + K R_2}\right)\left(\frac{R_1 + R_2}{R_1}\right) = +1$$

for any ratio of R_1:R_2. With the switch open, it is possible to show that

$$\frac{E_{out}}{E_{in}} = \left(\frac{R_1}{R_1 + R_2}\right)\left(\frac{R_2 + 2R_1}{2R_1}\right) - \frac{R_2}{2R_1}$$

If R_1 is made equal to $\frac{\sqrt{5}-1}{4} R_2 \approx 0.309\, R_2$, the gain with the switch open is -1.

Implementing the ability to handle both polarities for the X input would thus require three additional amplifiers, one as a threshold detector and two as switchable inverters. (It seems that it should be possible to combine the threshold function with the existing threshold detector and save one amplifier, but I have not developed the details of this approach.) This should increase power consumption for the multiplier-divider by approximately a factor of two, since the amplifiers which are added would be gated with the rest of the system.

O. THE CONTINUOUSLY ON GATED AMPLIFIER

All the applications presented this far have involved the use of the gated amplifier in a sampling mode, such that the amplifier remains OFF most of the time. This type of gated-amplifier operation should be used whenever possible in order to minimize system power consumption. The disadvantage of sampling-mode operation is primarily that the bandwidth capabilities are severely reduced from those of the gated amplifier in the ON state.

While a majority of space-system data signals can be processed with sampling techniques, certainly not all signals are in this category. In the occasional situations where input-signal frequency precludes the use of sampling-mode operation, it is possible to use an ON-state gated amplifier in any way that an operational amplifier with equivalent performance can be used. Since the ON-state power consumption of the gated amplifier is at least an order of magnitude lower than that of other operational-amplifier designs, a significant degree of power economy is retained.

In certain applications a third possibility exists which may permit the use of a gated amplifier to process high-frequency signals with

lower average power consumption. For example, scintillating crystals and photomultiplier tubes are occasionally used in space experiments to detect energetic particles, gamma rays, or cosmic rays. In such cases the photomultiplier pulse is often less than 1-μs wide, and thus cannot be processed with sampling-mode operation. However, maximum pulse repetition rates are often less than 10 Kc. Suppose that it is possible to detect (but not process) the occurrence of a signal at the photomultiplier tube. If a delay greater than the gated-amplifier turn-on time is introduced into the signal path with a delay line, the amplifier can be gated ON when the pulse is detected, and will be active and ready to process the pulse after it has been delayed. The amplifier is then gated OFF and remains inactive until the next pulse arives.

P. NON-SPACE APPLICATIONS

The major research effort with the gated amplifier has been specifically tailored toward designing circuits and systems for data processing in space applications. This design approach is manifested in the types of compromises which were included in the development of the amplifier, particularly with respect to minimizing power consumption.

Gated-amplifier designs are possible which should be useful in earth-based analog computers, particularly in hybrid analog computation where operational-amplifier control is accomplished with digital signals. In order to tailor a gated-amplifier design to these requirements, increases in power consumption would be tolerated in exchange for greater output voltage range, faster turn ON, and possibly greater bandwidth in the ON state.

The applications of the gated amplifier to hybrid analog computation center on its use as an electronic switch. One obvious application involves use of a gated amplifier as a high-quality sample-and-hold circuit. Another frequent requirement is the rapid reset of integrators to specific initial conditions. A hybrid computer is often operated repetitively, in which case the computer is cycled between two modes of operation, compute and reset. The equation under investigation is solved during the compute portion of the cycle, while initial conditions are applied to integrators during the reset cycle. It is desirable to

have reset occur in minimum time so that the computer spends most of the time actually computing.

A frequently used method for switching between these two modes is shown in Fig. 4-13. With switch 1 closed and switch 2 open, the transfer function of the operational amplifier is $E_{out}(t) = -\frac{1}{R_1 C}\int E_1(t)\,dt$. Reset is accomplished with switch 2 closed and switch 1 open, in which case equilibrium is reached with $E_{out} = -E_2$. The switches shown in the figure do not have power gain, but it is important for them to have a low series resistance when closed, and to have very high resistance when open. The booster amplifier is included to permit rapid reset by supplying high current to the capacitor. Voltage gain greater than unity is not required from this amplifier.

At least in cases where compute and reset are the only two required modes, the functions of both the switches and the booster amplifier can be realized with a single gated amplifier. The gated amplifier is connected for a non-inverting gain of unity and replaces the booster amplifier and switch 2. Switch 1 is eliminated entirely (replaced by a direct connection). With the gated amplifier OFF, the operational amplifier functions as an integrator. With the gated amplifier ON, the output is forced to $-E_2$ regardless of the input E_1, since the very low output impedance of the unity-gain gated amplifier prevents E_1 from influencing the output. The low charge dump of the gated amplifier (which could be made even smaller in this application where little output voltage range is required) should minimize another common problem of existing switch designs.

This technique has been tested using one gated amplifier as a reset switch and a second as the operational amplifier. Reset times with this combination are essentially the same as the times required for sampling described earlier. For example, if a 0.1-μF capacitor is used around the integrator, a full 8-volt reset can be accomplished in approximately 7 μs. This is at least an order of magnitude lower than the reset time normally specified for conventional reset methods under similar conditions.

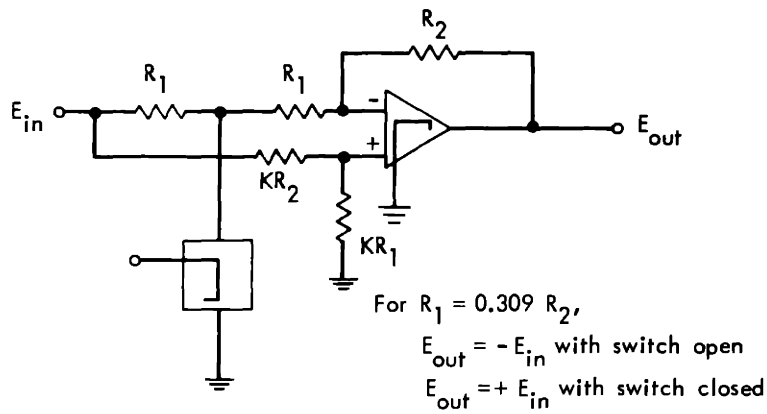


Fig. 4-12 Circuit which Provides Gain of ±1

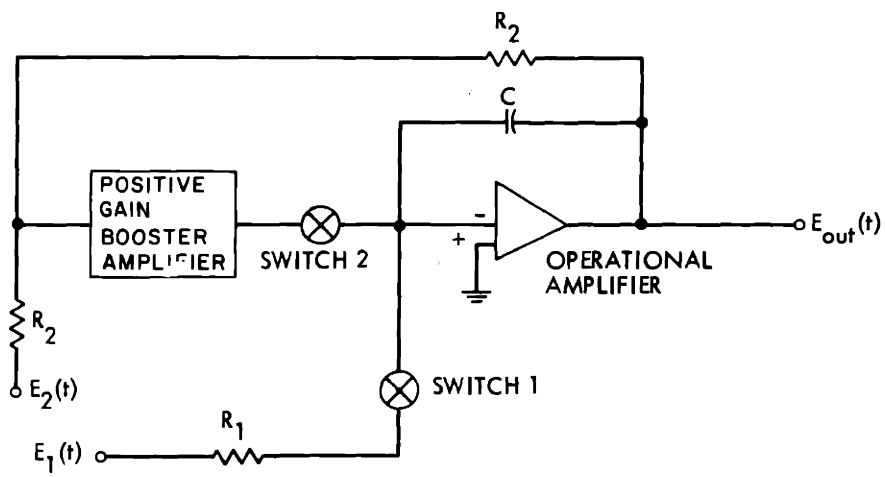


Fig. 4-13 Method for Switching an Integrator between Integrate and Hold Modes

Another possible gated-amplifier application is in the area of automatic programming of analog computers in response to digital commands. Even in the case of hybrid computers, most analog programming is accomplished by physically interconnecting computing elements with wires on some type of a patching system. To date a minimum amount of actual programming is done by electronic control, primarily because of the economic problems associated with providing sufficient switching capacity.

There are, however, several reasons why an electronically-controlled programming system is desirable:

1. The manual labor and possibility of error associated with hand programming is eliminated.

2. The time required for many studies can be greatly reduced. Patching a one-hundred amplifier problem (which is not particularly large for modern analog computers) requires several hours at the very least. Usually another day is spent discovering the errors made in programming. After this phase is completed, complete solutions can often be obtained at rates in excess of 100 per second. Thus, for many problems, actual solution times consume an insignificant fraction of the total time spent on the machine.

3. There is the interesting possibility that, at least for a large class of problems, the actual interconnection diagram can be developed directly from a problem statement in differential equation form with the aid of a digital computer. The problem can then be implemented automatically on an analog machine if sufficient switching capability is available.

4. Because of the high reliability typical of semiconductor components, the patching system is probably the least reliable element of an analog computer system. Much time is often wasted searching for poor contacts, broken patchcords, or other failures. Automatic programming can eliminate this reliability problem.

5. Present operational-amplifier speed capabilities are severely restricted by the patchboard system. While it is possible to design operational amplifiers which have cross-over frequencies (or -3db closed-loop bandwidths) in excess of 100 Mc, there is no patchboard system known which maintains adequate signal fidelity for signals in excess of 1 Mc. Even if ringing, etc., could be eliminated through use of a terminated cable interconnection system (which isn't practical because of impedance levels), time delays could cause instabilities for high-speed solutions.

   The only way to circumvent this problem seems to be the design of very small (probably in integrated circuit form) operational amplifiers and associated electronic programming switches so that an entire computer occupies a small enough volume to permit its use at high frequencies.

While it is realized that a good, economical switch is not all that it is required to overcome the problems listed above, the development of such a switch would solve one of the major problems.

The realization of a switch with a gated amplifier is an almost trivial application. In fact, if this is the only required function, the circuit becomes much simpler, with a final configuration quite similar to that shown in Fig. 1-2. This simple circuit has self-evident economic advantages compared with the high-performance gated amplifier shown in Fig. 2-18. Design simplifications in the case of a gated amplifier intended only for use as a switch are possible for several reasons:

1. ON-state input current is unimportant, since this current can usually be supplied from a low-impedance point.
2. High open-loop gain is unnecessary since the amplifier is used only with a closed-loop gain of unity.
3. The maximum output current can generally be reduced since sampling is not required.
4. The temperature extremes experienced in a general-purpose analog computer are low.

5. Since a fixed configuration is used, frequency-stability problems are minimized.

6. Increases in power consumption are tolerable.

A modification of the basic gated-amplifier design exists, and this modification should be useful for automatic programming systems because of the way such a system would probably be organized. Ideally, it should be possible to connect the output of every computing element to the input of every other element with an automatic programming system. In practice this is not required, and the ability to supply the input of an element from one of possibly five outputs of other elements allows sufficient programming freedom.

It is possible to develop a gated-amplifier circuit that can be used as an "N-to-one" switch; that is, one of N signals can be electronically selected and switched to a common output terminal with unity gain. The complexity of such a circuit is much less than that of N single gated amplifiers. In order to demonstrate the feasibility of such a design, I have built a 2-input gated-amplifier switch and there seems to be no fundamental problem in extending the basic configuration to handle 5 to 10 input signals. The basic technique used to design this type of switch is described in Appendix II.

Because of the relatively relaxed specifications for a multiple-input gated-amplifier design intended only for use as a switch, it should be possible to construct the circuit in integrated-circuit form with present-day technology. The number of switches required for an automatic programming system should be on the order of the number of operational amplifiers used in the computer if a five-input switch is designed. The possibility that a relatively small number of inexpensive switches can form an automatic programming system may make such a system economically feasible.

Another possible use for the gated amplifier in conventional data-processing operations is in electronically-tunable filters. Virtually any required linear transfer function can be generated with standard analog simulation techniques using only summing amplifiers and integrators. Assume that a system is designed with a transfer function A(s).

It can be shown that increasing the gain of every integrator (K if the integrator transfer function is K/s) by a multiplicative factor of C modifies the system so that the new transfer function is A(Cs).

It can be seen from the discussion of the sampling-mode integrator (Section D) that the gain of such an integrator is directly proportional to the sampling frequency. Therefore, control of the sampling frequency provides a method for frequency scaling a transfer function simulated with sampling-mode integrators.

Q. CONCLUSIONS

This chapter has demonstrated ways that gated amplifiers can be interconnected to perform both linear and nonlinear data-processing operations. The repeated use of several basic connections permits the design of data-processing systems which use only gated amplifiers, passive feedback and storage elements, logic circuits, and a shunt switch.

The advantages of the gated amplifier as a system building block include:

1. A versatility unmatched by conventional operational amplifiers, which require more complex ancillary circuitry in many applications.
2. This versatility is manifested by less complex systems in some applications in spite of the greater complexity of a gated amplifier compared with an operational amplifier.
3. The use of sampling-mode operation can result in power reduction of 2 to 3 orders of magnitude compared with other data-processing methods.

The disadvantages of the gated amplifier are:

1. In certain cases (such as sampling-mode integration), the accuracy is somewhat lower than that possible with conventional analog techniques.
2. The bandwidth of a gated-amplifier system which operates in a sampling mode is quite low.

The tradeoff which reduces bandwidth and in some cases accuracy in exchange for lower average power consumption is most desirable in space-system applications for several reasons. Most typical experimental variables are slowly time varying, with major frequency components limited to less than 100 c/s. Examples of this type of data include solar-flare data, plasma-density measurements and meteorite-impact data. Similarly, the rate at which data can be prepared for telemetry is limited by telemetry channel capacity. Furthermore, the need for highly accurate data processing is not present in space systems to the extent that it is in earth-based analog computation for a fundamental reason. Design compromises necessitated in order to develop sensors which are small and light enough for use in a spacecraft generally limit the available signal-to-noise ratio from these devices. Thus typical errors in the original data-containing signals will often mask processing inaccuracies of 5 percent or more.

In contrast to the design freedom allowed in the case of bandwidth and accuracy, power minimization is of vital importance in current space experiments, and decisions as to what experiments will be attempted are often made on this factor alone. The situation may ease when reactor power systems become practical but such power systems will be limited to the largest and most complex space experiments. The smaller experimental packages will probably be powered by solar cells, and hence will have very definite power limitations, for many years.

It has been shown, at least in the case of the tested systems, that predictions of important system characteristics are easily made from gated-amplifier characteristics. Power predictions are based on calculation of amplifier average power consumption as a function of duty factor. The power required to supply various loads is obtained by realizing that all load current must be supplied from 7 volts. The only observed discrepancies in power predictions arise at very low average power levels, and are traceable to some increase in power consumption because of nonideal output waveforms. The errors are generally less than 25 percent.

Many possible error sources can usually be neglected, since most of these, such as dielectric absorption, show up only as scale-factor changes and thus can be easily compensated. Generally only one or

two non-compensatable error sources contribute most of the error and, once the relevant sources are discovered, realistic error prediction is quite simple for a particular system.

The examples included in this chapter have been selected as representative of the techniques for gated-amplifier use which I have found. More applications undoubtedly exist. The operational amplifier has been used for at least 20 years, and new applications are still being found for this element. The same type of extended experience will be required with the gated-amplifier circuit to develop the full versatility which should be possible through the unique use of time sequencing inherent to gated-amplifier systems.

CHAPTER V

ANCILLARY CIRCUITS

In addition to the gated amplifier itself, certain other designs such as logic circuits and shunt switches are required in gated-amplifier systems. The functions which these ancillary circuits perform are not new, but currently-available designs generally operate at power levels which exceed the ON-state power requirements of the gated amplifier. It is evident that the power economy of systems using gated amplifiers would be severely degraded if, for example, the one-shot multivibrator and gate driver normally associated with a gated amplifier required higher average power than the amplifier itself.

The circuits presented in this chapter are basically divided into two categories. The first of these includes clocks, one-shot multivibrators, flip-flops, gate drivers, a specific class of logic circuit, and shunt switches. These represent all of the circuits which were actually required for the system design presented in the preceding chapter. Typical designs for these circuits are presented. The second class of circuit includes an improved shunt switch and a multiple-voltage power supply. These circuits were not required to complete the tests and have not been constructed. However, it is evident that certain more complex systems would require some or all of these elements, and design approaches which could be used are outlined.

The designs presented in this section have not been investigated to the extent of the gated amplifier. In contrast to the gated amplifier itself where ultimate performance is required, the major design criterion used for the ancillary circuits was that they should be compatible with gated amplifiers. Compatibility in this sense implies only that the ancillary circuits do not significantly degrade the system performance which could be obtained with ideal ancillary circuits.

The performance of these ancillary circuits is superior in some respects to that of conventional designs, particularly when power consumption is considered. The complexity is generally somewhat greater than that of conventional circuits. The basic designs can be used in many applications not involving gated amplifiers, and this represents an important subsidiary benefit of the research.

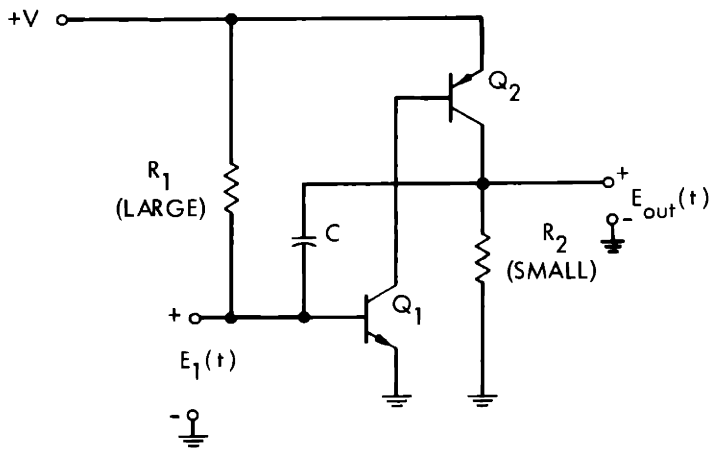
A. CLOCK

A clock circuit is used to provide a repetitive pulse train which is required in many applications. The requirements for the clock used in gated-amplifier systems are not particularly severe in most respects, but, as with all other circuits, power requirements must be minimized.

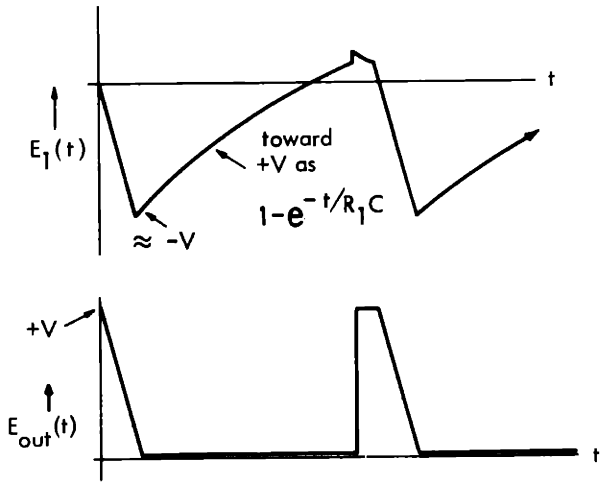
The basic clock circuit is shown in Fig. 5-1, and the operation of this circuit is explained with the aid of the included waveforms. It is assumed that at time $t = 0$ transistor Q_2 is just emerging from saturation, and at this time the output voltage is driven toward zero by the current through R_2. The output-voltage fall time is determined by the size of R_2 and any capacitance (stray or load) present at the output. The output voltage is capacitively coupled to the base of Q_1, and initial conditions are such that this base voltage falls to approximately -V. The capacitor starts to charge exponentially toward +V, with a time constant equal to R_1C. When the voltage at the base of Q_1 becomes slightly positive Q_1 turns on, and the circuit regenerates because of positive feedback around the loop containing the two transistors and the capacitor. Since both transistors are turning on, output-voltage rise time is excellent if circuit capacitances are small.

The output voltage remains high for a time determined by a number of factors, including the magnitude of the two resistors and the capacitor, the input resistance of Q_1, and storage time and current gain of Q_1 and Q_2. Eventually, providing $R_1 > \beta_1\beta_2 R_2$ so that saturation cannot be maintained, Q_2 emerges from saturation and a new cycle is started.

The circuit which is used as a clock in gated-amplifier systems is shown in Fig. 5-2. The major difference between this circuit and that of Fig. 5-1 is the addition of transistor Q_3. A necessary condition to prevent a lock-up state for the circuit of Fig. 5-1 is $R_1 > \beta_1\beta_2 R_2$. Satisfaction of this inequality leads to unrealistic component values. Transistor Q_3 insures that no lock-up state is possible, since it reduces base drive to Q_1 after the output has been positive for a prolonged period. The diode in the collector circuit of Q_3 is required to prevent an undesired charging path through the collector-to-base



a) Circuit Diagram



b) Waveforms

Fig. 5-1 Basic Clock Circuit

junction of Q_3 and the 120-K base resistor. The forward voltage of this diode necessitates a second diode in the emitter circuit of Q_1.

Oscillation frequency is lowered by placing a capacitor across terminal pair T_1. The 1-K resistor in series with this terminal pair limits the maximum current required from Q_2 during regeneration. In order to obtain oscillation frequencies above 20 Kc it is necessary to shunt the 6.8-M charging resistor with a resistor at terminal pair T_2.

The important characteristics of this circuit are:

1. The frequency can be adjusted to any value below 300 Kc by connecting a capacitor or a resistor across terminal pair T_1 or T_2.

2. The circuit provides a 0 to +7 volt output pulse with a typical transition time (10 percent to 90 percent of full output) of 5 ns, independent of operating frequency. Fall time is much slower, but this is unimportant since leading-edge triggers are used exclusively.

3. The circuit operates from -60°C to +100°C and for variations in supply voltage from 4 volts to 10 volts.

4. Frequency variation with temperature is less than 0.05 percent per degree centigrade, and is linear from -25°C to +75°C. Thus, a capacitor with an appropriate temperature coefficient can be used to reduce the variation to less than 0.01 percent per degree centigrade if required.

5. The frequency change is approximately ±2 percent for a ±10 percent change in supply voltage and is linear with supply voltage.

6. Time jitter is less than 0.01 percent rms.

7. The power required with no load and with a 7-volt supply is $P = 4 \times 10^{-5} + 2.5 \times 10^{-8} F$, where P is the power in watts and F is the frequency of operation expressed in cycles per second.

The clock circuit can be easily modified for use in specific applications. Several possible modifications are:

1. The circuit can be made to operate to frequencies in excess of 10 Mc by reducing all resistor values and by including an emitter-to-base resistor for transistor Q_2. This modification is useful for high-speed A-D conversion and other applications which require high-frequency pulses.

2. The clock can be gated if a grounded-emitter PNP transistor is included in series with the charging resistor. This transistor is used as a switch. The possible need for a gated clock was indicated in the section on A-D conversion.

3. The clock can be changed to a voltage-to-frequency converter if the charging resistor is replaced with a controlled current source. This technique is used in part of the power-supply circuit.

B. FLIP-FLOP

The basic designs for both the flip-flop and the one-shot multivibrator are versions of the four-transistor complementary switching circuit.[12] This configuration (shown in simplified form in Fig. 5-3) has several significant advantages compared with the more common two-transistor switching circuit including:

1. Switching speed is essentially independent of quiescent power consumption.

2. Rise and fall times are identical.

3. Very high peak currents for use as triggers are available when the circuit is in transition, yet average power requirements can be made extremely low.

(The simplified circuit shown in Fig. 5-3 is intended for illustration only and does not fully exploit the advantages of the configuration.)

The circuit shown in Fig. 5-3 has two stable states, either with Q_1 and Q_4 conducting (in which case Q_2 and Q_3 are nonconducting) or with Q_2 and Q_3 conducting (Q_1 and Q_4 nonconducting). The existence

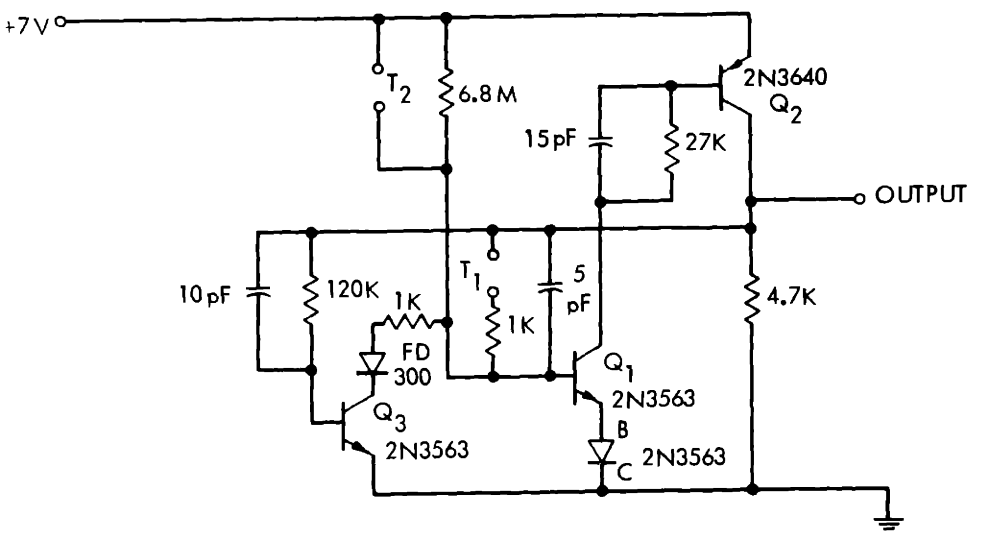


Fig. 5-2 Practical Clock Circuit

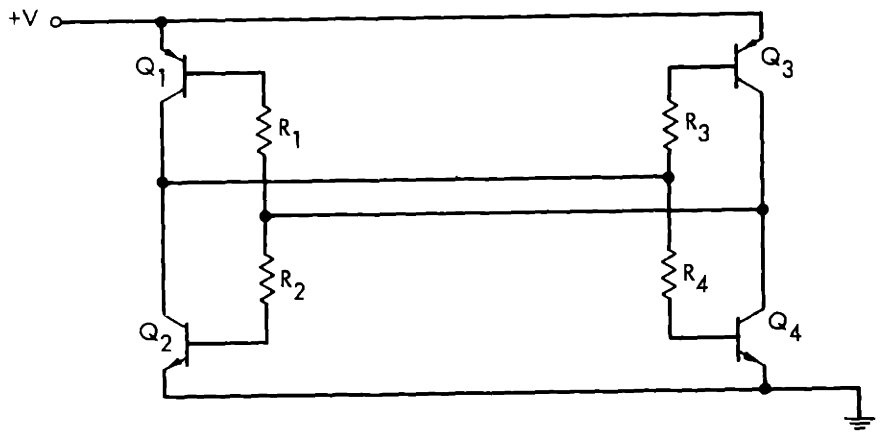


Fig. 5-3 Basic Four-Transistor Switching Circuit

of these two stable states can be shown if, for example, it is assumed that Q_2 is conducting. The collector potential of Q_2 is near ground, and therefore Q_3 is conducting because of base current supplied through R_3. With Q_3 conducting, current is supplied to the base of Q_2 through R_2, and this condition justifies the initial assumption. Q_1 and Q_4 will be off providing certain inequalities are satisfied. Q_4 is off if the saturation voltage of Q_2 plus the product of R_2 and the leakage current (I_{CBO}) of Q_4 is less than the voltage required to turn on Q_4. This inequality and the corresponding one involving Q_1 and Q_3 are satisfied for any realistic resistor values providing low-leakage transistors are used.

The circuit is most frequently constructed with all four resistors equal, but this is not necessary or even desirable in many applications, and all versions used with gated amplifiers are designed with non-equal resistor values. The exact method of triggering determines how the circuit functions (set-reset flip-flop, one-shot multivibrator, etc.).

A practical schematic for a flip-flop is shown in Fig 5-4. While this circuit is not identical to any flip-flop used for system design, it does illustrate the various triggering methods which can be used. Any required flip-flop function can be realized by removing certain trigger networks shown in Fig. 5-4 and/or including additional ones in other locations.

Speed-up capacitors are included in the flip-flop design to enhance switching speed and to provide high output current during transition. Since high-value cross-coupling resistors are used,it is necessary to include diodes which provide discharge paths for the speed-up capacitors.

This particular version is constructed with non-symmetrical base drive resistors for the following reasons. It is assumed that this flip-flop will be used to generate gating pulses rather than as part of a counter, and therefore should remain in the logical 0 state most of the time. (Positive logic is assumed throughout this discussion; the 1 output of the flip-flop is at +7 volts with the flip-flop in the 1 state.) Base-drive current is supplied by 2.7-M resistors with the flip-flop in the zero state, and the resultant quiescent power consumption (in absence of load) is 30 μW. The base-drive resistors with the flip-flop in

the logical 1 state are 1 M, resulting in a quiescent power dissipation in this state of 80 μW. The lower-value resistors permit higher load currents in the 1 state.

Set and reset are implemented with simple diode gates. Either the leading or the falling edge of a signal can be used depending on whether the particular network is connected to the base of an NPN or a PNP transistor. These networks can be either a-c or d-c coupled as shown. Certain logic functions can also be built into the flip-flop. For example, triggering on a logical OR combination is possible if two trigger networks are connected to the base of one transistor. With this amount of freedom in the choice of trigger networks, it is often possible to eliminate separate inverters and gates which might be required if other flip-flop designs were used.

The complement input uses transistor pair Q_5 and Q_6 to provide current steering, and operates as follows. Assume that the flip-flop is in the 1 state. In this case the base-to-emitter voltage of Q_3 exceeds that of Q_1. Therefore, the base of Q_6 is biased more negative than that of Q_5. Application of a positive transition to the complement input steers charge through Q_6 to the base of Q_4 and this action changes the state of the flip-flop. These two transistors are omitted if the complement function is not required. Similarly, the collectors of Q_5 and Q_6 can be connected to transistors in a following stage for a shift-register design.

In addition to the 1- and 0-state quiescent power requirements, a certain amount of energy, primarily reflecting the energy necessary to charge circuit capacitance, is required to change the state of the circuit. The energy required to change state with the component values shown in Fig. 5-4 is approximately 3×10^{-9} joule. It is possible to reduce this energy by reducing the size of the speed-up capacitors (values as low as 10 pF are acceptable) in cases where high peak output currents are not required such as in a counter.

The average power requirements for the flip-flop shown in Fig. 5-4 can be calculated for any specific operating conditions as a combination of quiescent and transient power consumption. For example, assume the flip-flop is triggered with a complementing input at a 50-Kc rate. In this case the flip-flop spends one half of the time in each state, and

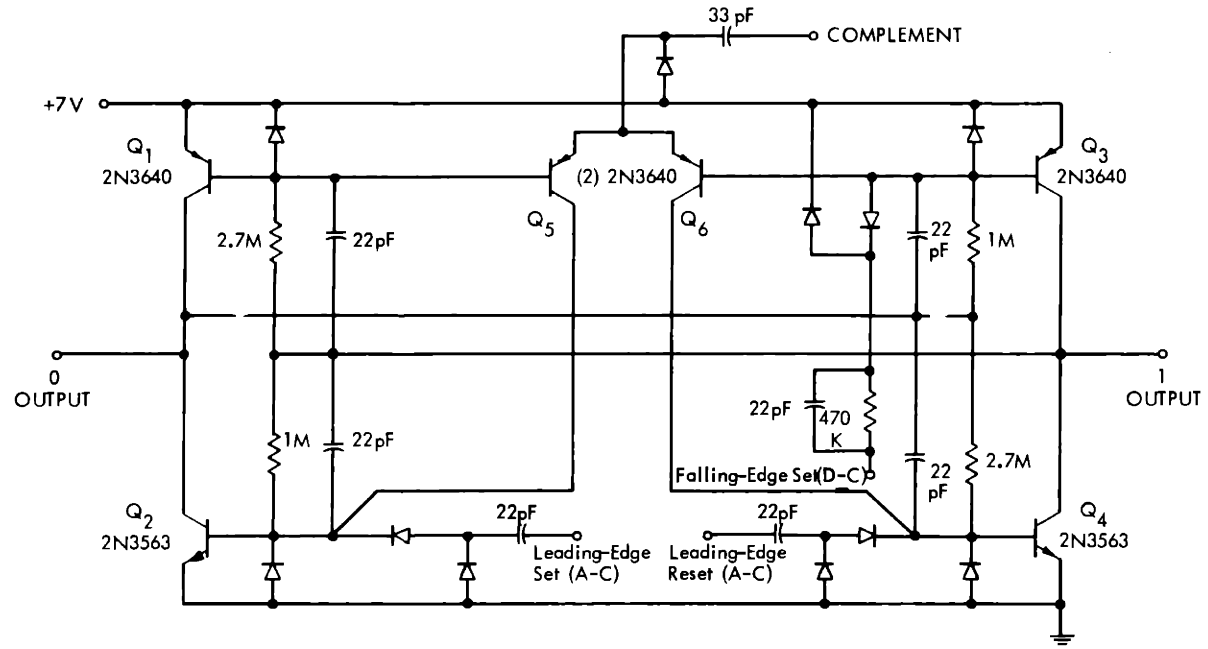


Fig. 5.4 Practical Flip-Flop Circuit

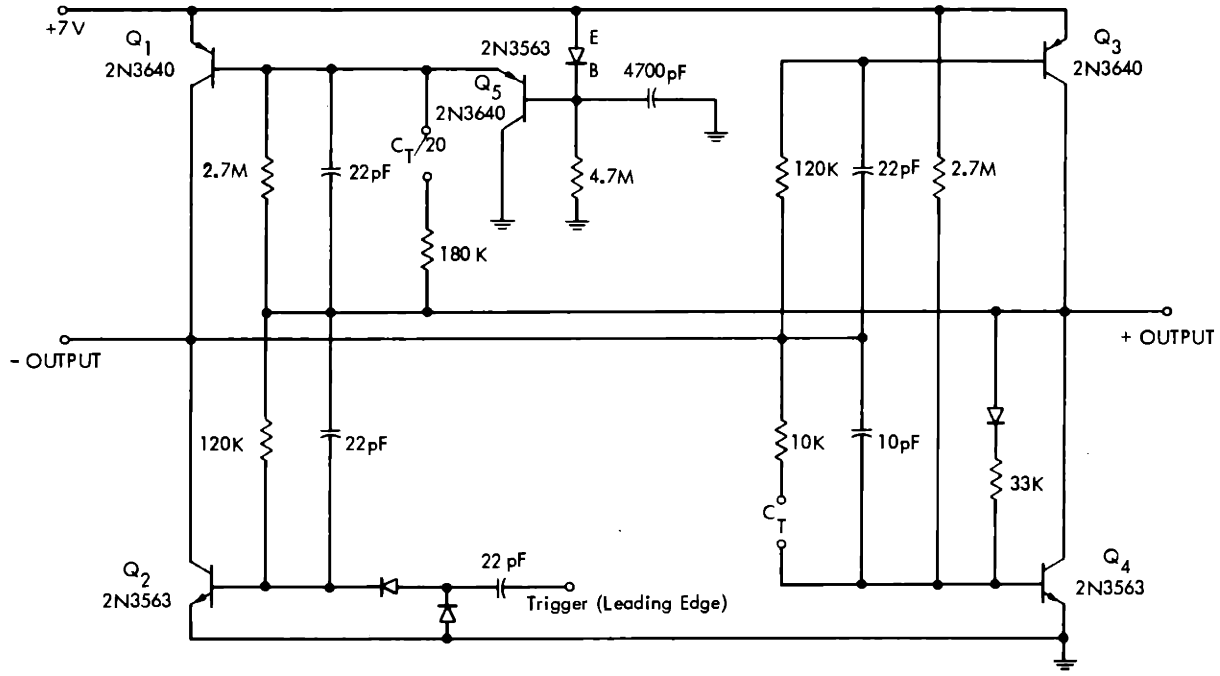


Fig. 5-5 One-Shot Multivibrator

this operation results in a quiescent power consumption of 50 μW. The switching power requirement for this trigger rate is 150 μW, and therefore average power consumption is 200 μW.

The circuit shown in Fig. 5-4 displays rise times, fall times, and propagation delays of less than 5 ns. Maximum trigger rates in excess of 10 Mc are possible.

C. ONE-SHOT MULTIVIBRATOR

Some further modification of the basic switching circuit results in the one-shot multivibrator circuit shown in Fig. 5-5.

The normal state exists with Q_1 and Q_4 maintained in conduction by 2.7-M base-drive resistors. A positive trigger applied to the base of Q_2 turns on this transistor, and regeneration drives the circuit into a temporary state with Q_2 and Q_3 conducting. (A negative trigger applied to the base of Q_3 can also be used.) The output current capability in this state exceeds 1 mA, since relatively low base-drive resistors are used. The assumption implicit in this design is that the circuit spends most of the time in the state with the positive output low and in this state power consumption is approximately 40 μW. Power consumption in the temporary state is 4 mW.

The time period spent in the temporary state is determined by the timing network in the base circuit of Q_4. If no timing capacitor (C_T) is used, the time spent in the temporary state is less than 0.5 μs. This time interval can be increased without limit by increasing the value of C_T, and electrolytic capacitors can be used if required to reduce size. The scale factor relating time in the temporary state to capacitor size is 0.025 μs per pF.

Charging current for the timing capacitor is provided by the network consisting of a 33-K resistor and a diode connected in series between the timing capacitor and the positive output. An interesting feature of this method of charging is that power is dissipated in the network only while the circuit is in the temporary state.

The fifth transistor is added to the basic switching circuit to insure rapid transition to the normal state. A peculiarity of the four-transistor switching circuit is that both of the members of a pair of transistors must conduct for the circuit to regenerate. Consider the

transition from the temporary to the normal state for the circuit shown in Fig. 5-5. At some instant Q_4 starts to conduct, and the voltage at the positive output starts toward ground from +7 volts. The circuit does not regenerate, however, until Q_1 becomes active. Therefore, the transition is slow for an interval equal to the time required to turn Q_1 on. The diode forward voltage and the base-to-emitter voltage of Q_5 are chosen so that Q_1 is biased close to conduction with the circuit in the temporary state. This insures that a potential change of less than 0.6 volt is required at the positive output to initiate regeneration.

The capacitor which is placed across the terminals labeled $C_T/20$ is included to permit rapid recharge of the timing capacitor. The timing capacitor is recharged following transition to the normal state through the 10-K resistor connected between the collector of Q_1 and the timing capacitor. Peak recharge currents exceed 0.5 mA and Q_1 must supply these currents. It is evident that the required collector current would not be available if the 2.7-M resistor provided the only base drive for Q_1. The network including the capacitor $C_T/20$ and a 180-K resistor provides temporarily increased base drive immediately following transition to the normal state.

The important characteristics of the one-shot multivibrator shown in Fig. 5-5 are:

1. Two 7-volt pulses are provided, one positive going and the other negative going. All four transition times are less than 10 ns (10 percent to 90 percent of full output) with typical values of 5 ns. The 50-percent points of the positive and negative waveforms occur within 5 ns of each other.

2. Time spent in the temporary state can be adjusted from a minimum of less than 0.5 μs to any higher value with two capacitors.

3. Maximum duty factor (ratio of time spent in temporary state to total time) exceeds 50 percent.

4. More than 1 mA of output current is available from either output with the circuit in the temporary state.

5. The circuit operates satisfactorily from -60°C to +100°C and exhibits a variation in pulse width of less than 0.1 percent per degree centigrade over this temperature range.

6. Power is computed as a linear combination of the 40 μW required in the normal state and the 4 mW required in the temporary state. The 4 mW required in the temporary state includes the power necessary to charge timing capacitors. A certain amount of energy is required to charge circuit capacitances (other than the two timing capacitors) on each cycle of operation, but contributions from this term are negligible under normal operating conditions.

D. GATE DRIVER

The gate driver performs several functions in gated-amplifier systems:

1. Voltage gain is supplied. The 0 and +7 volt logic signals used as inputs to the gate driver are amplified to +9 and 0 volts (gating levels) respectively. Operation at the 7-volt level permits the design of lower-power logic circuits than would be possible if a 9-volt level were used. The associated inversion turns an amplifier ON for a logical 1 applied to the input of the gate driver.

2. Current gain is provided. This permits a further reduction in logic-circuit power requirements and also increases the number of gated amplifiers that one logic circuit can drive.

3. Pulse shaping is provided. While the logic circuits supply rapid-transition pulses, transmission along one foot of wire slows the transition and introduces ringing. Terminated cables cannot be used to eliminate this effect because of unrealistically high power requirements. The gate driver restores deteriorated signals, and supplies gate-drive signals with transition times of less than 5 ns. The gate driver is normally located near the associated amplifier so that pulse fidelity is maintained.

The circuit used as a gate driver in all experimental gated-amplifier systems is shown in Fig. 5-6, and is essentially one half of the complementary flip-flop circuit. If the input is +7 volts, the output is near ground with Q_2 conducting and gated amplifiers driven from the output will be ON. The circuit can supply gate current to more than 10 gated amplifiers in this state. Switching the input negative pulses Q_1 momentarily, forcing the output to +9 volts. The output is maintained at +9 volts through the 220-K resistor, since no current is required by the gate leads of gated amplifiers in the OFF state. The circuit consumes less than 1 mW of power with the input at +7 volts, and less than 10 μW with the input at ground. Transitions between the two states (10 percent to 90 percent of full output) occur in less than 5 ns.

E. LOGIC GATES

The basic complementary-switching approach used for the flip-flop, one-shot multivibrator, and gate driver can also be used for logic gates. The required function can either be implemented with a separate logic circuit or, at least in some cases, can be combined with the function of a gate driver.

A two input OR gate is shown immediately preceding a gate driver in the multiplier-divider system discussed in Chapter IV. (See Fig. 4-9.) This OR gate is actually combined with the gate driver as shown in Fig. 5-7. With reference to the discussion of the multiplier-divider system, amplifier C is gated ON if the signal from the voltage-to-time converter is a 1 OR if the output of the one-shot multivibrator is a 1. Furthermore, the signal sequence is always identical. The output of the voltage-to-time converter first becomes a 1. At some later time this variable switches to 0 and simultaneously the one-shot output becomes a 1. The cycle ends when the one-shot output returns to 0.

In the circuit shown in Fig. 5-7, the A input represents the output of the voltage-to-time converter. When this input is switched to +7 volts, the circuit output is driven to ground by Q_3. Input B of Fig. 5-7 represents the signal from the one-shot. This signal must switch to +7 volts at the same time that the A input switches to ground. The output remains low (and therefore an amplifier gated from this output remains ON), since Q_2 conducts with input B at +7 volts. When input

B returns to ground Q_3 is pulsed momentarily, driving the circuit output to +9 volts.

This type of design can be used to combine logic-function generation with a gate-driver circuit in many typical applications, but the method lacks generality since a particular input sequence is assumed. A modified design procedure can be used for the generation of any logic function of the form*

$$(X_1 \cdot X_2 \cdots X_\ell) + (Y_1 \cdot Y_2 \cdots Y_m) +++ (Z_1 \cdot Z_2 \cdots Z_n)$$

The operation of a circuit designed by the modified method will be independent of the sequence in which inputs are applied. The general design method is:

1. A series-parallel combination of NPN transistors is designed which could be used, with a resistive load, to synthesize the complement of the required function.
2. The dual network is designed using PNP transistors. In forming this dual, all series connections of transistors are replaced by parallel connections and vice versa.
3. Corresponding NPN and PNP transistors are driven by r-c base-drive networks from the same input variable.
4. The PNP collection of transistors is used in place of a load resistor for the NPN transistors. This circuit will realize the complement of the desired function.
5. If required, the circuit can be followed by a two-transistor complementary inverter. This step can often be avoided, however, since both input signals and their complements are available if the inputs are supplied from flip-flops or one-shot multivibrators.

A logic gate designed by this method has the same advantages of rapid transition, high load capability, and low quiescent dissipation

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* In accordance with convention, dots are used to indicate the logical AND function, while plus signs indicate a logical OR.

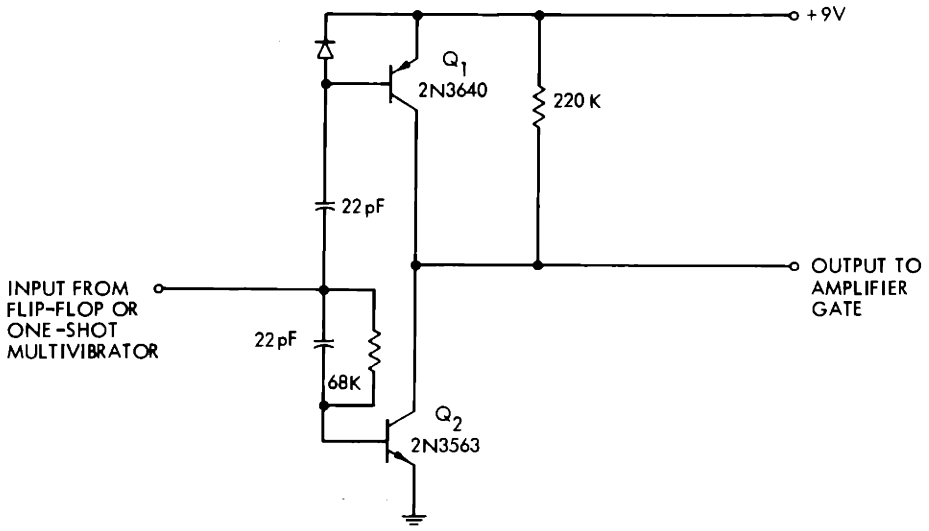

Fig. 5-6 Gate Driver

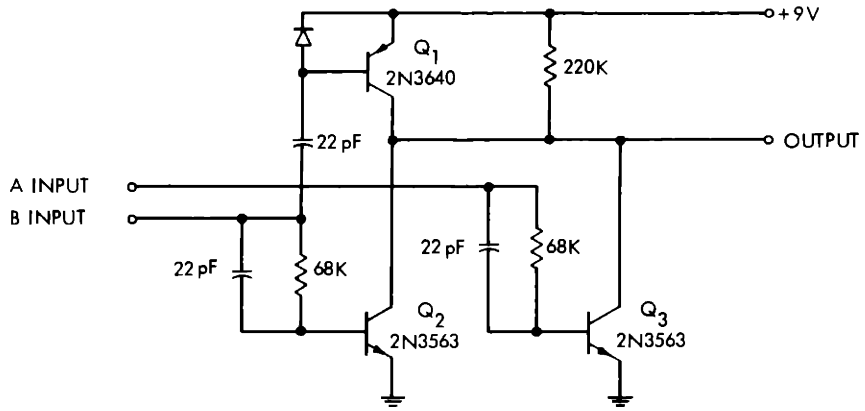

Fig. 5-7 Gate-Driver Circuit Including Logic

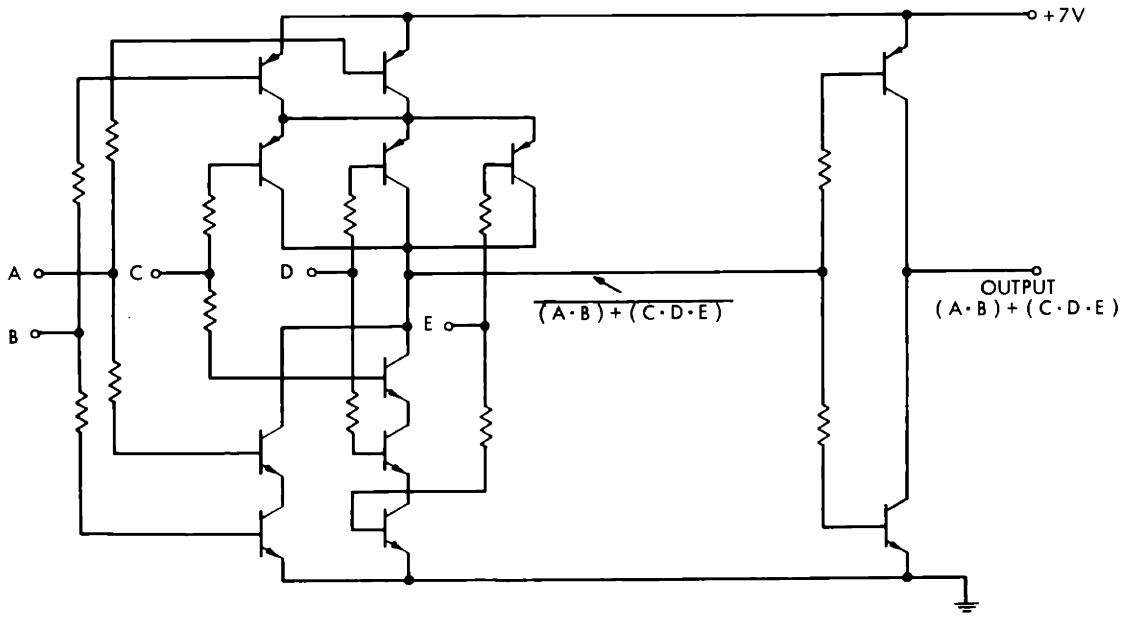

Fig. 5-8 A Circuit Illustrating the Design of Complementary Logic Gates

inherent to the regenerative complementary switching circuits.

The general method is best illustrated by an example, and for illustration it is assumed that the required function is $(A \cdot B) + (C \cdot D \cdot E)$. A circuit which generates this function is shown in Fig. 5-8. (Speed-up capacitors and diodes to discharge the speed-up capacitors have been omitted for simplicity.) Note that without an externally connected load, only base-drive power is required for any possible combination of inputs.

No logic circuits of this type were constructed specifically for use in gated-amplifier systems. I have, however, used the design method for other systems, and my experience with the method indicates that transition times under 10 ns coupled with quiescent power consumptions of less than 50 μW per input are possible.

F. IMPROVED SWITCHING CIRCUITS

As mentioned in the introduction of this chapter, the designs used for the ancillary circuits were not investigated in detail. The demonstrated performance seemed adequate for all intended applications at the time the designs were completed. As a result of some of the systems research, however, it became evident that the power consumption of the various switching circuits can dominate system average power requirements in certain applications such as sampling-mode integration, at least in cases where low sampling rates are used.

Redesign for further power reduction is possible for all of the circuits described in Sections A through E of this chapter. One approach is simply to operate the circuits from a lower supply voltage. The circuits described earlier in this chapter were tested without modification using a 5-volt supply. This resulted in a 50-percent reduction in power consumption with no detectable performance degradation. The lower voltage was not used for system design since an additional supply would be required, and the interconnection technique used made this approach difficult.

The satisfactory operation of these circuits over wide temperature ranges indicates that resistor and capacitor values can probably be altered in order to reduce further power consumption. Combination of lower-voltage operation and minor redesign should permit reduction

of switching-and logic-circuit power consumption to less than 25 percent of the levels quoted in this chapter with no performance degradation. Such redesign will be advantageous if more sophisticated gated-amplifier systems are assembled.

G. SHUNT SWITCH

Simple grounded-emitter transistor connections were used as shunt switches for the system design described in Chapter IV. Two transistor types, the General Electric 2N3415 and the Texas Instruments 2N3704 were used as switches, and either of these types results in an off-set voltage (the voltage appearing across the switch terminals with the switch shorted out but conducting no current) on the order of 5 mV and open-state leakage current under 10^{-10}A.

Two configurations were used depending on application. In the case where the switch is used to charge or discharge a capacitor, a single grounded-emitter transistor is sufficient. A speed-up capacitor larger than the capacitor to be discharged divided by β is used in parallel with a large resistor to provide base drive.

In certain applications such as the switch used to short out the input to amplifier C (Fig. 4-9) of the multiplier-divider system, a slightly more complex two-state switch is required. The basic circuit used for this type of attenuator switch is shown in Fig. 5-9. Note that the resistor which functions as the amplifier input resistor is actually divided into three components, rather than two as shown in Fig. 4-9.

The base-drive resistor of $Q_1(R_2)$ is selected so that Q_1 can be held in saturation for any expected value of E_{in}. However, the saturation resistance of Q_1 precludes attenuation ratios much in excess of 100 through this part of the switch. This leads to high feedthrough in this section when the switch is shorted out. The base-drive resistor for $Q_2(R_3)$ is selected to minimize the off-set voltage of Q_2 when the switch is in its short-circuit state. This compound switch results in offsets equal to the off-set voltage of Q_2 independent of variation in E_{in}. Base drive for the two switch transistors is provided by Q_3, and

connecting the control lead to ground causes the switch to short out. This simple drive can be replaced with a complementary drive incorporating speed-up capacitors to improve switching speed if required.

It is possible to design switches which exhibit better performance (primarily significantly lower off-set voltages) for either capacitive-discharge applications or for use as attenuators. This was not done during the experimental program since the switches described above are sufficient to demonstrate the various gated-amplifier applications and since the components required to design better switches were not readily available. However, it is evident that better switches may be required in more sophisticated applications. For example, the only effect which prevents absolute 10-bit accuracy with the D-A converter described in Chapter IV is off-set voltage in a switch.

The major requirement for a device used in either a discharge or an attenuator switch is low off-set voltage. At least two types of devices are available which exhibit lower off-set voltages than a bipolar transistor operated in the forward direction. One of these is a bipolar transistor used in an inverted connection with collector and emitter connections interchanged. Many types of silicon bipolar transistors exhibit off-set voltages of less than 0.5 mV in the inverted direction. However, unless the device is specially designed for use in this mode, leakage current and low current gain usually preclude successful operation. A number of devices are designed specifically for use in the inverted connection, and these could be used as switches. A second device which is quite attractive for use as a switch is the field-effect transistor (FET). Either junction-gate or MOS devices display virtually zero off-set voltage.

The main disadvantage of either an inverted bipolar transistor or a FET is the high dynamic resistance when on, and this effect prevents the use either of these devices alone as a switch in gated-amplifier systems. It is, however, possible to combine these devices with bipolar transistors in such a way as to realize nearly ideal switches.

Figure 5-10 shows a circuit which can be used for capacitor discharge. (It is assumed that the capacitor connected to this circuit is always charged to a positive voltage.) When the control signal is switched to ground, sufficient charge is supplied to the base of Q_1 to discharge

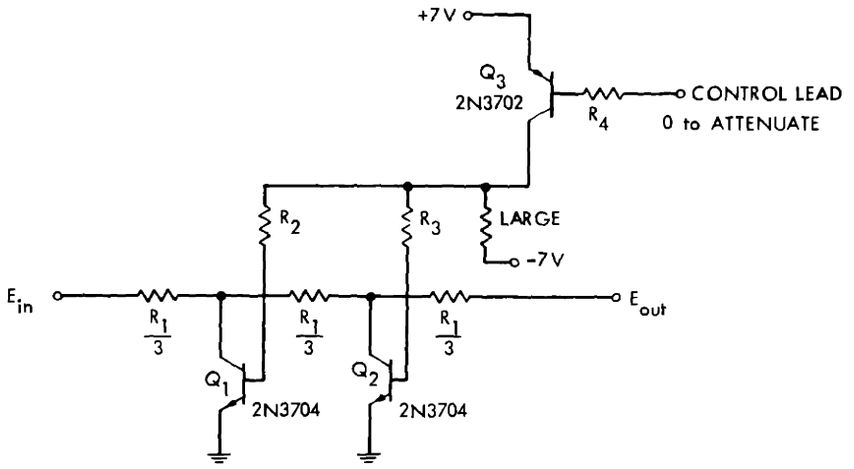

Fig. 5-9 Switch used to Attenuate a Signal Path

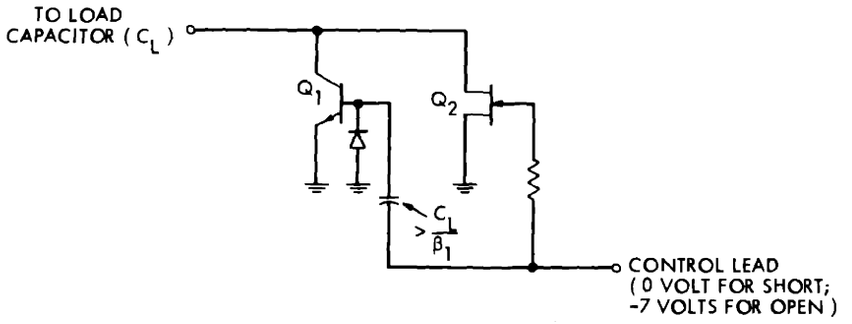

Fig. 5-10 Improved Capacitive-Discharge Switch

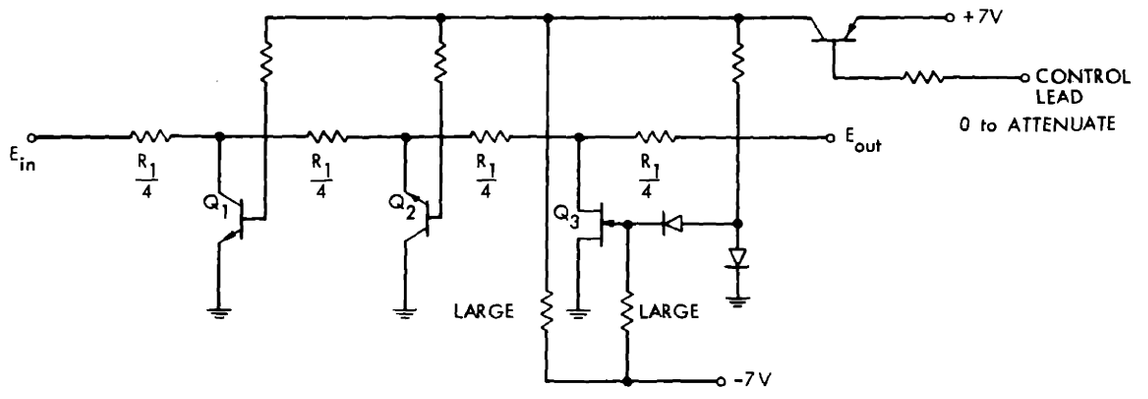

Fig. 5-11 Improved Attenuator Switch

the load capacitor to the off-set voltage of this transistor. The load capacitor is then further discharged to ground potential through the on-state drain-to-source resistance of Q_1. With the control lead at -7 volts, neither transistor conducts. Possible improvements of this circuit include a complementary drive to improve switching speed and the use of diodes to compensate for leakage currents of the two transistors.

While this circuit has not been tested specifically for use with gated amplifiers, my experience with these types of devices indicates that discharge of a 0.1-μF capacitor to less than 100 μV (exclusive of the effects of dielectric absorption) within 100 μs coupled with leakage currents in the open state of less than 5×10^{-11} A should be possible.

Similarly, it should be possible to improve the operation of a switch used as a signal attenuator by designing the 3-stage switch shown in Fig. 5-11. The first stage of the switch is a forward-connected bipolar transistor, and with this transistor conducting, it should be possible to reduce its collector voltage to less than 50 mV for any expected value of E_{in}. The second stage consists of an inverted bipolar transistor, and with this device saturated, its collector potential should be less than 1 mV. The third stage is an FET. The low off-set voltage of the FET should attenuate an input signal to less than 100 μV when the switch is in the short-circuit state. The total leakage current with the switch open should be under 10^{-10} A. The two-diode clamping network associated with Q_3 is used to provide a gate-drive signal at ground potential to turn the device on.

As in the case of the capacitive discharge switch, this type of attenuator switch has not been tested, but the techniques are well understood and no particular difficulty is anticipated with an actual design.

H. POWER SUPPLY

The power supply used for all system tests was a laboratory supply which provides 8 independent output voltages. Electronic current limiting is included, as well as an adjustment which changes all outputs by a constant percentage. This supply was extremely useful

for testing, but the general design is unacceptable for space use because its efficiency is too low.

There are several stringent requirements which apply to the design of a power supply intended for use in conjunction with gated-amplifier systems:

1. Regulation is important since amplifier drift is dependent on supply voltage. As mentioned in Chapter III, any variation in output voltage which does occur should be a uniform percentage change in all output voltages, since this type variation minimizes drift.

2. Noise and ripple should be below 1 mV rms to minimize amplifier output variations from these causes.

3. Efficiency should be as high as possible in order to realize the low power consumption typical of the gated amplifier itself on a system level. This requirement is complicated by the fact that gated-amplifier systems can display widely varying power requirements as a function of time, and therefore the power supply must maintain high efficiency over a wide range of power transfer levels.

The requirements listed above are difficult to realize simultaneously. A dissipative regulator (which generally consists of a series element that can be considered as a variable resistance) satisfies the first two requirements but is inefficient, particularly for large variations in input voltage which lead to high dissipation in the regulating element.

Higher efficiency regulators generally employ some type of resonant charging circuit where temporary magnetic energy storage is used to achieve theoretically lossless conversion from one voltage level to another. Even this type of supply is normally efficient over only a narrow range of power transfer levels.

I have already reported on a power-supply design which does maintain high efficiency over a 100:1 range of output power.[13] The essential features of this circuit are explained with the aid of Fig. 5-12. Whenever an output pulse is supplied by the voltage-to-frequency converter, the one-shot multivibrator closes the switch. This causes the

transformer primary current to increase, and magnetic energy is stored in the transformer core. The winding polarity is such that no secondary current flows during this portion of the cycle. Open-loop compensation is used to adjust the on time of the one-shot as a function of supply voltage so that a constant volt-second product, independent of supply voltage, is applied to the transformer primary. This method insures that the stored energy is independent of supply voltage.

When the switch opens, the primary current decreases to zero, the primary voltage reverses polarity and, because of mutual coupling, the dotted side of each secondary winding becomes positive. The diodes connected to the secondary windings close, and the energy stored in the core is transferred to the output capacitors. If transformer leakage inductance and the forward voltages of the diodes are negligible, the ratios among the multiple output voltages are controlled by the secondary turns ratio of the transformer. The number of primary turns and the ratio from primary to secondary are unimportant in determining output voltage, and these parameters are chosen as a function of switch and core characteristics.

Since the ratio among the output voltages is constrained by transformer parameters, regulation of all output voltages is possible with feedback from only one voltage. This voltage is compared with a reference, and the difference is applied to the voltage-to-frequency converter. The voltage-to-frequency converter used is a modified clock circuit as described earlier in the chapter, and this circuit is designed to have very sharp transfer characteristics. If the output voltage exceeds the reference by several millivolts the circuit output frequency drops to zero, while if the output drops slightly below the reference the circuit operates at maximum frequency. Equilibrium is reached with the converter operating at the frequency that exactly supplies the load requirements.

This configuration can maintain high efficiency for a wide range of power transfer levels because the circuit transfers a fixed amount of energy from input to output on each cycle of operation. Important design parameters such as number of primary turns, switch drive, and core parameters can be selected to maximize transfer efficiency for

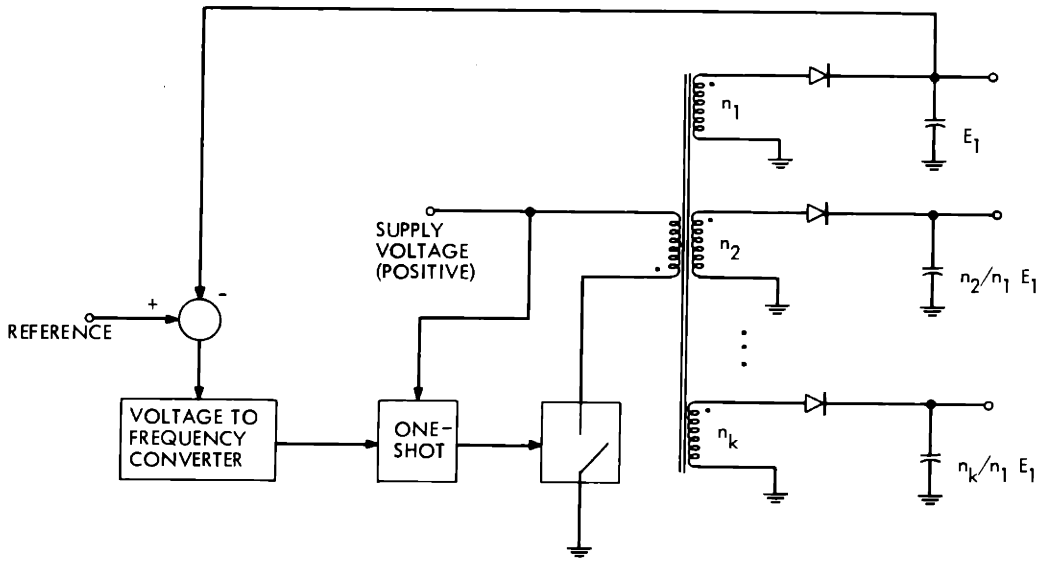

Fig. 5-12 Basic High Efficiency Converter

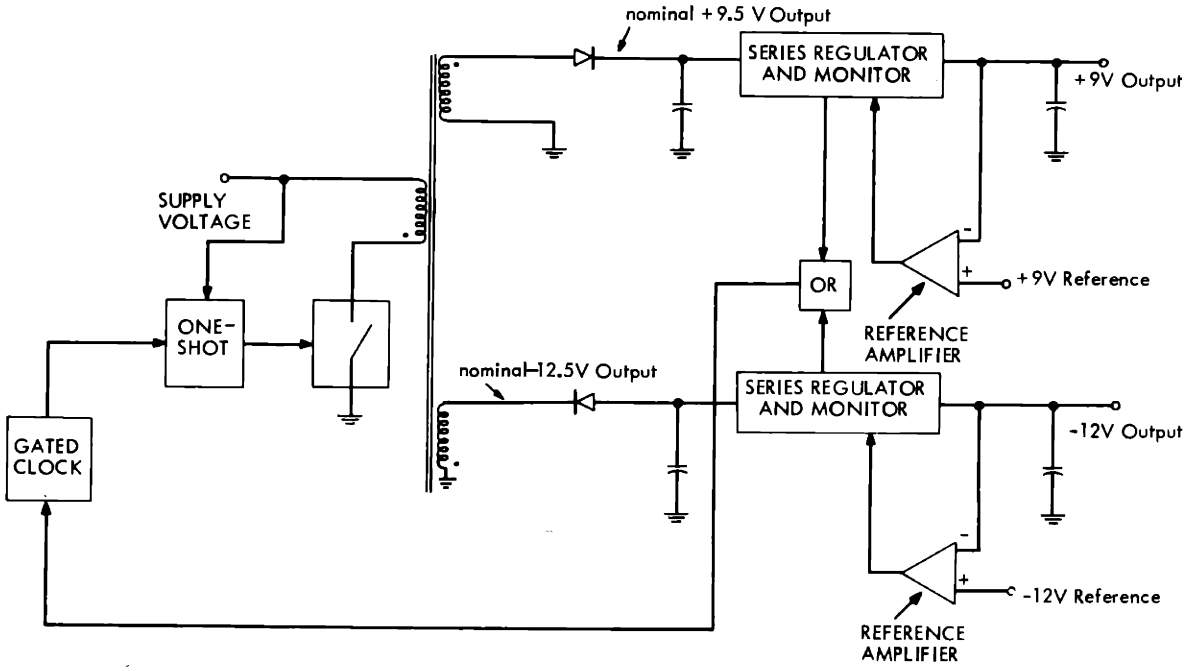

Fig. 5-13 High Efficiency Converter with Improved Regulation

the particular energy level chosen, since the transfer efficiency is independent of the rate at which the cycle is repeated.

A prototype one-watt converter using this design technique was tested and displayed the following characteristics:

1. Output voltages are ±12 volts, ±9 volts, ±6 volts and ±3 volts.
2. Output-voltage regulation is maintained for input-voltage variations from 10 volts to 30 volts.
3. Regulation against changes in load was measured by keeping the ratio of the currents required from the various output voltages constant while changing the magnitudes. This is a realistic test, since as the duty factor of gated-amplifier operation is increased, all output currents should increase proportionately. With this constraint, regulation of all outputs except the ±3 volt outputs is within ±2 percent for any load from no load to full load, and any input voltage from 10 volts to 30 volts over the temperature range of -60°C to +100°C. Under similar conditions, the ±3 volt outputs are regulated to within ±4 percent.
4. Output ripple voltage is less than 20 mV rms at any load.
5. The efficiency is 84 percent at the one-watt level, and remains above 80 percent at any level above 10 mW.

While this type of supply does have several attractive features, further modification would be required for use with gated amplifiers. In particular, regulation should be improved and ripple reduced. An improved supply has not been designed, and development of a satisfactory supply would be a fairly extensive engineering project. I have, however, conducted some preliminary investigations which indicate that the required performance could be obtained by combining a supply of the type discussed above with series regulators. Series regulators provide excellent regulation and very low ripple, and can be made efficient if the voltage across the regulating element is kept low.

A possible design is outlined in Fig. 5-13. (For clarity, only two of the five voltages required by the gated amplifier are shown in this diagram.) The transformer secondary turns ratios are selected so that each output voltage is nominally 0.5 volt higher than required.

The output voltages are then further regulated individually with series regulators driven by reference amplifiers. (All reference voltages would be derived from a single reference element to insure that all output voltages varied proportionately.) The series regulators consist of transistors with low saturation voltages. Devices are available which can regulate effectively with 0.2 to 0.3 volt across the transistor.

The voltage across each series regulator is monitored with a logic circuit which provides a 1 output if the voltage across the particular transistor is less than 0.5 volt. The logic signals are combined with an OR gate and the circuitry is arranged so that a constant-frequency clock turns on if the voltage across any series regulator becomes less than 0.5 volt. With the clock on, all preregulated output voltages, (and therefore the low one) will be increased because of energy transferred through the transformer. In practice, one transfer cycle would be sufficient to restore the low voltage and thus turn the clock off. The time until the clock operated again would be dependent on load, and the frequency of operation should stabilize at a value dependent on load and the energy transferred per cycle.

This type of circuit combines the best features of both the series regulator and the flyback-type circuit. The excellent regulation and low ripple of the series regulator are maintained, but dissipation is minimized because of the low voltage across the series elements.

The efficiency of this type of circuit would be somewhat lower than that of the regulator described earlier for two reasons. The first is the power lost in the series regulating element, and the second is the power required by the reference amplifiers, monitors, and other additional circuitry. However, these circuits could all be operated at very low current levels (or possibly gated), since low bandwidth is tolerable.

While it is emphasized that this type of circuit has not been tested and that considerable enginering effort would be required to develop a final circuit suitable for space use, I have done some preliminary calculations in an attempt to predict the behavior of such a power supply. These calculations show that a one-watt regulator could be designed with efficiency between 75 percent and 80 percent at the one-watt level. Efficiency should exceed 70 percent at a 25-mW level.

CHAPTER VI

SUMMARY AND SUGGESTIONS FOR FUTURE RESEARCH

The advantages of the gated amplifier, a new circuit which incorporates integral electronic switching into the design of an operational amplifier in order to enhance versatility and minimize power consumption, have been demonstrated.

In addition to the inclusion of the gating feature, the design of the gated amplifier differs from that of conventional operational amplifiers in that most of the voltage gain is obtained in one stage, a cascode amplifier loaded with a constant current source. This stage is preceded by a differential amplifier and followed by a unity-voltage-gain buffer amplifier. This approach minimizes ON-state power consumption, yields very high bandwidth, and permits simple compensation for any required load and feedback combination. The performance of the gated amplifier in the ON-state is comparable with state-of-the-art operational amplifiers except for a slightly reduced maximum output voltage. An outstanding feature of the gated amplifier in the ON state is that its power consumption is at least one order of magnitude lower than that of commercially-available operational amplifiers. For these reasons, it is felt that the basic design technique can be used to advantage in the design of conventional operational amplifiers.

Gated-amplifier applications have been presented in the form of a series of systems which can be used to perform typical data-processing operations. In cases where the input-signal frequency is limited, it is possible to operate the amplifiers in a sampling mode such that they remain OFF most of the time. Capacitive storage is used to maintain data while the amplifiers are OFF. When this type of operation is possible, a power reduction of from two to three orders of magnitude compared with conventional approaches is generally obtained. Because of the low power consumed by these sampling systems they are particularly attractive for space applications.

The versatility of the gated amplifier as an analog data-processing circuit has been demonstrated by the ease with which systems can be realized. Only a small amount of ancillary circuitry (primarily logic circuits) is used, and in many cases an overall system simplification

is possible in spite of the somewhat larger component count of the gated amplifier compared with other operational amplifiers.

Two systems, a digital-to-analog converter and an analog multiplier-divider, have been built and tested. The accuracy of both systems is comparable to that of conventional systems. The gated-amplifier approach yields somewhat less complex systems in both cases as well as an average power consumption that is approximately 1/1000 that of other realizations.

The results of tests on these two systems show that other systems which were designed but not actually constructed and tested should yield equally satisfactory performance, since similar techniques are used in all gated-amplifier systems.

The ancillary circuits which are required for the tested systems have been designed and built. Several other types of circuits, such as a power supply and an improved shunt switch, will be required in more complex space systems and design procedures for these circuits have been outlined. In addition to their application to gated-amplifier systems, the ancillary circuits are general-purpose designs which should prove useful in other low-power applications.

Several areas for future gated-amplifier research became evident during the program. While the basic configuration used for the gated amplifier seems ideally suited to this purpose, several specific improvements should be included in future designs:

1. The final packaging technique is important. A significant fraction of the capacitance at all of the critical amplifier nodes arises from stray capacitance. Therefore, a package designed for minimum capacitance would result in improved frequency response with no increase in ON-state power.

2. Circuit modifications should be made to take full advantage of device improvements as they become available. In particular, an integrated-circuit gated amplifier should be designed as soon as feasible, since it will result in improved bandwidth as well as greatly reduced size.

3. The gate-driver circuit, which is required in nearly all applications, should be incorporated into the gated-amplifier design and these two circuits packaged as a unit.

4. The circuit should be modified to lower OFF-state power consumption, since in some applications this represents a large fraction of the average power requirements. This can be accomplished by either gating the input-current compensating network or by increasing the resistance of the components used in this network.

The gated amplifier described in this report is intended to illustrate the basic principles of operation and is a general purpose circuit. It will generally be possible to design a unit which is better for a specific application in that the necessary engineering compromises can be tailored specifically to that application. The design techniques outlined in Chapter II can be used as guidelines for this type of redesign. An example of an application where redesign would be advantageous is that of circuits intended for use in non-space analog computation, where power would be traded for increased dynamic range, higher bandwidth, and faster switching.

Redesign of some of the ancillary circuits is also recommended if a large space system is designed. Reduction of logic levels to 5 volts would result in equivalent performance circuits which operate on one half the power of those described in Chapter V. No circuit modification would be required, and the only penalty would be the need for one additional supply voltage. In a large system this small increase in power-supply complexity is justified. Some slight modification of the circuits should result in further power reduction by at least a factor of two.

The greatest potential improvement probably involves new application methods which use the gating feature to further increase versatility and reduce power consumption. The examples presented in Chapter IV were not limited in scope because of limitations discovered in the basic concept but rather because of lack of time to develop other applications. It seems a virtual certainty that the range of applicability will be extended as further experience is gained with the gated amplifier as a building block.

An example of a technique which could yield further power reduction is that of variable-rate sampling. This technique, which has not yet been investigated in detail, seems attractive for use in any system that employs sampling-mode operation. Consider a system such as the multiplier-divider. This system is arranged so that small-amplitude signals require less average power for processing than large-amplitude signals. Variable-rate sampling may offer a method to extend this self-optimization so that lower-frequency inputs also automatically reduce power consumption. Suppose that the clock used to generate sampling pulses were modified to function as a voltage-to-frequency converter. The change in output voltage on each cycle of operation could be monitored by sensing total charge supplied to a hold capacitor during the cycle. The clock frequency could be adjusted to maintain a fixed change in output voltage per cycle, and this modification would result in constant dynamic errors. Preliminary investigations show that implementation of this technique, coupled with a minimum amount of circuit modification to lower amplifier OFF-state power and logic-circuit dissipation, should result in a system with performance characteristics equivalent to those of the multiplier-divider described in Chapter IV for high-frequency, large-amplitude inputs. However, power consumption would automatically drop to less than 200 μW for low-frequency, small-amplitude inputs. It is felt that the above example is only one illustration of many possible methods which further exploit the unique capabilities of the gated amplifier.

In summary, the gated-amplifier is ideally suited to space-system data processing since it can be used to implement many required operations with a small amount of ancillary circuitry and since the average power required to perform a specific operation with gated amplifiers is dramatically lower than that of other methods. Simple modifications of the specific circuit described in this report should result in a gated amplifier tailored to general-purpose analog computation. Further research should extend the range of applicability and result in the development of new methods which can further lower power requirements.

APPENDIX I

CIRCUIT CONSTRUCTION TECHNIQUES, PARTS SELECTION, AND INITIAL ADJUSTMENTS

The performance of high-frequency circuits such as the gated amplifier and the ancillary circuits used with it is dependent upon the packaging of the circuits, and for this reason the packaging techniques used to obtain the results presented in the report must be included. Furthermore, many of the components used in the gated-amplifier circuit are selected, and details of the selection process are necessary for duplication of the circuit.

The material presented in this appendix should permit construction of gated-amplifier circuits and systems that duplicate the performance of those described in this report. Suggestions for the repackaging that would be required for actual space experiments are included.

A. GATED-AMPLIFIER PACKAGING

This section describes the details of the construction method used to realize the gated-amplifier circuit. While the packaging selected for the gated-amplifier circuit described in this report is not intended for use in space applications, or even as a prototype for space circuits, packaging is important for several reasons:

1. The gated amplifier is a high-frequency circuit, and excessive lead inductance, node capacitance or poor grounds will deteriorate performance.

2. The multiplier-divider system described in Chapter IV includes approximately 600 components. The time required for testing such a system becomes prohibitively long if connections are not reliable.

3. Since a primary consideration with the gated amplifier is versatility, the amplifiers must lend themselves to easy interconnection either with other amplifiers or with ancillary circuitry as required by system considerations.

4. As with any experimental circuits, extensive testing of the gated-amplifier is necessary. Internal voltages must be readily available to permit this testing.

Fabrication in printed-circuit form was ideal for the experimental circuits since it combines the features listed above and since this work could be done in house to minimize the time required for circuit construction.

A gated-amplifier circuit which is typical of those used for all experimental investigations is shown in Fig. 3-1. A front view of a completely wired circuit is shown together with a back view of an unwired board in this photograph. Six amplifiers were constructed in this form for use in the experimental program.

Several construction features are evident from this photograph. The most prominent element in the assembled circuit is the aluminum block used to equalize the temperature of the input transistors and diodes. Over 80 percent of the conductor pattern on the reverse side of the board is either ground or supply voltages (incremental grounds). This entire area is effectively a ground plane which maintains a noise-free local ground and provides shielding between adjacent boards used in system design. All holes in the board are plated through to increase the reliability of connections between circuit components and the conductor pattern, and a maximum size conductor pattern is maintained to minimize the possibility of conductors lifting from the epoxy-glass base material.

All connections to the circuit are made by means of hermaphrodite banana plugs located around the perimeter of the circuit board. The four corner plugs are grounded, while the plugs located to the top left of the board are supply-voltage connections. Plug locations which are not connected to the circuit are provided at the top right of the board. These plugs are used as signal jumpers in systems. The input, output, gate and compensation terminals are located along the bottom of the board. Two possible plug locations are provided for each of these terminals, a feature which facilitates interconnection. In typical applications, the only modification made to a particular amplifier to adapt it for use in a certain operation is relocation of these plugs. All feedback and compensating networks are located external to the amplifier on special-purpose interface boards, with the result that all amplifiers are interchangeable in systems.

B. ANCILLARY-CIRCUIT PACKAGING

All ancillary circuits used for system realization were hand wired on special-purpose interface boards. This technique was chosen in preference to printed-circuit construction since it allows greater freedom in the design of the ancillary circuits.

The general circuit schematics used for the ancillary circuits have been presented in Chapter V. However, no two ancillary circuits used in the design of the systems described in Chapter IV are identical; minor variations, such as changes in the type of trigger networks used in the case of flip-flops, are introduced as required in a particular system. Hand wiring permits this type of design and also allows the construction of several types of circuits on each interface board without the need for an individual printed-circuit layout for each board.

The feedback and compensation elements for the gated amplifiers are also located on interface boards together with the ancillary circuits. The interface boards are connected to gated amplifiers with banana plugs to form systems. The interconnection method is illustrated by Fig. 3-2, which shows the multiplier-divider system. Numbered from top to bottom, boards 1, 3, 4 and 6 are gated amplifiers, while boards 2 and 5 are interface boards. The freedom from external jumpers and ease of interconnection made possible by the assembly method is evident from the photograph.

C. SEMICONDUCTOR SELECTION FOR GATED AMPLIFIERS

Every transistor and diode used in the gated amplifier is tested to some extent, and many devices are selected for certain characteristics. This is done for two reasons:

1. The plastic-encapsulated transistors used in the gated amplifier typically have a wider range of parameter variation than their metal-cased counterparts. Selection is required in order to achieve parameter spreads equivalent to those of metal-cased devices.

2. Selection is one method for improving performance without adding components to the circuit.

While the time and effort required for component selection is a disadvantage in mass-production situations, selection is practical for circuits designed for space applications. Components intended for space use are normally inspected very carefully both mechanically and electrically, often before and after certain stressing operations such as prolonged high-temperature bake and thermal shock. The data is recorded to permit elimination of potentially unreliable devices, as well as to aid in determination of causes of any possible failure, either in system test or in space. Little additional effort is required to select transistors for use in specific circuit locations.

Aside from testing time, the cost increase as a result of selection is minimal. For example, since transistor collector-to-base junctions are used as diodes in the gated-amplifier circuit, transistors which are unacceptable as active devices are not discarded. This option is particularly attractive in view of the fact that the transistor junctions offer improved performance compared to most diodes and that the transistors are generally less expensive than high-quality diodes.

As an initial screening procedure, the leakage currents and forward voltages of all transistors and diodes were measured, and extremes of the distributions were eliminated. In most cases these tests were more severe than manufacturer's acceptance tests. For example, the specified maximum collector-to-base leakage current for a 2N3563 is 5×10^{-8}A at 25°C with 15 volts applied to this junction. However, the typical value under these conditions is 10^{-11}A. Accordingly, all devices with leakage currents in excess of 10^{-10}A (10 percent of the distribution) were eliminated. The reasoning that underlies this type of screening is that leakage current and forward voltage are good indicators of potentially unreliable devices. Excessive leakage currents often indicate surface damage, while deviations in forward voltage generally indicate differences in transistor geometry.

In addition to general screening, many devices were selected for use in certain circuit applications. These selection procedures are necessary to realize the performance described in Chapter III. The specific selection procedures used for particular transistors and diodes are outlined in Table A1-1. (Numbers correspond to those used in Fig. 2-18.)

Table A1-1

Characteristics of Transistors and Diodes which are Selected

Transistor or Diode	Selected Parameters
Q_1, Q_2	$\beta > 300$ at $I_c = 100\ \mu A$. $I_{CBO} < 2.5 \times 10^{-10}$ A at 20 V. Base-to-emitter voltage match within 10 mV at $I_c = 100\ \mu A$.
D_1, D_2	I_L (reverse leakage current) $< 10^{-11}$ A at 15 V. Diodes are selected so that the forward voltage of D_1 plus the base-to-emitter voltage of Q_1 at 100 μA is equal to the sum for D_2 and Q_2 within 2 mV.
Q_3, Q_4	$\beta > 25$ at $I_c = 0.2\ \mu A$. $I_{CBO} < 10^{-11}$ A at 20 V.
D_3, D_4	Selected to minimize OFF-state input currents. See Section D.
Q_5	$\beta > 40$ at $I_c = 400\ \mu A$.
Q_6	$r_c > 4$ M at $I_c = 400\ \mu A$.
D_5, D_6	Selected for temperature compensation. See Section D.
Q_7	$r_c > 5$ M at $I_c = 200\ \mu A$.
Q_8	$r_c > 5$ M at $I_c = 200\ \mu A$.
Q_9	$r_c > 5$ M at $I_c = 250\ \mu A$. $\beta > 40$ at $I_c = 250\ \mu A$.
Q_{10}, Q_{11}	$\beta > 40$ at $I_c = 200$ mA. $\beta > 25$ at $I_c = 100\ \mu A$. Base-to-emitter voltage match within 10 mV at $I_c = 100\ \mu A$.
Q_{12}, Q_{13}	Same as Q_{10}, Q_{11}.
D_{16}, D_{17}	$I_L < 10^{-11}$ A at 15 V.

D. INITIAL AMPLIFIER ADJUSTMENTS

There are certain adjustments which are performed on the gated-amplifier circuits following preliminary testing. These adjustments are made in the following order: (See Fig. 2-18).

1. OFF-state input current. This is adjusted by selecting diodes D_3 and D_4 with leakage currents equal to uncompensated OFF-state input currents.

2. ON-state input current. Several steps are required to make this adjustment. The amplifier is first voltage balanced by placing a selected resistor across the terminals from R_{3A} to R_{3C} on the circuit board, and is then connected as a unity-gain amplifier (direct connection from the output to the negative-gain input terminal). Positive-gain input current can then be measured directly. Resistor R_{1A} is selected about ten percent lower than the actual value ($R_{1A} + R_{1B}$) required to reduce the input current to zero and is soldered in place. Resistor R_{1B} is used as a vernier to finalize the adjustment. This resistor is not permanently connected to permit future adjustments if required to compensate for power-supply-voltage changes or to zero input current at some temperature other than room temperature. Negative-gain input current is measured by connecting the positive-gain terminal to ground and connecting a 10-M resistor from the output to the negative-gain input. In this case it can be shown that the amplifier output voltage is -10^7 times the negative-gain input current. The current is reduced to zero by adjustment of R_{2A} and R_{2B}.

3. Voltage drift vs. temperature is the final adjustment. The amplifier is connected for a non-inverting gain of 100 (as explained in Chapter III) and the positive-gain input terminal is grounded. This forces an output voltage which is 100 times the drift referred to the input. Resistor R_{3A} is selected to be approximately 4 K less than the total value ($R_{3A} + R_{3B} + R_{3C}$) required to achieve zero drift with two arbitrarily selected diodes inserted for D_5 and D_6. The amplifier output is then

set to zero volts (with D_5 and D_6 in place) by placing a single resistor in the location normally occupied by R_{3B} and R_{3C}. The amplifier is temperature cycled from 0°C to + 50°C, and if the valley temperature is not between 20°C and 30°C, a new set of diodes is selected for D_5 and D_6. If the total forward voltage across D_5 and D_6 is increased by 20 mV, the valley temperature increases by approximately 10°C, and this relationship is used as an aid in selecting the replacement diodes. The amplifier is then temperature cycled a second time to insure correct compensation. Resistors R_{3B} and R_{3C} are used as coarse and fine voltage-drift adjustments, and are selected after temperature compensation is completed. Resistor R_{3C} is not permanently connected, and may be changed to compensate for changes in supply voltage, or to reduce the drift at some particular temperature to zero.

While the component selection and adjustment procedures outlined in Sections C and D are somewhat complex, they are justified in terms of improved amplifier performance and uniformity. While not every parameter of every completed amplifier was tested, the finished amplifiers show amazing consistency of such important characteristics as open-loop gain, step response for specific feedback connections, and maximum output current, and this allows direct interchangeability in system design.

The total time required for component selection and final amplifier adjustment averaged two days for each amplifier, with possibly four hours of this time devoted to preliminary amplifier tests. As mentioned earlier, some of this time would be required in any flight program to insure reliability of the semiconductors. It is felt that this time could be reduced somewhat by the increased familiarity and somewhat more systematic test procedures that would evolve during a large-scale construction program. Furthermore, most of the work involved in this phase of the construction can be performed by skilled technicians as opposed to professional staff.

E. SUGGESTIONS FOR IMPROVED PACKAGING

The packaging described in Section A is not intended for use in flight systems or even as a prototype for final packaging. While the construction method used in this research is mechanically acceptable (at least if the final circuit is potted) from a reliability point of view, the size requirement of 19 cubic inches per amplifier precludes the use of this method in any but the most simple space experiments.

Several acceptable methods of repackaging are available for use in space systems. One of these is packaging in integrated-circuit form. The types of components required prevent monolithic (or single-chip) integration of the gated-amplifier circuit with present-day technology. It should be possible, however, to integrate the circuit on two or more chips, with different chips used for different transistor types. All transistors, diodes, and low-value resistors and capacitors could be included on these chips. High value resistors could be deposited, and decoupling and adjustment components included external to the rest of the circuit. This approach would require a rather involved development program, but should result in an extremely small circuit. Bandwidth would probably be at least a factor of two higher than the amplifier described in this report because of lower node capacitance.

An intermediate approach is construction in discrete-component printed-circuit cordwood form. This technique has been used for circuits of equivalent complexity intended for use in space systems.[11] It would be necessary to replace most components used in the gated amplifier with physically smaller components as listed below:

1. All transistors should be obtained in a TO-46 or smaller package. This type of repackaging is available from most semiconductor manufacturers.

2. All resistors should be replaced with 1/8-watt units. This would not affect reliability since all resistors operate at less than 2-mW average power.

3. All ceramic capacitors should be replaced with 50-volt units. This would not affect reliability since all capacitors used in the circuit operate at less than 20 volts.

4. The values of capacitors used for decoupling should be reduced. This would be possible since the shorter lead lengths inherent to this type of packaging reduce decoupling requirements.

Repackaging in cordwood form should reduce the volume of the gated-amplifier circuit to approximately 1.5 cubic inches and this size should be adequate for many applications. The bandwidth of the circuit would probably be increased by 20 percent to 30 percent because lower node capacitances are possible with this method.

APPENDIX II

THE MULTIPLE-INPUT GATED AMPLIFIER

The basic gating techniques used in the gated-amplifier circuit can be extended to a type of circuit that I call a multiple-input gated amplifier. An appropriate multiple-input gated-amplifier design can be used in any gated-amplifier application described in this report. Furthermore, the versatility of a multiple-input gated amplifier is greater than that of the gated amplifier, since a single multiple-input circuit can be used for multiplexing operations.

A model for the multiple-input gated amplifier is shown in Fig. A2-1, and this model has N+1 states as follows:

1. All switches are open and the amplifier requires minimum power.

2. The switch at the output, the input terminal labeled minus, and the +1 input are closed, but all other switches are open. In this case

$$E_{out}(s) = [E_{+1}(s) - E_{-}(s)]\, A(s)$$

3. The switch at the output, the input terminal labeled minus, and the +K input (K = 2 to N) are closed, with all other switches open.

$$E_{out}(s) = [E_{+K}(s) - E_{-}(s)]\, A(s)$$

This circuit can be used to eliminate several gated amplifiers in some applications. For example, many experiments have a number of different outputs which are often sampled and A-D converted sequentially. With the circuit shown in Fig. 5-14, N signals could be connected to the N positive inputs, and the output connected to the negative input and also to a capacitor to ground. The various inputs could then be independently sampled. Selection of any one of N signals is also possible in a continuous rather than a sampling mode, and this type of connection could be quite useful for conventional analog computation as explained in Chapter IV. The "N-to-one" switch is obtained if the output is connected to the negative input terminal and the N signals applied to the N positive input terminals.

This type of circuit could be developed by appropriately interconnecting a number of gated amplifiers. There is a much simpler alternative which is outlined in Fig. A2-2. A two-input circuit is shown for simplicity. With the first current source on, the input stage consists of Q_1 and Q_2, and the output is proportional to $E_{+1} - E_1$. With the second current source on, the input stage is formed by Q_1 and Q_2', and the output is proportional to $E_{+2} - E_-$. The common output stage is gated on whenever either of the two input stages is on.

The concept can be extended by adding one input transistor, two diodes, and a current source for each additional input. An economy of components is achieved by sharing a common output section, the most complex portion of the gated amplifier, among many individually-selectable input stages.

The components comprising the input stages are matched in groups. The base-to-emitter voltage of Q_1 plus the forward voltage of D_1 are selected to be equal to the corresponding values for Q_2 and D_2. Similarly, the voltage across Q_1 and D_1' is made equal to that across Q_2' and D_2'. In contrast to the gated amplifier, it is not possible to achieve balance for all inputs by varying the resistor shown in Fig. A2-2. Instead, the magnitudes of the current sources are varied to reduce input drift.

The same type of input-circuit modifications described earlier in connection with the gated amplifier can be used to improve the performance of this type of multiple-input stage. Examples include transistors to compensate ON-state input current and reverse-biased diodes to compensate OFF-state input current.

It should be possible to achieve performance which is equivalent to that of the gated amplifier with the single exception of somewhat reduced bandwidth. This arises since the total capacitance seen at the input node of the final amplifier is increased by multiple input transistors. The increased capacitance should reduce the bandwidth approximately a factor of two below that of the gated amplifier for a six-input design. The operating current levels can be increased in order to increase bandwidth in applications where increased power consumption is tolerable.

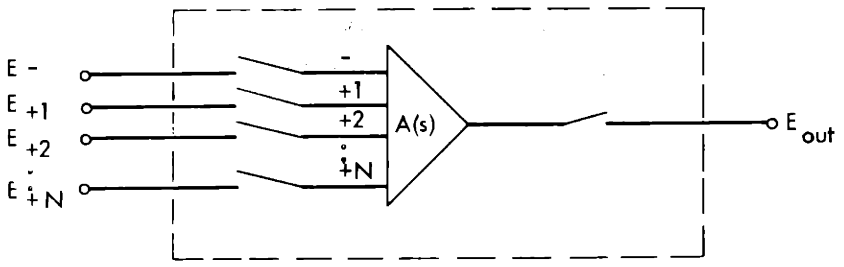

Fig. A2 - 1 Model for Multiple-Input Gated Amplifier

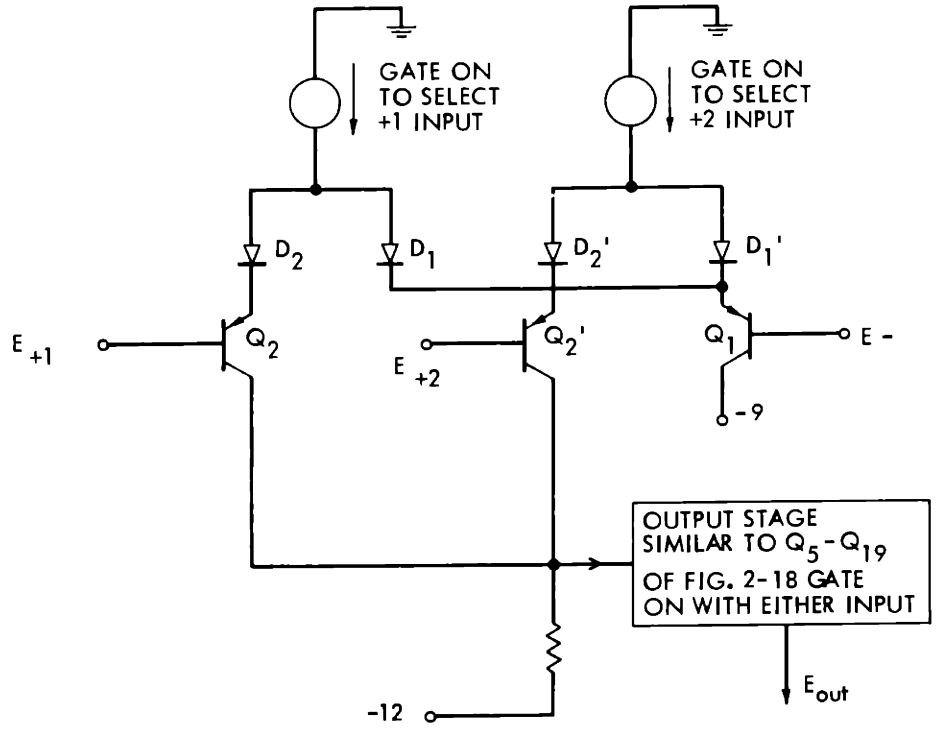

Fig. A2 - 2 Two-Input Gated Amplifier

A multiple-input gated amplifier which operates at the low power levels of the gated amplifier described in this report has not been designed. I have, however, demonstrated the feasibility of the basic approach with a 2-input gated amplifier intended for use as an analog switch.[14] The switch provides very low output impedance and low crosstalk between the OFF input signal and the switch output. Power consumption was not critical in this particular application, and component types and current levels were altered in order to obtain 80-Mc bandwidth through the switch and 25-ns transfer time between inputs.

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BIOGRAPHICAL SKETCH

James K. Roberge was born in Jersey City, New Jersey, on June 13, 1938. He received the S.B. and S.M. degrees in electrical engineering from the Massachusetts Institute of Technology, Cambridge, Massachusetts in 1960 and 1962 respectively.

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