Intelligent Field Emission Arrays

by

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ABSTRACT

Field emission arrays (FEAs) have been studied extensively as potential electron sources for a number of vacuum microelectronic device applications. For most applications, temporal current stability and spatial current uniformity are major concerns. Using the kinetic model of electron emission, field emission can be described as two sequential processes— the flux of electrons to the tip surface followed by the transmission of the electrons through the surface barrier. Either of these processes could be the determinant of the emission current. Unstable emission current is usually due to absorption/desorption of gas molecules on the tip surface (barrier height variation) and non-uniform emission is usually due to tip radius variation (barrier width change). These problems could be solved if the emission current is determined by the electron supply to the surface instead of the electron transmission through the surface barrier. In this thesis, we used the inversion layer of a MOSFET to control the electron supply. It results in additional benefits of low turn-on voltage and low voltage swing to turn the device on and off.

A novel CMP-based process for fabricating integrated LD-MOSFET/FEA is presented. We obtained FEA devices with an extraction gate aperture of 1.3 μm and emitter height of 1 μm. We present a comprehensive study of field emitter arrays with or without MOSFET. The silicon field emitter shows turn-on voltage of ~24 V with field enhancement factor (b_{FN}) of ~370. We demonstrated that the LD-MOSFET provides excellent control of emission current. The threshold voltage of the LD-MOSFET is ~ 0.5V. The integrated device can be switched ON and OFF using a MOSFET gate voltage swing of 0.5V. This results in an ON/OFF current ratio of 1000:1. The current fluctuation is significantly reduced when the MOSFET is integrated with the FEA device and the device is operated in the MOSFET control regime. The emission current of the integrated LD-MOSFET/FEA remains stable regardless the gas and vacuum condition. The saturation current level of the integrated devices in the MOSFET controlled region is also the same regardless the emitter array size or the FEA's position on the wafer.

We also present a comprehensive study of three-dimensional oxidation in silicon emitter tip formation. Stress plays an important role in the oxidation mechanism. A new sharp emitter tip formation mechanism is proposed: rather than a continuous oxidation process,

an emitter neck breaking stage occurs before the sharp emitter tip is formed. Stress from volume difference of silicon and silicon dioxide is the main cause for the emitter neck breaking. Initial formation of microcracks around the neck occurs at high temperature due to volume difference stress, oxide grows into the cracks right after crack formation, and a sharp emitter tip is then formed by further oxidation.

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1. Introduction

Field emission is the ejection of electrons from a solid surface into a vacuum when high electrostatic fields are applied. The phenomenon consists of the tunneling of electrons through the potential barrier at the surface, deformed by the applied electrostatic field. It is different fundamentally from thermionic emission or photoemission, where only electrons with energy higher than the potential barrier are ejected [1.1].

Typically, field emission devices are fabricated as arrays of microstructures. These microstructures are called field emission arrays (FEAs). There are also other types of field emitter structures such as field emission ridges and thin film field emitters, but the cone shape field emitters are the most widely used field emission structure. FEAs are being studied as electron sources for several applications, such as flat panel display, radio frequency (RF) amplifier and sensor, multi-beam electron lithography, etc. Most commonly used field emission materials are metals such as molybdenum. The physics of the field emission from metals is well studied [1.2] and the fabrication process for metal field emitters is mature [1.3]. Silicon-based FEAs, on the other hand, offer some potential benefits and they are compatible with silicon IC technology [1.4-1.6]. Silicon FEAs have also been fabricated in our laboratory using metal or polysilicon gates [1.7], and have been proposed for achieving of high current density and low-voltage field emission. Silicon FEAs also have good emission characteristics and reliability. Furthermore, silicon emitter tips could be sharpened by oxidation and the properties of the silicon emitters could be easily changed by altering doping concentration.

In this chapter, we will briefly present some field emission applications. We will then discuss the performance issues for field emission devices in these applications and discuss the traditional approaches to improve the performance.

1.1 Field Emission Applications

There are many applications relying on the extraction of electrons into a vacuum by the electrostatic field, such as field emission displays, RF amplifiers, lithography, switches, etc. This section will briefly introduce two field emission applications.

Field Emission Display

The predominant application for FEAs is the field emission display (FED). The bulky cathode ray tube (CRT) dominated the television and computer monitor market in the last few decades. However, they are being replaced by flat panel displays in the last few years. The current dominant flat panel display technology is liquid crystal display (LCD), which has several advantages over CRTs and other flat panel display technologies. However, it also has some inherent performance disadvantages. Liquid crystal in LCD acts as a spatial light modulator or light valve that either blocks or transmits light coming from a light source. In addition to the liquid crystal, LCD consists of several diffusers, polarizers, and filters. These layered components in LCD result in reduced brightness, lower luminous efficiency, and smaller viewing angle. Moreover, LCD can only operate within a rather narrow temperature range because of the material property of the liquid crystal. These disadvantages motivated the study of an alternative display technology based on cathodoluminesence – the field emission display.

FED is essentially a thin flat CRT. It has CRT's advantages of high spot brightness, large viewing angle, and higher luminous efficiency without CRT's bulky package and substantial power dissipation. FED and CRT are similar in concept in that an electron beam strikes the phosphor where hole-electron pairs are created and radiative recombination of electrons and holes produces light [1.8-1.10]. However, unlike a CRT which uses a raster-scanned single electron source to generate images on a phosphor screen, the FED generates images by using a two-dimensional array of matrix-addressed

micro-electron sources which are proximity focused on a phosphor screen. Since there is no need in FED to raster the electron source, it is possible to reduce the cathode-anode separation and obtain a thin flat display. The schematic diagram of a typical FED is shown in Figure 1-1. The front plate of the FEA is composed of a glass faceplate (phosphor screen) coated with a layer of indium tin oxide and phosphors. A FED pixel consists of several field emitters that are proximately focused on the phosphor screen. The space between the cathode and the phosphor screen must be kept under vacuum. Electrons tunnel out from the field emitters into vacuum when a high electric field is applied to the gate of the field emitters. The device performance (current density, operating voltage, beam spread, temporal and spatial uniformity) is essentially determined by the energy barrier formed between the emitter (metal or semiconductor) and vacuum.

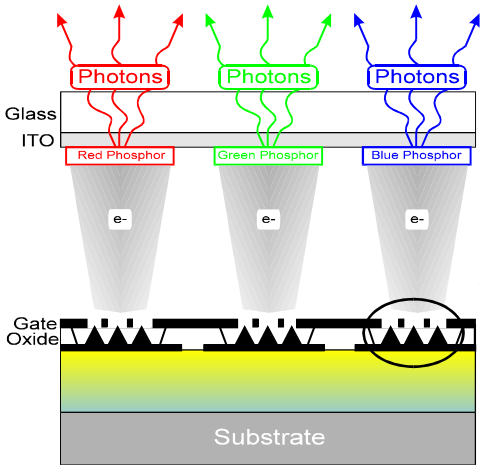


Figure 1-1. Schematic of a typical FED.

The non-linear and exponential current-voltage characteristic makes the FEAs suitable for matrix addressing without the need for a non-linear switching element such as thin film transistor (TFT) in active-matrix liquid crystal display (AMLCD) [1.11]. In a typical FED configuration, the rows of the display are connected to the emitters while the gates are connected to the columns. Both are biased at about half the operating voltage

($V_{op}/2$) initially [1.11]. The selection of a row changes the row voltage from $V_{op}/2$ to 0 V while the selection of a column changes the column voltage from $V_{op}/2$ to $V_{op}/2 + V_{data}$, where V_{data} corresponds to the pixel gray scale. V_{data} can take a value between 0 V and $V_{op}/2$. The non-linear device characteristic ensures that only the selected pixel would emit electrons. The extracted electrons are accelerated to the phosphor screen by an electric field due to large potential difference between the anode and the cathode. Light is generated where the emitted electrons strike the appropriate pixel on the phosphor screen.

Microwave Power Amplifier Tubes

There are basically two types of power amplifiers, one is the vacuum tube and the other is solid-state transistor. Typically, the vacuum tubes are made from thermionic cathodes. These vacuum tubes have several limitations because they need to be heated at very high temperature for electron emission to occur. The greatest drawback of the vacuum tubes is their limited lifetime associated with the degradation of thermionic cathodes. For low power applications, solid-state transistors substitute the vacuum tubes as better amplifiers. However, for high power applications, the transistors need to be operated in parallel with complex microstrip combining circuits and bulky thermal management equipment. In contrast, vacuum tubes could be compact and efficient. The incorporation of cold cathodes, FEA, in vacuum tubes for high power applications provides the best features of both vacuum tubes (high power) and power transistor (long lifetime) [1.12].

The nonlinear high-voltage impedance of field emitters makes them suitable for peak sharpening, modulation, and detection in high-voltage circuits, especially in pulsed operation at microwave frequency, where high instantaneous currents can be drawn [1.13]. Linear-beam device known as the traveling-wave tube (TWT) is commonly used in microwave power amplification. Figure 1-2 shows the structure of a TWT where the electron source is replaced by the FEA [1.14]. The beam modulation in the microwave tube is still performed in the conventional way. Field emitter cathode produces an

electron beam that is then focused and accelerated down a beam tunnel surrounded by a wire helix. At the cathode end of the helix, the microwave input signal causes the electron beam to bunch into small clusters of electrons. These bunches gain energy as they are accelerated down the beam tunnel. At the output end of the helix, the added kinetic energy is extracted by the helix and an amplified signal is output [1.5,1.15].

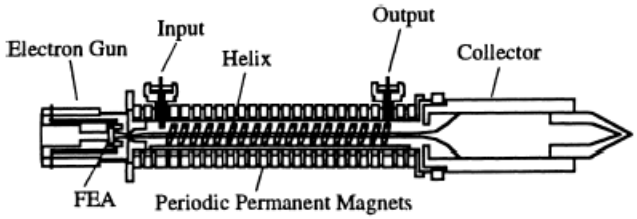


Figure 1-2. Structure of a TWT, in which the electron source is replaced by a FEA [1.14].

1.2 Statement of the Problem

FEA technology, while adequate for a number of applications, has four major shortcomings: spatially non-uniform emission current, temporally unstable emission current, high addressing voltages, and device lifetime.

The spatial non-uniformity and temporal instability of the emission current stem from the inherent nature of the electron emission process—electron tunneling through a barrier. Electrons tunnel out of the emitter when the barrier is made narrow by the application of a gate voltage. Spatial and temporal non-uniformity in the emission current occur with small changes in the barrier height or width. The non-uniform and unstable emission current degrades the resolution and the quality of the field emission device. Field emission applications require stable and uniform electron emission sources.

Most field emission applications also require low voltage operation. However, in order to have high enough electric field on the field emitters, the addressing voltages are

usually very high. Low voltage operation would reduce the power dissipation in the addressing electronics [1.13, 1.16]. The power dissipated is:

$$E = CV_g^2 f \tag{1.1}$$

where C is the load capacitance and f is the switching frequency. Reduction of the power dissipation would increase the overall power efficiency of the device.

This dissertation would not address field emission device lifetime because it is outside the scope of this thesis.

1.3 Objectives and Technical Approach

The objectives of this thesis are to fabricate a high performance field emission device, which has (1) spatially uniform emission current, (2) temporally stable emission current or lower noise, and (3) low operating voltage.

Traditionally, emission current non-uniformity and instability problems have been addressed by adding a series resistor to the field emission device [1.17]. This negative feedback "ballast" resistor is used to achieve spatial uniformity and stabilize the current by creating a load line as shown in Figure 1-3. Without a ballast resistor, and at a given extraction gate voltage, the emission current depends exponentially inverse of the field factor β (barrier width). Slight changes in the work function and the field factor result in huge changes in the current. The field factor is roughly inversely proportional to the tip radius. Shown in Figure 1-3 is a plot of the field emission current as a function of extraction gate voltage at various tip radii. At a particular extraction gate voltage, small changes in tip radius results in huge changes in the emission current because of the exponential dependence.

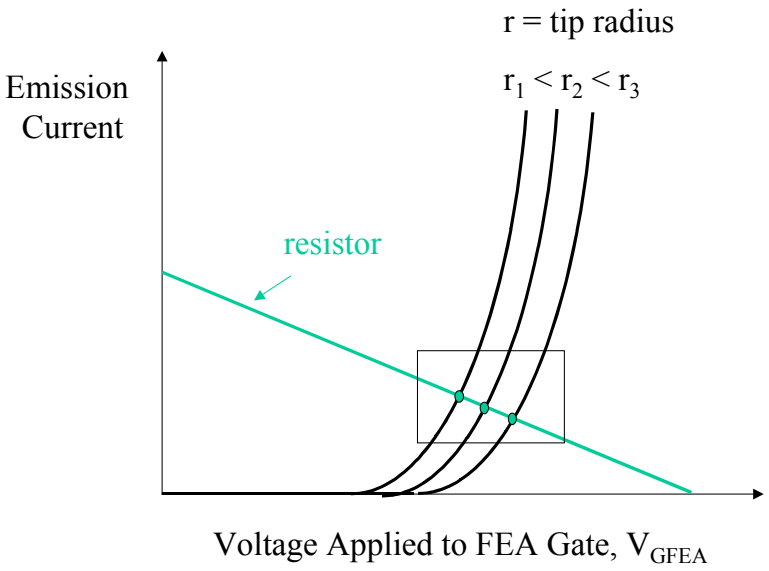


Figure 1-3. The operation of field emission devices integrating with a resistor.

The addition of a resistor in series with field emitter establishes a load line that in effect divides the voltage applied to the extraction gate (V_{GFEA}) between the field emitter (extraction gate to emitter voltage, V_{GE}) and the resistor (IR).

$$V_{GFEA} = V_{GE} + IR \tag{1.2}$$

Increases in emission current result in lower voltage drop across the field emitter and thus lower emission current, hence a negative feedback effect. This stabilizes the emission current to variations in the work function (barrier height) and tip radius (barrier width). We shall provide a mathematical derivation later.

This resistor load line can accommodate the variations in the field emission curves. The ballast resistor provides a high dynamic resistance that keeps the difference of the operating currents considerably smaller. The operating current becomes more uniform as the resistance of the series resistor increases. One approach is to create a resistive mesh on which FEAs are placed, as shown in Figure 1-4 [1.13,1.18].

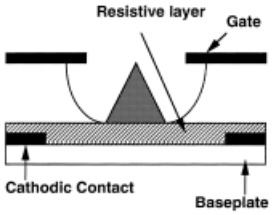


Figure 1-4. Integrating the resistive layer with the field emitters [1.13].

This ballast resistor moderately improves the field emission device performance in achieving stable and uniform emission current. However, it does not solve the high operating voltage problem. In this thesis, we will explore the sources of the temporal and spatial variation of field emission device performance and propose a compact and efficient approach to improve the device performance.

1.4 Thesis Organization

The outline of this thesis is as follow:

Chapter 2 of this thesis reviews the physics of field emission. Next, the sources of the less than optimal performance of field emission devices are explored. An approach to improve the field emission device performance is proposed. Then, we will review the basic physics of MOSFET device. Finally, the theoretical framework of the intelligent FEA is developed and discussed in detail.

In Chapter 3, we outline the fabrication process for silicon field emitters. The silicon emitters are fabricated using isotropic silicon etching and oxidation sharpening. The fabrication process to achieve uniform and sharp silicon field emitters is presented. Oxidation sharpening is discussed in detail and a new mechanism of sharp emitter formation is proposed. Three-dimensional oxidation process and mechanism are also presented.

In Chapter 4, we present the design of the intelligent FEA device and the fabrication process of integrating the lightly doped drain-MOSFET (LD-MOSFET) with silicon FEA. Integrated devices are fabricated by (1) using the process discussed in Chapter 3 to form sharp and uniform silicon emitters, (2) chemical mechanical polishing (CMP) to form self-aligned FEA extraction gate, and (3) modified standard CMOS base-line process to form a LD-MOSFET.

In Chapter 5, the current-voltage characterizations of the three-terminal device, field emission arrays, are presented. Device characterization results and analysis are reported.

In Chapter 6, the current-voltage characterizations of the four-terminal device, integrated LD-MOSFET/FEA, are presented. Device characterization results and analysis are reported.

Chapter 7 presents the summary of this thesis and suggestions for future work.

Appendices contain more detail mask-set and processing information, three-dimensional oxidation simulation results, derivations of current sensitivity to work function and the field factor, and current-voltage characterizations of field emitter ridges.

2. Field Emission Theory

2.1 Field Emission

Metal has a free gas of electrons confined by a potential barrier. In order to eject the electrons from a metal surface into the vacuum, it is necessary to remove the electrons from the potential well in which they are trapped. The potential barrier between the highest normally occupied electron energy level inside the metal and the vacuum level is called work function. Ejections of electrons from inside the metal to the vacuum can be accomplished in two ways as shown in Figure 2-1. First is to raise the energy of the electrons to exceed the potential barrier as in photoemission and thermionic emission. Second is to reduce the width of the potential barrier at the surface with applied electric field so that electrons can tunnel through the barrier and cause field emission. In this thesis, we focus on the electron field emission. Field emission is a quantum mechanical tunneling phenomenon. In contrast to the thermionic emission from filaments, field emission occurs at room temperature from unheated cathodes under an electric field [2.1].

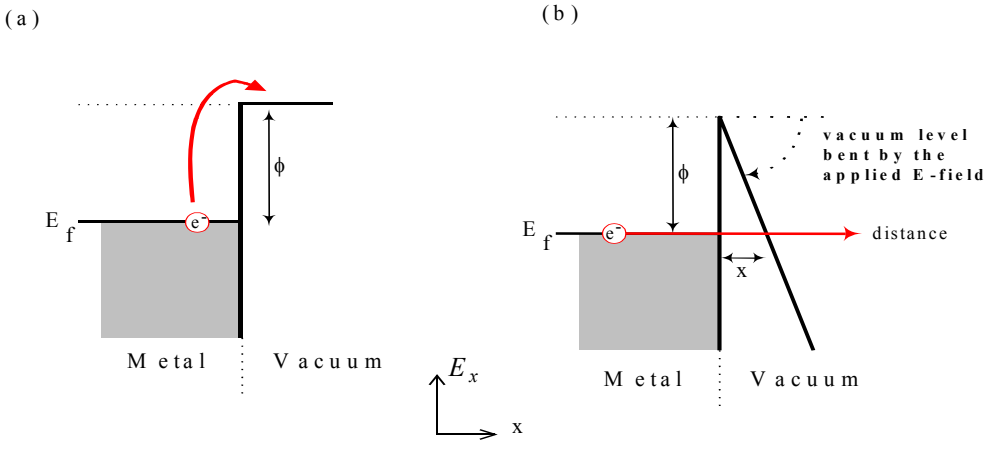


Figure 2-1. Two ways of electron ejection: (a) thermionic emission or photoemission, and (b) field emission. ϕ is the work function.

Using the kinetic model of electron emission, field emission can be described as two sequential processes -- the flux of electrons to the tip surface followed by the transmission of the electrons reaching the surface through the surface barrier. Either of the processes could dominate the emission process. In metals, electrons are in a partially filled conduction band and the supply of mobile electrons is relatively high. In the field emission process from metal surface, the emission current is limited solely by the transmission of electrons through the surface barrier [2.2, 2.3]. Similar to metals, semiconductor can also be described as having a free electron gas; however, there are two bands. The electron supply comes from two bands: the conduction band and the valence band, which are separated by a bandgap, E_g. For conduction band electrons, the surface barrier height is the electron affinity χ, while for the valence band electrons, the surface barrier height is $\chi + E_g$. Semiconductor has an almost empty conduction band and the supply of electrons is relatively limited. Doping or the application of an electrostatic field to form a two-dimension (2D) Fermi-sea such as an inversion layer or an accumulation layer could change the electron density in the conduction band [2.4-2.8]. As a result, electron emission from semiconductors is limited either by the transmission through the energy barrier or the electron supply to the emission surface.

Field emission process in a semiconductor is similar to that in a metal. However, the effects of surface states and field penetration have to be taken into account. Unlike metals, the electric field will penetrate into the semiconductor surface and reach into the semiconductors. A sea of electrons will form at the interface due to accumulation or inversion of the surface. This accumulation or inversion layer makes the semiconductor behave like a metal. Figure 2-2 is a schematic of the electron emission at the surface of an n-type silicon showing field penetration and the formation of an accumulation at the surface.

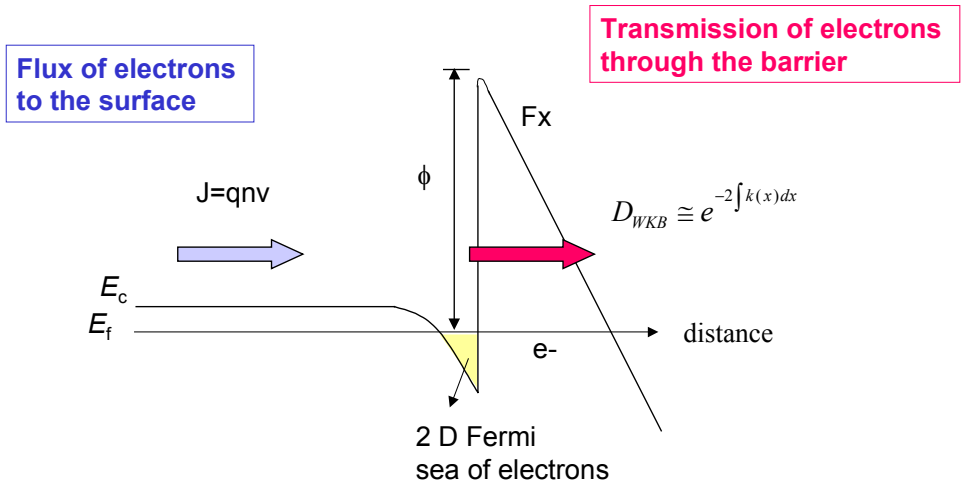


Figure 2-2. Schematic of the electron emission at the surface of an n-type silicon.

The field emission current density,

$$J(V,E_x) = e\int_0^\infty D(V,E_x)N(E_x)dE_x \quad (\text{A/cm}^2), \tag{2.1}$$

where D(V, E_x) is the transmission probability at normal kinetic energy (E_x), and electron potential energy V; while N(E_x) is the supply function comprised of the available electron states and the occupation of the states as determined by the Fermi function. As the applied field on the solid surface increases, the vacuum level would bend and the width of the energy barrier decreases. Electrons are able to tunnel from the Fermi-sea to vacuum when the barrier width is less than 1 or 2 nm. As the barrier width decreases, the transmission probability of electrons increases and hence the emission current increases. The electron transmission probability for one-dimensional barriers can be modeled using the Wentzel-Kramers-Brillouin (WKB) approximation,

$$D_{WKB}(V,E_x) \cong e^{-2\int k(x)dx}, \tag{2.2}$$

and

$$k = \sqrt{\frac{2m}{\hbar^2}(V - E_x)}\ . \tag{2.3}$$

$$V = -F \bullet x \tag{2.4}$$

where F (in volts/cm) is the applied field on the emitter surface and x (in cm) is the width of the barrier. If we limit electrons to ones at the Fermi-level,

$$E_x \cong -\phi \text{ (vacuum level as a reference point)} \tag{2.5}$$

where ϕ (in volts) is the work function of the emitter material.

The transmission probability for the electrons at the Fermi-level,

$$D_{WKB}(\phi, F) \cong e^{-2\int k(x)dx} \tag{2.6}$$

and

$$k = \sqrt{\frac{2m}{\hbar^2}(\phi - F \bullet x)}\ . \tag{2.7}$$

The emission current density equation can be reconstructed as

$$J = \frac{AF^2}{\phi t^2(y)} \exp(-B\frac{\phi^{3/2}}{F} v(y))\ , \tag{2.8}$$

where $A = 1.54 \times 10^{-6}$, $B = 6.87 \times 10^7$ and $y = 3.79 \times 10^{-4} F^{1/2} / \phi$. $v(y)$ and $t^2(y)$ are the Nordheim elliptical functions added to account for image charge effects [2.9]. Their values are well approximated by $t^2 = 1.1$ and $v(y) = 0.95 - y^2$. Substituting $J = I / \alpha$ and $F = \beta \times V$ into the equation, where α is the emitting area, I is the emission current, β is the local field conversion factor at the emitting surface, and V is the voltage applied to the extraction gate, the Fowler-Nordheim (F-N) equation, which is the current-voltage relationship of the field emission device, can be obtained as follow:

$$I = a_{FN} V^2 \exp(-b_{FN}/V)\ , \tag{2.9}$$

$$a_{FN} = \frac{\alpha A \beta^2}{1.1\phi} \exp\left[\frac{B(1.44\ x10^{-7})}{\phi^{1/2}}\right], \tag{2.10}$$

and

$$b_{FN} = \frac{0.95\, B \phi^{3/2}}{\beta}. \qquad (2.11)$$

The barrier height of the F-N equation is replaced by the electron affinity of silicon, χ, which is 4.05V in silicon [2.10].

Field Emission Device

A typical field emission microstructure consists of an emitting surface (metal or semiconductor) with a small tip radius located within a conducting gate electrode containing an annular aperture. Figure 2-3 is a schematic of the field emission microstructure. When the gate electrode is biased relative to the emitter, a very high electric field appears at the tip apex and nearby. The high electric field reduces the surface barrier width and consequently increases the electron emission probability. Electrons are extracted by tunneling from the emitting surface when the gate electrode voltage is high enough [2.9,2.11]. It takes around 10 MV/cm of the electric field to obtain reasonable emission current [2.1]. The gate electrode and the emitter electrode are separated by insulator. The emitted electrons are collected by the anode, which is typically several millimeters away from the emitter cone and is biased at a high voltage.

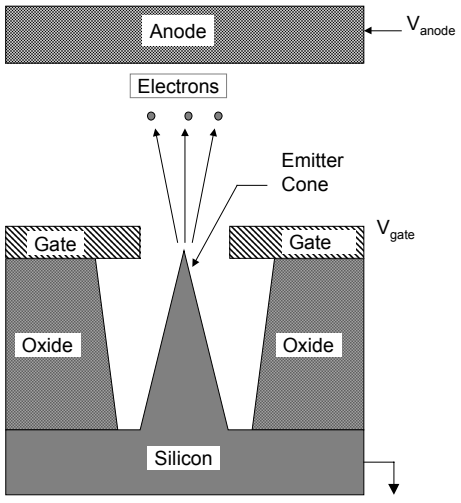


Figure 2-3. Schematic of a field emission microstructure [2.13].

A good model to describe the geometry effects on the electric field in a field emission microstructure is the ball-in-a-sphere model as shown in Figure 2-4 [2.12]. The interior ball is analogous to the cone tip and the outer sphere is the gate structure. The ball in a sphere can be solved analytically in spherical coordinates. A solution to Laplace's equation with boundary conditions

$$V\ (\ r\ )\ =\ 0\ ,V\ (\ d\ )\ =\ V\quad , \tag{2.12}$$

gives the electric field at the tip surface to be

$$F\ =\ \frac{V}{r}\left[\ \frac{d}{d\ +\ r}\right]\ , \tag{2.13}$$

where d is the distance between tip center and the gate, and r is the radius of curvature of the tip [2.11]. To the first order, where d >> r,

$$F\ \approx\ \frac{V}{r}\ , \tag{2.14}$$

in other words,

$$\beta\ \approx\ \frac{1}{r}\ . \tag{2.15}$$

The electric field is independent of the gate aperture and is inversely proportional to the radius of curvature of the emitter tip. The sharper the emitter is, the larger the field that can be generated around the tip apex and nearby.

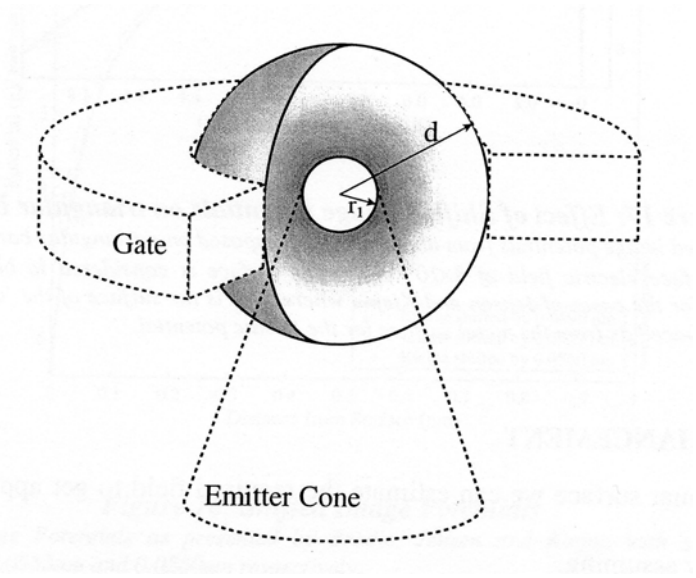


Figure 2-4. Ball-in-a-sphere model [2.12].

2.2 Sources of the Non-Uniform and Unstable Emission Current

Spatial Uniformity

As mentioned in the previous section, the transmission coefficient, predicted by WKB approximation, depends on both the work function of the emitter material and the field we apply on the emitter surface. Here, the applied field is first considered. As discussed earlier, the sharper the emitter is, the larger the field factor, β is. Hence, the field generated on the emitter surface would be larger for the same magnitude of the applied voltage as β increases. To the first order, the transmission coefficient depends exponentially on the negative of the emitter tip radius. Unfortunately, the emitter tip radius varies spatially even with very careful fabrication process. Typically the tip radius has a distribution similar to that shown in Figure 2-5 (a). Better control of the process would provide a tip radius distribution with narrower width; however, it would not completely eliminate the variation. The emitter tip formation processes developed by D. Pflug, has a log normal distribution with the width of 0.5 nm [2.12]. Due to the exponential dependence of current on the negative of the tip radius, a very small

difference in tip radius would result in orders of magnitude variations in the emission current at an applied extraction gate voltage as shown in Figure 2-5 (b).

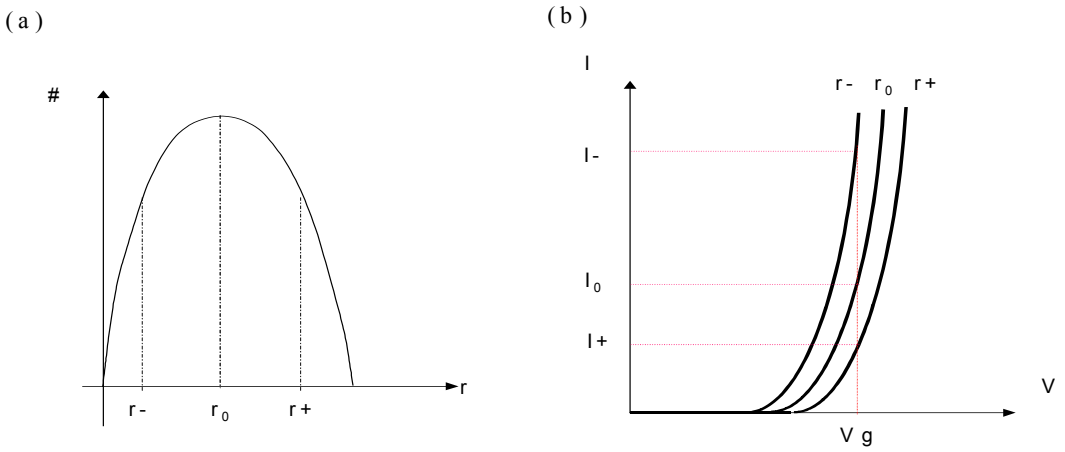


Figure 2-5. (a) Emitter tip radius distribution. (b) Small difference in emitter radius results in large difference in emission current.

How tip radius changes the emission current can be expressed by the following equations by assuming that the work function of the emitter ϕ is constant:

$$I = f(r) \tag{2.16}$$

$$\frac{\Delta I}{I} = \frac{\partial I / \partial r}{I} \times \Delta r \tag{2.17}$$

$$I = \frac{\alpha A}{1.1 r^2 \phi} \exp\left[\frac{B\left(1.44 \times 10^{-7}\right)}{\phi^{1/2}}\right] V^2 \exp\left(-0.95 B r \phi^{3/2} / V\right) \tag{2.18}$$

$$\frac{\Delta I}{I} = \frac{\partial I / \partial r}{I} \times \Delta r = \left[\frac{-2}{r} - \frac{0.95 \phi^{3/2} B}{V}\right] \times \Delta r \tag{2.19}$$

Detail derivation is shown in Appendix H.

There are several solutions to this spatial non-uniformity. These are (1) make uniform emitters and (2) control the device with a current source. The first solution is nearly impossible using existing fabrication techniques. The second solution is basically to add

a current source to the field emission device so that the emission current would only be dependent on the current source and not the field emitter tip sharpness. This approach will be discussed in detail in the following section.

Temporal Stability/Lower Noise

Transmission coefficient is dependent on the work function of the emitter material. When the field emission device is operated in the vacuum environment, the residual gas molecules would absorb and desorb randomly on the emitter surface. This absorption/desorption changes the surface work function with time as depicted in Figure 2-6 (a). The adsorbed molecule can be considered as a dipole aligned perpendicular to the surface. If the dipole has its negative charge away from the surface, the work function is increased [2.6]. It could be described by the following equations:

$$\phi(t) = \phi_0 + \Delta\phi(t) \tag{2.20}$$

$$\Delta\phi(t) = 2\pi P_i N_s \theta \tag{2.21}$$

where ϕ_0 is the original work function of the emitter material, N_s = maximum number of adsorption sites per unit area on the surface, P_i = dipole moment for each adsorbed particle, and $\theta(t)$ = amount of coverage at time t [2.14]. θ would change as the pressure changes and eventually it would reach an equilibrium value θ_{eq}:

$$\theta_{eq} = \frac{k_a P}{k_d + k_a P} \tag{2.22}$$

where k_a is the adsorption rate constant for unit pressure, k_d is the desorption rate constant, and P is the pressure [2.6]. Detail derivation is shown in Appendix I. Assuming the same field at the surface, changes in work function would result in changes in the barrier width x, hence it would result in large changes in emission current due to its exponential dependency as shown in Figure 2-6 (b).

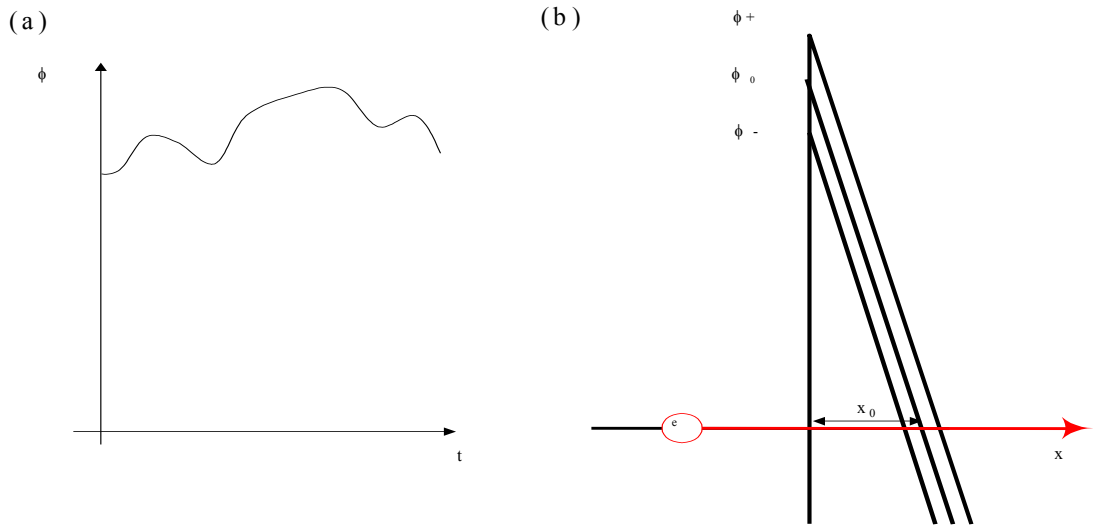


Figure 2-6. (a) Work function changes with time randomly. (b) Changes in work function result in changes in energy barrier width x.

How the work function changes the emission current can be expressed by the following equations by assuming emitter tip radius r is constant:

$$I = f(\phi) \tag{2.23}$$

$$\Delta I = \frac{\partial I}{\partial \phi} \times \Delta\phi \tag{2.24}$$

$$\frac{\Delta I}{I} = \frac{\partial I / \partial \phi}{I} \times \Delta\phi \tag{2.25}$$

$$I = \frac{\alpha A \beta^2}{1.1\phi} \exp\left[\frac{B\left(1.44 \times 10^{-7}\right)}{\phi^{1/2}}\right] V^2 \exp\left(-\frac{0.95 B \phi^{3/2}}{\beta \bullet V}\right) \tag{2.26}$$

$$\frac{\Delta I}{I} = \frac{\partial I / \partial \phi}{I} \times \Delta\phi = \left[\frac{-1}{\phi} - \frac{0.72 \times 10^{-7} B}{\phi^{3/2}} - \frac{1.425 \phi^{1/2} B}{\beta V}\right] \times \Delta\phi \tag{2.27}$$

Detail derivation is shown in Appendix H.

The solutions to the temporal instability are to (1) make very large array so that the emission current in the presence of the imperfect vacuum could be averaged out, or to (2) control the device with a current source. The first solution has been demonstrated and has achieved moderate success. The second solution is to use a current source to control

the field emission device so that the emission current would only be dependent on the current source and not the field emitter surface cleanness. This approach will be discussed in detail in the following section.

Low Voltage Control

In order to turn-on a field emission device, a high voltage is required to achieve very high field at the emitter apex. The higher field bends the vacuum level leading to a narrower energy barrier width, x, and hence electrons have higher probability to tunnel out. In comparison with most microelectronic devices, which can be switched on/off within less than 10 V, field emission devices require voltages of ~ 50 V, to be switched on. High voltage switch increases the power dissipation of the field emission device, especially when used in a display. In order to use low voltage to control the field emission devices, we can either (1) fabricate field emitters using low work function materials, (2) fabricate very sharp emitters, or (3) fabricate emitters with small gate apertures. The first approach would reduce the energy barrier height. In other words, we can use much lower applied voltage to achieve the same energy barrier width to have the same electron tunneling probability as shown in Figure 2-7 (a). This approach has had moderate success lowering operation voltage of field emission device. However, low work function materials are easily oxidized. When oxidized, the materials have high work function and change the emission properties. The second and third approaches would reduce the energy barrier width. If the same extraction voltage were applied to the field emission devices, the one with sharper emitters and smaller gate apertures would have much higher field at the tip apex and smaller energy barrier width as shown in Figure 2-7 (b). In other words, a much lower extraction voltage could be used to achieve the same energy barrier width with the same electron tunneling probability. This approach has also provided moderate success lowering operation voltage. There is one other method to achieve low voltage control: control the field emission device by a current source. Field emission consists of electron supply and transmission processes. The first three approaches modulate the electron transmission process, which has exponential dependence on work function width

and height. The forth approach is to modulate the electron supply. This approach will be discussed in detail in the next section.

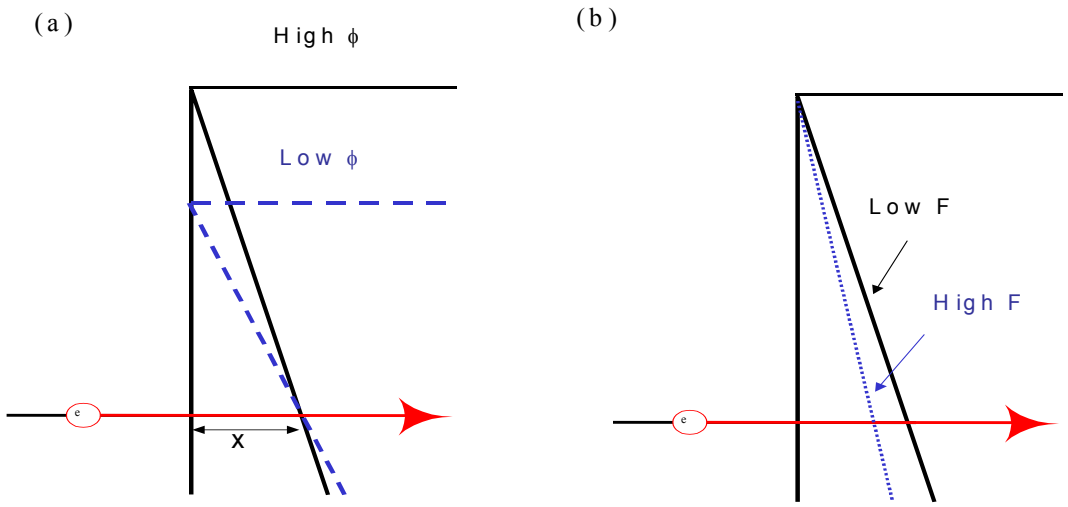


Figure 2-7. (a) Changes in work functions, and (b) Changes in applied fields to achieve low voltage control on field emission devices.

Summary of Approaches to Improve Field Emission Device Performance

We have discussed the sources of the less than optimal performance of the field emission devices. It is obvious that these imperfections in field emission devices emanate from the electron transmission process through the energy barrier. We also presented several possible solutions for all the imperfections. One potential solution that is common to all of the three imperfections mentioned in the previous sections is to control the field emission device by modulating the electron supply. Referring back to Section 2.1, we described the field emission process as consisting of two sequential processes -- electron supply to the emitter surface followed by electron transmission through the barrier. We can use either process to control the electron emission. If we use electron supply to modulate field emission while ensuring that the electron transmission is high, field

emission current is only determined by the electron supply. The imperfections generated from the electron transmission process would no longer be an issue.

This concept can be explained more clearly using the water flow analogy [2.17]. Figure 2-8 shows two water reservoirs, and there are two faucets between the reservoirs. The amount of water accumulating in the final reservoir depends on the tightness of the both faucets. If the first faucet is kept loose and the supply of the water is sufficient, the increase of the water in the second reservoir only depends on the tightness of the second faucet. When the second faucet is loose, the accumulation rate in the second reservoir is large, and when the second faucet is tight, the accumulation rate is small. On the other hand, if the second faucet is kept loose, the accumulation rate in the second reservoir only depends on the tightness of the first faucet. As long as the second faucet is kept looser than the first faucet, small changes in the tightness of the second faucet would not affect the amount of water accumulating in the second reservoir. The first faucet is like the electron supply control in the field emission process and the second faucet is like the electron transmission control. When the electron emission is controlled by the electron supply, as long as the transmission is high, small changes in the transmission would not affect the electron emission.

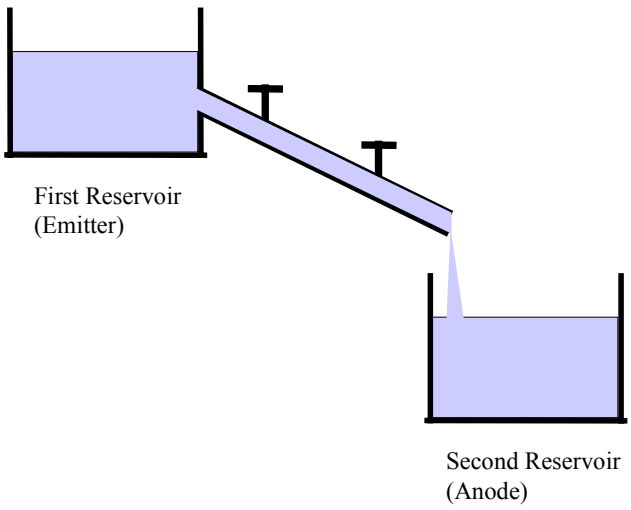


Figure 2-8. Water reservoir and faucet analogy [2.15].

How do we control the field emission by electron supply? As described in Section 2.1, we can fabricate the field emitter with semiconductor materials and alter doping or electrostatic field to modulate the electron supply. There have been several literature reports on controlling the field emission through electron supply, such as effective negative electron affinity (NEA) GaN cold cathode [2.15,2.16], and solid-state field controlled cathode [2.8]. In the effective NEA GaN cold cathode, the electrons are injected over a pn junction barrier followed by transmission through a NEA surface [2.16]. In the solid-state field controlled cathode, the electrons are injected over a Schottky barrier followed by transmission through a low electron affinity (LEA) or NEA surface [2.8]. The electron supply to the emission surface is controlled by the pn junction and Schottky barrier, respectively.

One of the approaches to modulate the electron supply is to use a voltage controlled current source. If a voltage controlled current source is put in series with field emitters, the supply of electrons to the emitter surface is controlled by the voltage controlled current source. Figure 2-9 shows the emission currents from a field emission device with spatial or temporal variation and a current source load line. The concept is the same as the traditional approach of using a ballast resistor to achieve uniform field emission as presented in Section 1-3. It is obvious that the differences in emission current due to either tip radius difference or gas absorption/desorption can be eliminated by the current source. Furthermore, the uniformity is much better than that could be achieved by a resistor. In this thesis, we use metal oxide semiconductor field effect transistor (MOSFET) as the voltage controlled current source for modulating the electron supply, hence, the field emission [2.17-2.21]. Other advantages of the integrating current source with the field emission device will be demonstrated in the later sections.

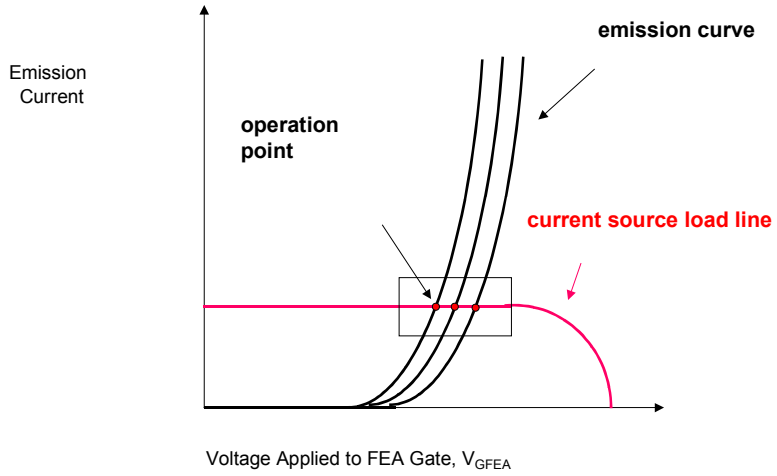


Figure 2-9. Current source accommodates the differences in emission current.

2.3 Theoretical Framework of MOSFET/Field Emission Device

In this thesis, we use MOSFET as a voltage controlled current source to modulate the field emission device with electron supply. This is realized by integrating the MOSFET device with the field emission device. Since the operation of the integrated MOSFET/field emission device depends on MOSFET properties, we will first briefly discuss how a MOSFET device works and compare the MOSFET device with the field emission device in this section. The operation of the integrated MOSFET/FEA device will later be discussed. We will next present how the sensitivity of the field emission device is changed with the inclusion of the MOSFET device.

Comparison of Semiconductor Microelectronics and Vacuum Microelectronics

MOSFET, a semiconductor microelectronic, is often used as a switch and amplifier. Figure 2-10 shows a typical MOSFET structure and Figure 2-11 shows the conduction

band energy as a function of position along the device channel of a MOSFET in both of the off and on states. Before voltage is applied to the MOSFET gate, there is a barrier between the source and channel with the magnitude of E_g (energy of band gap, ~ 1 V for silicon). A similar barrier exists between the channel and drain. The device is in the OFF state. When a voltage is applied to the MOSFET gate, the barrier is lowered. The semiconductor surface potential, ϕ_s, which is the barrier lowered by the gate voltage, is related to the gate voltage, V_{GS},

$$V_{GS} = \phi_s + \frac{\varepsilon_{silicon} x_{ox}}{\varepsilon_{ox}} \sqrt{\frac{2qN_A}{\varepsilon_{silicon}\varepsilon_0}\phi_s} \quad , \tag{2.28}$$

where $\varepsilon_{silicon}$ is the permittivity of the silicon, ε_{ox} is the permittivity of the silicon dioxide, x_{ox} is the gate oxide thickness, N_A is the channel doping concentration, q is the electron change, and ε_0 is the permittivity of free space. If a small voltage is also applied to the drain at the same time, this provides the driving force for electron transport from the source to the drain. Electrons are emitted over the source/channel barrier by thermionic emission. The device is now in the ON state [2.15]. The typical values for MOSFET gate voltage and the drain voltage for the ON state are both less than 5 V. In other words, we apply a small voltage on the gate, invert the channel while the source is grounded, and expect to have a large current to flow between source and the drain. A large current in the drain-source, "power loop", is generated in response to a much smaller applied signal in the gate-source, "control loop" as shown in Figure 2-12 [2.15].

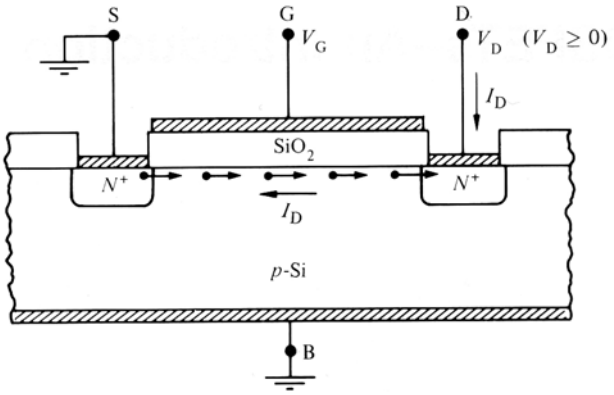


Figure 2-10. A typical MOSFET structure. G represents the gate, D is the drain, S is the source, and B is the back electrode of the MOSFET device [2.22].

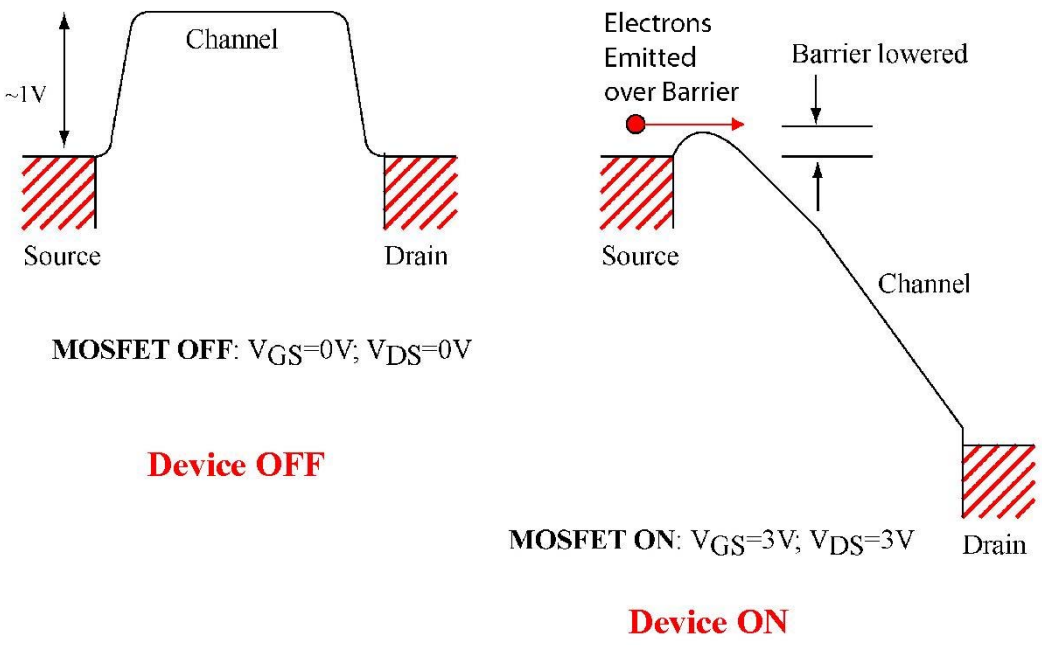


Figure 2-11. Energy band diagrams for a MOSFET device at OFF and ON states [2.15].

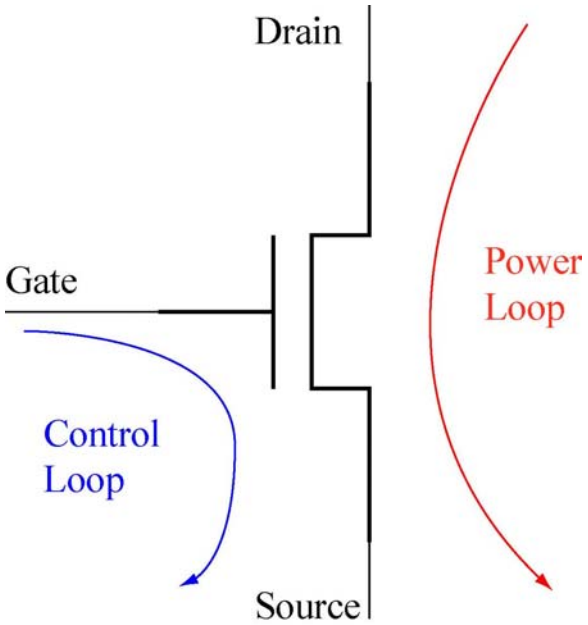


Figure 2-12. Equivalent circuit of a MOSFET device [2.15].

Field emission device, a vacuum microelectronics device, is often used as an electron source in amplifiers, displays, and switches. Figure 2-13 shows the energy band diagrams for the field emission device in both off and on states. The emitter in the field emission device is analogous to the source in the semiconductor devices. Same analogy applies to extraction gate as gate, anode as drain, and the vacuum channel as semiconductor channel. Before a voltage is applied to the extraction gate, there is a barrier between the silicon emitter and vacuum channel with the magnitude of electron infinity (χ) or work function, φ (~ 4.5 V for silicon). A similar barrier between the vacuum channel and anode exists. The device is in the OFF state. When a voltage is applied to the extraction gate, the barrier is narrowed, allowing electrons to tunnel out. If a voltage is applied to the anode at the same time, electrons that tunnel out of the emitter by field emission are collected by the anode. The device is now in the ON state [2.15]. The typical values for extraction gate voltage and anode voltage for the on state are 50 V and 1000 V, respectively. They are both much higher than the control voltage (the gate voltage) and the driving force (drain voltage) of the MOSFET. However, similar to semiconductor microelectronic devices, a large current in the "power loop" is generated in response to a much smaller applied signal in the "control loop" as shown in Figure 2-14 [2.15]. Here, the power loop is the anode-emitter segment and the control loop is the gate-emitter segment. While the fundamental device structure and transport mechanisms appear similar between semiconductor microelectronic devices and vacuum microelectronic devices, there are significant differences that account for the differences in operating voltages. The first one is the nature of the barrier between the electron reservoirs (source or emitter) and the conducting channel (semiconductor or vacuum). The barrier height is much higher in the vacuum microelectronic devices; hence it would require higher voltages at the controlling gate (extraction gate) to inject electrons from the reservoir (emitter) into the channel (vacuum) in comparison to these required for the semiconductor microelectronic devices. Next, because the barrier is very high for vacuum microelectronic devices, the mechanism for electron injection into the channel is tunneling because thermionic emission would be impractical. Thirdly, the distance between the injecting reservoir (emitter) and collecting reservoir (anode) is much larger than in a semiconductor microelectronic devices in which distance between injecting

reservoir (source) and collecting reservoir (drain) is defined by lithography. Since electron collection depends on the field est ablished, much larger anode voltages are required in the vacuum microelectronic devices to collect electrons.

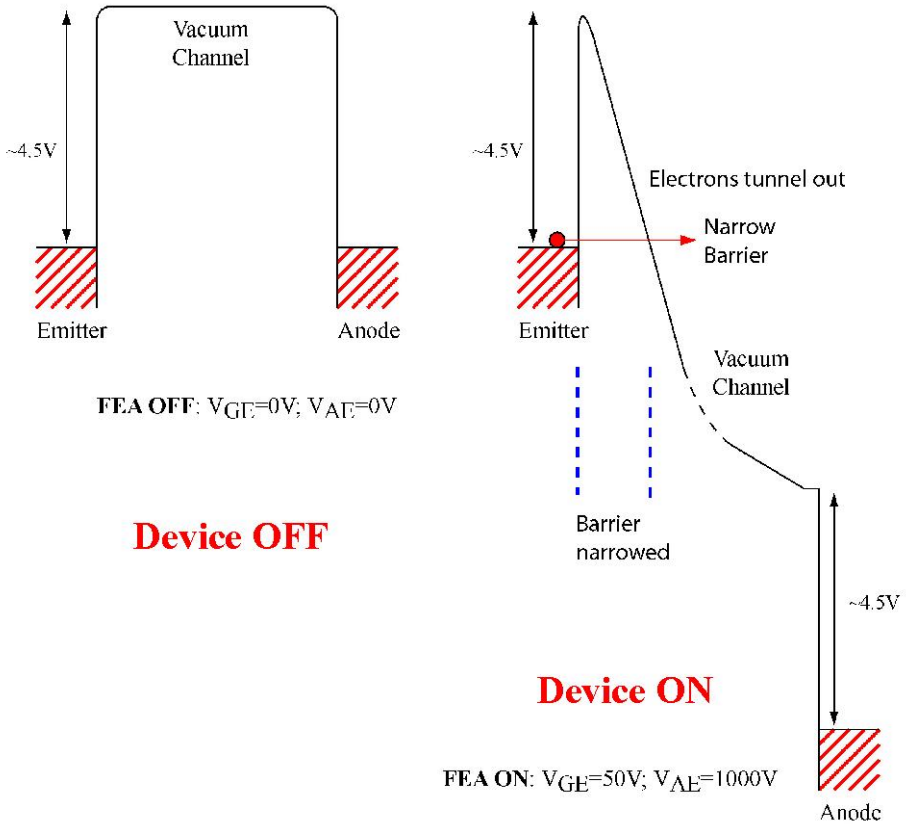


Figure 2-13. Energy band diagrams for a field emission device at OFF and ON states [2.15].

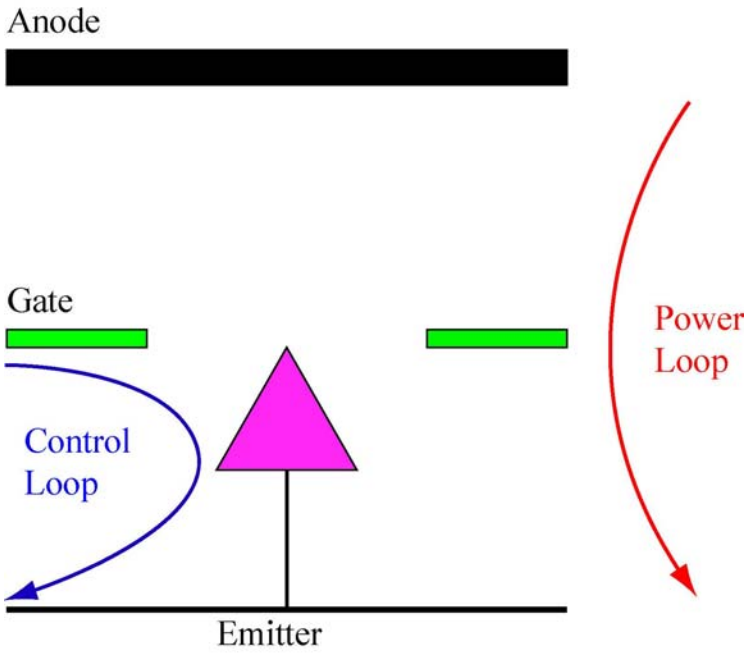


Figure 2-14. Similarity of a FEA device with a MOSFET device, shown in Figure 2-12 [2.15].

The device and performance comparison of semiconductor microelectronics and vacuum microelectronics is summarized in Table 2-1 [2.15]. In summary, semiconductor microelectronic devices could be described as having excellent input circuits because of the relative ease of injecting electrons into the channel. On the other hand, vacuum microelectronic devices could be described as having poor input circuits because of the high electron reservoir channel barrier height. It means current density and transconductance would be higher in a semiconductor microelectronics device. The vacuum microelectronic device could be described as having an excellent output circuit because of the ability to put high voltages on the anode. On the other hand, semiconductor microelectronic devices could be described as having poor output circuits because of the limitation on the collecting electrode voltage due to the proximity between source and drain.

Table 2-1. Comparison of the device and performance of the semiconductor microelectronics with vacuum microelectronics [2.15].

	MOSFET	FED
Channel	Semiconductor	Vacuum
Source/Channel Barrier	$\approx E_G$	$\approx \chi$ or ϕ
Electron Injection Mechanism	Thermionic Emission	Field Emission
Gate/Channel Coupling	Capacitive	Capacitive
Collector / Source Separation	Small	Large

	MOSFET	FED
Switching Voltage	<1 V	>20 V
Current Density	$10^4 - 10^5$ Acm^{-2}	$10^2 - 10^3$ Acm^{-2}
Transconductance	High	Low
Collector Voltage	< 5 V	>1000 V
Power Density	Very High	Moderate

	MOSFET	FED
Input Circuit	**Excellent**	**Relatively Poor**
Output Circuit	**Poor**	**Excellent**

We have described the operation of MOSFET devices and field emission arrays (FEA) separately. In this thesis, we would like to integrate these two devices and use MOSEFT to control the electron supply to the field emitter surface. In the integrated MOSFET/FEA device, the inversion layer formed in the MOSFET channel supplies a flux of electrons that is proportional to the MOSFET gate voltage to the field emission surface. Electrons tunnel out from the accumulation layer formed by surface band bending at the field emission surface while the MOSFET supplies electrons to replenish the electrons that have tunneled. The extraction gate voltage determines electron emission flux that depends on the transmission of the barrier, while the MOSFET gate voltage determines the electron supply. When the integrated MOSFET/FEA device is operated such that the electron emission is determined by the electron flux to the Fermi-sea, the device can be turned on and off by small changes in the MOSFET gate voltage. This is because the barrier between the source and the channel in a MOSFET is very small. In order to modulate the emission current by altering the electron supply, the electron transmission has to be high. In other words, in the integrated MOSFET/FEA device, the applied voltage on the FEA extraction gate should be kept high to ensure the high electron transmission probability. When the MOSFET is turned on, electrons flow out of MOSFET to the field emission surface, and are extracted by the high extraction gate voltage. When the MOSFET is turned off, even though the extraction gate voltage in the FEA may be high, there is no electron supply to the emitters and the integrated device is off. The operating mechanism of the integrated MOSFET/FEA will be presented in the next section.

By integrating the MOSFET with FEA device, we could not only achieve the goals of this thesis -- to obtain spatial uniformity, temporal stability and low operating voltage, we also benefit from other advantages from MOSFET devices.

Operating Mechanism of the Integrated MOSFET/FEA Device

The equivalent circuit of the integrated MOSFET/FEA device is shown in Figure 2-15 indicating that the field emitter and the MOSFET are in series. The drain of the MOSFET is floating and the value of the drain voltage is determined by the operating points of the devices. The voltage applied to the FEA extraction gate (V_{GFEA}) equals the sum of the voltage drop between the gate and emitter (V_{GE}) and the voltage drop across the MOSFET channel (V_{DS}). When the integrated device is on, an inversion layer is formed in the MOSFET channel, and electrons flow from source, though the MOSFET channel to the emitting surface. Then the electrons are extracted by the FEA gate and collected by the anode.

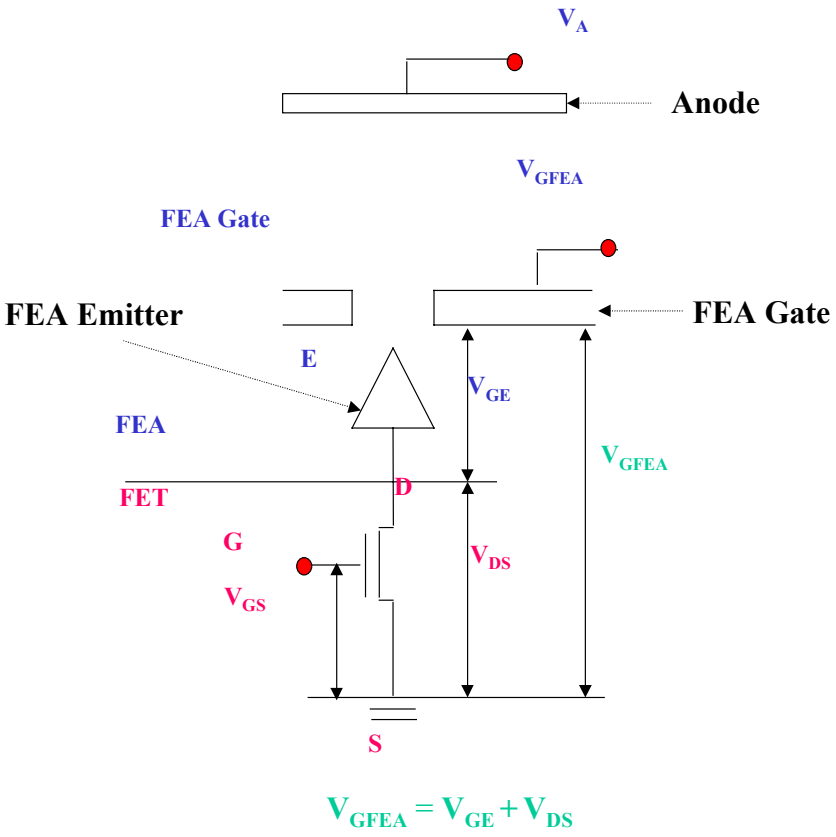
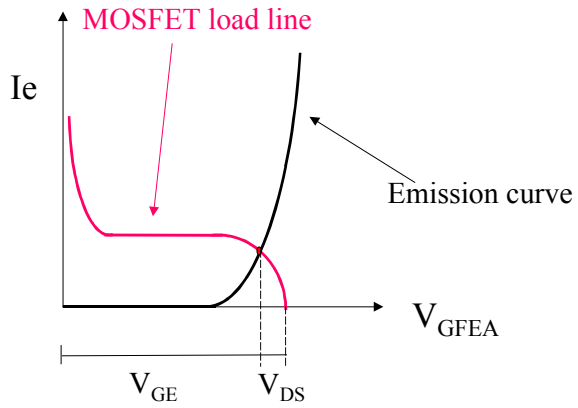


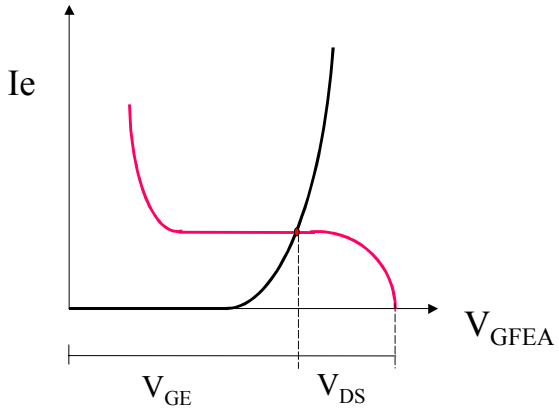
Figure 2-15. Equivalent circuit of an integrated MOSFET/FEA device.

The operation of the integrated MOSFET/FEA device can be described by the intersection of the emission curves of a FEA device and a MOSFET load line, as shown in Figures 2-16 (a), (b), and (c). The y-axis is the anode current and x-axis is the voltage between the FEA extraction gate and ground. When a relatively low voltage is applied to the FEA extraction gate, as illustrated in Figure 2-16 (a), the emission curve intersects the MOSFET load line in the MOSFET linear region. The voltage across the MOSFET channel ($V_{DS,}$) is smaller than the saturation voltage of the MOSFET (V_{DS_SAT}). As the applied FEA gate voltage increases, the MOSFET load line moves right while the emission curve stays unchanged. The intersection point (emission current) moves along the emission curve as the applied FEA gate voltage (V_{GFEA}) increases. The device is operating in the transmission (FEA) controlled regime. As the applied FEA extraction gate voltage increases further, the saturation region of the MOSFET load line intersects the emission curve, as shown in Figure 2-16 (b). Further increase of the applied voltage only increases the voltage across the MOSFET channel while the voltage across the field emitter remains constant. The intersection point (emission current) also remains the same even though the applied FEA extraction gate voltage (V_{GFEA}) is increasing. V_{DS} is larger than V_{DS_SAT} and the emission current saturates. The device is operating in the electron supply (MOSFET) controlled regime. Further increases in the applied gate voltage results in the breakdown of the MOSFET. In the breakdown regime, shown in Figure 2-16 (c), V_{DS} is larger than the MOSFET breakdown voltage and this leads to the breakdown of the integrated device. The intersection point (emission current) moves along with the emission curve again as the applied FEA gate voltage increases. Emission current is not controlled by MOSFET in this regime. Avalanche multiplication increases the electron density rapidly in the MOSFET channel. Hence, the electron supply is high and the emission is again controlled by the transmission.

(A)


MOSFET load line
Ie
Emission curve
V_{GFEA}
V_{GE}
V_{DS}

(B)


Ie
V_{GFEA}
V_{GE}
V_{DS}

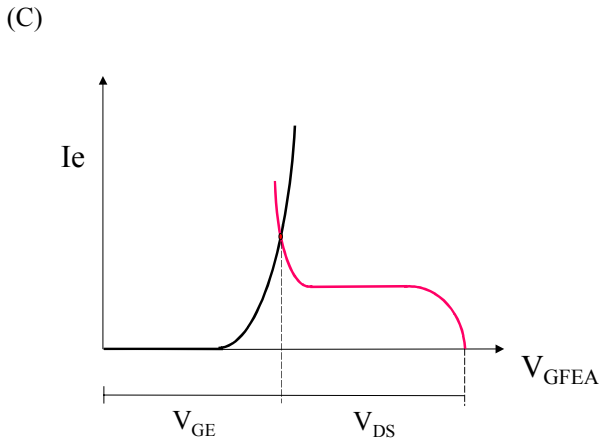


Figure 2-16. Operating mechanisms of an integrated MOSFET/FEA device. (a) The transmission (FEA) controlled regime. (b) The electron supply (MOSFET) controlled regime. (c) The breakdown regime.

In this thesis, we would like to have the integrated MOSFET/FEA device operating in the electron supply (MOSFET) regime. The device behavior of the integrated MOSFET/FEA device in the transmission (FEA) controlled regime is similar to the FEA only device and the integrated device could have all the imperfections as we mentioned in Section 2-2. We will also try to avoid the breakdown regime by increasing the breakdown voltage of the MOSFET device.

Device Simulation from *MATLAB*

The device was simulated using *MATLAB* to obtain the emission current versus extraction gate voltage relationship in the integrated MOSFET/FEA device. At the operating point of the integrated device, the emission current of the FEA equals the drain current of the MOSFET. Moreover, the voltage applied to the FEA extraction gate (V_{GFEA}) is the sum of the voltage across the field emitter (V_{GE}) and the voltage across the MOSFET channel

(V_{DS}). V_{DS} can be solved numerically using the above two equations. By substituting for V_{DS}, the emission current can also be obtained numerically. The simulation is done by solving these equations,

$$I_D = \mu_n C_{OX} \frac{W}{L}\left[(V_{GS} - V_T) \times V_{DS} - \frac{V_{DS}^{\ 2}}{2}\right] \qquad V_{DS} < V_{GS} - V_T$$

$$= \frac{1}{2}\mu_n C_{OX} \frac{W}{L}\left[V_{GS} - V_T\right]^2 \qquad V_{DS} > V_{GS} - V_T \qquad (2.29)$$

$$I_E = a_{FN} V_{GE}^{\ 2} \exp\left[\frac{-b_{FN}}{V_{GE}}\right], \qquad (2.30)$$

$$I_A = I_E = I_D, \qquad (2.31)$$

because

$$V_{GFEA} = V_{GE} + V_{DS}, \qquad (2.32)$$

by using ball-in-a-sphere model to obtain β, and

$$\alpha = \pi r^2, \qquad (2.33)$$

where r is the tip radius. The MOSFET we use in the simulation has the dimensions of 10 μm MOSFET width, 100 μm MOSEFT length with gate oxide thickness of 50 nm and substrate doping of 4×10^{17} cm^{-3}. The FEA has 10x10 emitters and the tip radius is 10 nm for all of the 100 emitters for simplification. Figure 2-17 shows the Fowler-Nordheim plot of the simulated result. The negative slope regime is the transmission (FEA) controlled regime, and the slightly positive slope regime is the electron supply (MOSFET) controlled regime.

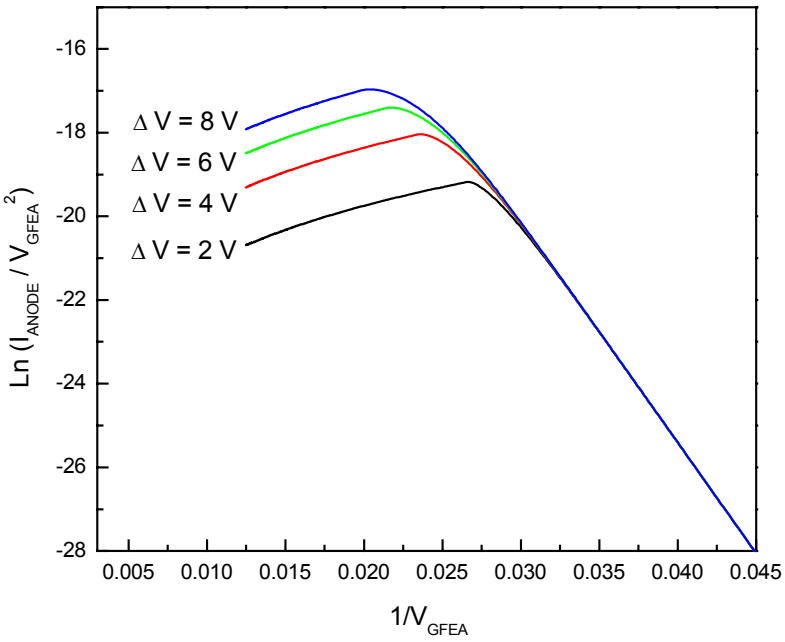


Figure 2-17. Simulated Fowler-Nordheim plot of an arbitrary integrated MOSFET/FEA device ($\Delta V=V_{GFET}-V_T$).

Sensitivity Reduction

When the field emission device is integrated with a current source, and the integrated device is operating in the saturation regime of the current source, this current source can accommodate the variation in emission current of the field emission device. In other words, the sensitivity of the field emission device to the environment is reduced due to the integration of the current source. We will discuss the sensitivity reduction in this section.

In a field emission device, as we discussed in Section 2.2, field emission current fluctuates with the changes of emitter work function and emitter tip radius by the following equations:

$$\frac{dI}{d\phi} = -\frac{\left[\frac{1}{\phi} + \frac{1.44\times10^{-7}B}{2\phi^{3/2}} + \frac{3}{2}\bullet\frac{0.95B\phi^{1/2}}{\beta V}\right]}{\frac{1}{I}} \tag{2.34}$$

$$\frac{dI}{dr} = -\frac{\left[\frac{2}{r} + \frac{0.95B\phi^{3/2}}{V}\right]}{\frac{1}{I}} \tag{2.35}$$

We start the sensitivity reduction analysis of a field emission device integrated with a resistor. The integration of the resistor with the field emission device is the most common approach to reduce the sensitivity to the work function changes and tip radius variation. It results in enhanced field emission device performance. The equivalent circuit of the feed back resistor approach is shown in Figure 2-18.

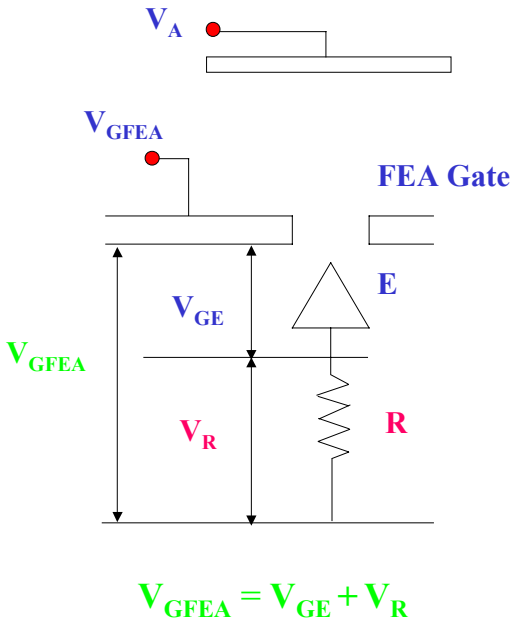


Figure 2-18. Equivalent circuit of a FEA device with a ballast resistor.

The applied voltage on the FEA extraction gate (V_{GFEA}) equals to the voltage across the field emitter (V_{GE}) and the resistor (V_R).

$$V_{GFEA} = V_{GE} + V_R . \tag{2.36}$$

Since the resistor and field emitter are in series, the current flows through both of them must be the same.

$$I_R = \frac{V_R}{R} = \frac{V_{GFEA} - V_{GE}}{R}, \tag{2.37}$$

$$I_E = \frac{\alpha A \beta^2}{1.1\phi} \exp\left[\frac{B\left(1.44\times10^{-7}\right)}{\phi^{1/2}}\right] V_{GE}{}^2 \exp\left(-\frac{0.95B\phi^{3/2}}{\beta V_{GE}}\right), \tag{2.38}$$

$$I_{FEA} = I_R = I_E, \tag{2.39}$$

where R is the resistance of the resistor, I_R is the current flow through the resistor, I_E is the current flow through the emitter, and I_{FEA} is the emission current collected by the anode. The emission current equation can be reconstructed as

$$I_E = \frac{\alpha A \beta^2}{1.1\phi} \exp\left[\frac{B\left(1.44\times10^{-7}\right)}{\phi^{1/2}}\right] \left(V_{GFEA} - I_E R\right)^2 \exp\left[-\frac{0.95B\phi^{3/2}}{\beta\left(V_{GFEA} - I_E R\right)}\right] \tag{2.40}$$

Emission current response to work function and tip radius changes can be obtained by the differentiation of emission current,

$$\frac{dI}{d\phi} = -\frac{\left[\frac{1}{\phi} + \frac{1.44\times10^{-7} B}{2\phi^{3/2}} + \frac{3}{2} \bullet \frac{0.95B\phi^{1/2}}{\beta\left(V - IR\right)}\right]}{\left[\frac{1}{I} + \frac{2R}{\left(V - IR\right)} + \frac{0.95B}{\beta} \bullet \frac{\phi^{3/2} R}{\left(V - IR\right)^2}\right]} \tag{2.41}$$

$$\frac{dI}{dr} = -\frac{\left[\frac{2}{r} + \frac{0.95B\phi^{3/2}}{\left(V - IR\right)}\right]}{\left[\frac{1}{I} + \frac{2R}{\left(V - IR\right)} + \frac{0.95Br\phi^{3/2} R}{\left(V - IR\right)^2}\right]} \tag{2.42}$$

Detail derivation can be found in Appendix H.

$\frac{dI}{d\phi}$ and $\frac{dI}{dr}$ can be reconstructed as following equations when substituting 1/I.

$$\frac{dI}{d\phi} = -\frac{\left[k_1(V-IR)+k_2\right]}{\left[\frac{\exp\left[\frac{0.95B\phi^{3/2}}{\beta(V-IR)}\right]}{k_0(V-IR)} + 2R + \frac{0.95B}{\beta}\bullet\frac{\phi^{3/2}R}{(V-IR)}\right]} \tag{2.43}$$

$$\frac{dI}{dr} = -\frac{\left[k_3(V-IR)+k_4\right]}{\left[\frac{\exp\left[\frac{0.95B\phi^{3/2}}{\beta(V-IR)}\right]}{k_0(V-IR)} + 2R + \frac{0.95B}{\beta}\bullet\frac{\phi^{3/2}R}{(V-IR)}\right]} \tag{2.44}$$

where k_0-k_4 are constants. When R increases, $I \bullet R$ increases even though I decreases, and $V - IR$ decreases. The numerators of the above two equations decrease and the denominators increase. Therefore, both $\frac{dI}{d\phi}$ and $\frac{dI}{dr}$ decrease while R increases. To the limit, when $R \to 0$, the expression reduces to $\left(\frac{dI}{d\phi}\right)_{No\ \mathrm{Re}sistor}$ and $\left(\frac{dI}{dr}\right)_{No\ \mathrm{Re}sistor}$, and

$$\left(\frac{dI}{d\phi}\right)_{\mathrm{Re}sistor} \leq \left(\frac{dI}{d\phi}\right)_{No\ \mathrm{Re}sistor} \tag{2.45}$$

$$\left(\frac{dI}{dr}\right)_{\mathrm{Re}sistor} \leq \left(\frac{dI}{dr}\right)_{No\ \mathrm{Re}sistor} \tag{2.46}$$

The resistor can reduce the sensitivity to both the work function and curvature of tip radius. In our case, V is of the order of 50-100 V while ϕ is of the order of 4 V and r is of the order of 10 nm, we shall need very high resistance to make sure that $\left(\frac{dI}{d\phi}\right)_{\mathrm{Re}sistor}$ and $\left(\frac{dI}{dr}\right)_{\mathrm{Re}sistor}$ are not too high. When R is very large, the voltage drop across the resistor, $V_R = IR$, is also very large, $V - IR << 1$,

$$\frac{dI}{d\phi} \approx -(V-IR)\bullet\exp\left[-\frac{0.95B\phi^{3/2}}{\beta(V-IR)}\right] \tag{2.47}$$

$$\frac{dI}{dr} \approx -(V - IR) \bullet \exp\left[-\frac{0.95B\phi^{3/2}}{\beta(V - IR)} \right] \tag{2.48}$$

To the limit, $R \to \infty$ $\frac{dI}{d\phi} \to 0$ and $\frac{dI}{dr} \to 0$.

Integrating a voltage controlled current source with FEA can be viewed as adding a high dynamic resistance device in series with FEA. To be more precise, the current source is not only a high dynamic resistance but also provides current to FEA,

$$I_{current\_source} \approx I_0 + I_R = I_0 + \frac{V_R}{R} \tag{2.49}$$

$$I_{FEA} = I_{current\_source} = I_E \tag{2.50}$$

$$V_{GE} = V_{GFEA} - V_R = V_{GFEA} - I_R R \tag{2.51}$$

$$I_E = \frac{\alpha A \beta^2}{1.1\phi} \exp\left[\frac{B(1.44 \times 10^{-7})}{\phi^{1/2}} \right] (V_{GFEA} - I_R R)^2 \exp\left[-\frac{0.95B\phi^{3/2}}{\beta(V_{GFEA} - I_R R)} \right], \tag{2.52}$$

Therefore,

$$I_E = \frac{\alpha A \beta^2}{1.1\phi} \exp\left[\frac{B(1.44 \times 10^{-7})}{\phi^{1/2}} \right] (V_{GFEA} - (I_E - I_0)R)^2 \exp\left[-\frac{0.95B\phi^{3/2}}{\beta(V_{GFEA} - (I_E - I_0)R)} \right]. \tag{2.53}$$

We can use very similar derivation for the resistor and obtain

$$\frac{dI}{d\phi} = -\frac{\left[\frac{1}{\phi} + \frac{1.44 \times 10^{-7} B}{2\phi^{3/2}} + \frac{3}{2} \bullet \frac{0.95B\phi^{1/2}}{\beta(V - (I_E - I_0)R)} \right]}{\left[\frac{1}{I_E} + \frac{2R}{(V - (I_E - I_0)R)} + \frac{0.95B}{\beta} \bullet \frac{\phi^{3/2} R}{(V - (I_E - I_0)R)^2} \right]} \tag{2.54}$$

$$\frac{dI}{dr} = -\frac{\left[\frac{2}{r} + \frac{0.95B\phi^{3/2}}{(V - (I_E - I_0)R)} \right]}{\left[\frac{1}{I_E} + \frac{2R}{(V - (I_E - I_0)R)} + \frac{0.95Br\phi^{3/2} R}{(V - (I_E - I_0)R)^2} \right]} \tag{2.55}$$

We have similar conclusion as a resistor integrated with a FEA. Both $\frac{dI}{d\phi}$ and $\frac{dI}{dr}$ decrease as resistance increases. When R is large, $I_E \to I_0$. Typically, $1 < V-(I_E - I_0)R < 100$ and $V-(I_E - I_0)R$ changes with R very slowly, $\frac{1}{I_E} << \frac{0.95Br\phi^{3/2}R}{(V-(I_E - I_0)R)^2}$, $\frac{1}{I_E} << \frac{2 \bullet R}{V-(I_E - I_0)R}$ for very large R,

$$\frac{dI}{d\phi} \approx \frac{\left[\frac{1}{\phi} + \frac{1.44\times10^{-7}B}{2\phi^{3/2}} + \frac{3}{2} \bullet \frac{0.95B\phi^{1/2}}{\beta(V-(I_E - I_0)R)}\right]}{\left[\frac{2R}{(V-(I_E - I_0)R)} + \frac{0.95B}{\beta} \bullet \frac{\phi^{3/2}R}{(V-(I_E - I_0)R)^2}\right]} \approx \frac{k_1}{k_2R + k_3R} \approx \frac{1}{R} \qquad (2.56)$$

$$\frac{dI}{dr} \approx -\frac{\left[\frac{2}{r} + \frac{0.95B\phi^{3/2}}{(V-(I_E - I_0)R)}\right]}{\left[\frac{2R}{(V-(I_E - I_0)R)} + \frac{0.95Br\phi^{3/2}R}{(V-(I_E - I_0)R)^2}\right]} \approx \frac{k_4}{k_2R + k_3R} \approx \frac{1}{R} \qquad (2.57)$$

where k_1-k_4 are constants. To the limit, $R \to \infty$ $\frac{dI}{d\phi} \to 0$ and $\frac{dI}{dr} \to 0$.

It is summarized that when integrating a resistor with a FEA device, the larger resistance would result in more reduction of sensitivity. However, when there is a resistor and there is a voltage drop across the resistor, we expect the current to be lower as R increases. In other words, if there is resistor, for the same current through the field emitter, the voltage required for an FEA with a resistor is higher than the voltage required for an FEA without the resistor. Comparing a resistor with a current source when they are integrated with a FEA as shown in Figure 2-19, the resistor reduces the total emission current more than a current source with the same resistance. In other words, the voltage across a resistor is more than a current source with the same resistance. The sensitivity reduction is more efficient with a current source than a resistor without sacrificing the emission current magnitude.

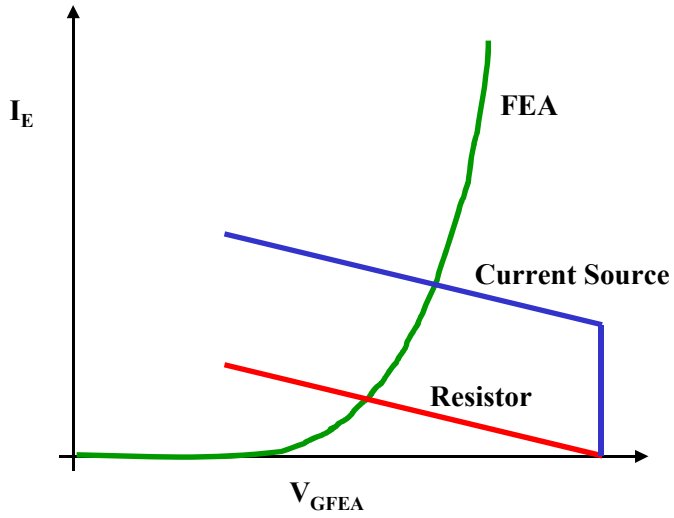


Figure 2-19. Comparison of a resistor with a current source. Both current source and resistor have the same resistance. Current source is simplified as $I = I_0 + I_R R$.

The sensitivity reduction discussed above is valid when the voltage applied to the FEA extraction gate is constant. Now, we discuss how the current source contains the variation with applied gate voltage assuming emitter work function and β are constant.

$$I = a_{FN} V^2 \exp\left[-\frac{b_{FN}}{V}\right], \tag{2.58}$$

$$\frac{dI}{dV} = \frac{\left[\frac{2}{(V-(I_E - I_0)R)} + \frac{b_{FN}}{(V-(I_E - I_0)R)^2}\right]}{\left[\frac{1}{I_E} + \frac{2 \bullet R}{(V-(I_E - I_0)R)} + \frac{R \bullet b_{FN}}{(V-(I_E - I_0)R)^2}\right]} \tag{2.59}$$

Detail derivation can be found in Appendix H.

For $R \to 0$, this expression reduces to FEA transconductance, i.e.

$$\frac{dI}{dV} \to I\left[\frac{2}{V} + \frac{b_{FN}}{V^2}\right] = \frac{I}{V}\left[2 + \frac{b_{FN}}{V}\right] \tag{2.60}$$

For $R \to \infty$, this expression reduces to current source conductance. Typically, $I_E \to I_0$, $1 < V - (I_E - I_0)R < 100$, and $\frac{1}{I_E} << \frac{R \bullet b_{FN}}{(V-(I_E-I_0)R)^2}$, $\frac{1}{I_E} << \frac{2 \bullet R}{V-(I_E-I_0)R}$ for very large R,

$$\frac{dI}{dV} \to \frac{\left[\frac{2}{(V-(I_E-I_0)R)} + \frac{b_{FN}}{(V-(I_E-I_0)R)^2}\right]}{\left[\frac{2 \bullet R}{(V-(I_E-I_0)R)} + \frac{R \bullet b_{FN}}{(V-(I_E-I_0)R)^2}\right]} = \frac{1}{R} \tag{2.61}$$

If we have a current source with high dynamic resistance, the transconductance is dominated by the current source conductance.

2.4 Chapter Summary

In this chapter, field emission theory was reviewed. We discussed the field emission device performance issues such as the non-uniformity and instability of the emission current, and high switching voltage. The conclusion is that these issues all emanate from the transmission part of the field emission process. Our approach to solve these problems is to add a voltage controlled current source to the field emission device. In this thesis, a MOSFET was chosen as the voltage controlled current source. After realizing the method to improve the performance of the field emission device, we presented a theoretical framework for the integrated MOSFET/FEA device operation. We presented the following: the device physics and a comparison of the operating principles of the MOSFET device, a semiconductor microelectronics device, with the FEA device, a vacuum microelectronics. Next, the operating mechanism of the integrated device was presented. Then, the integrated device behavior was simulated in *MATLAB*. We also presented an analysis of the sensitivity reduction when a resistor is in series with the FEA device and then proceeded to provide an analysis of the transistor in series with the FEA device.

3. Uniform and Sharp Silicon Field Emitters

In order to obtain emission current at a reasonable operating extraction gate voltage from a field emission device, a small radius emitter surface is desired. The emission current is an exponential function of the radius of curvature of the tip to the first order. The smaller the radius of curvature of the tip, the larger the emission current will be. In addition, a small change in the tip radius would result in large difference in emission current. Therefore, uniform and sharp emitters are essential to obtaining uniform and large emission current.

There are several methods to fabricate cone-shape structure field emitters. The Spindt approach is one of the most widely used approaches to fabricate sharp metal emitter arrays [3.1, 3.2]. Figure 3-1 illustrated the schematic of the Spindt approach [3.2]. The fabrication processes are described as follows: First, cavities are etched in the top two layers of a metal/dielectric/metal (or silicon) stack using resist patterning and wet or dry etching. Next, a sacrificial lift-off layer is deposited onto the top layer and inner walls of the upper portion of the cavity by grazing-angle deposition while rotating the substrate on an axis perpendicular to the surface. Then cones are formed in the cavities by depositing metal perpendicular to the substrate surface. The grazing-angle deposition can be used continuously or intermittently during this step to help control the hole-closure rate. Finally, lift-off is done by a wet etch of the lift-off material with a solvent that etches only the lift-off material.

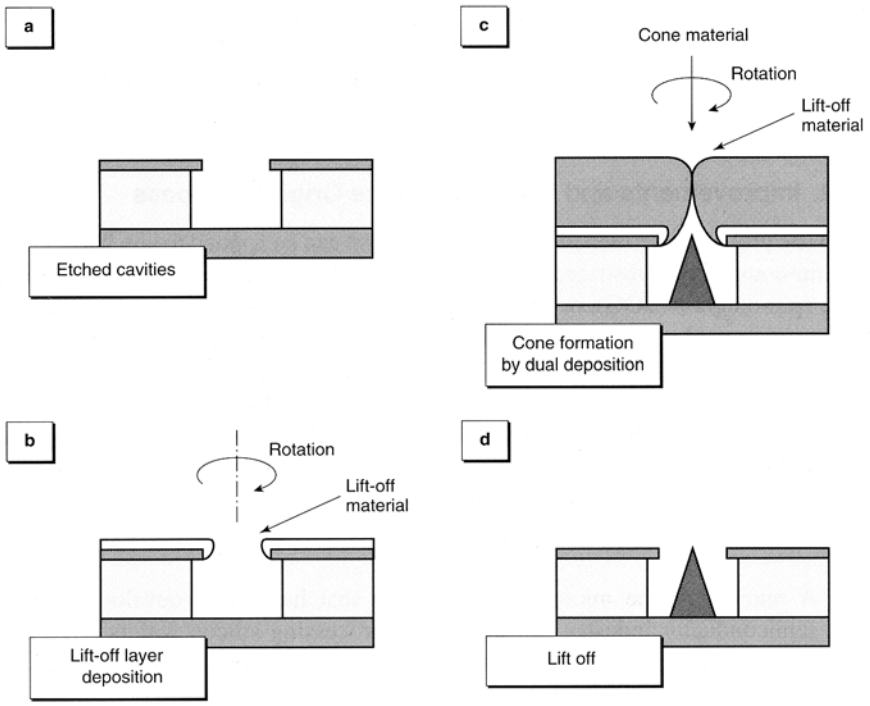


Figure 3-1. Schematic of the Spindt approach. [3.1]

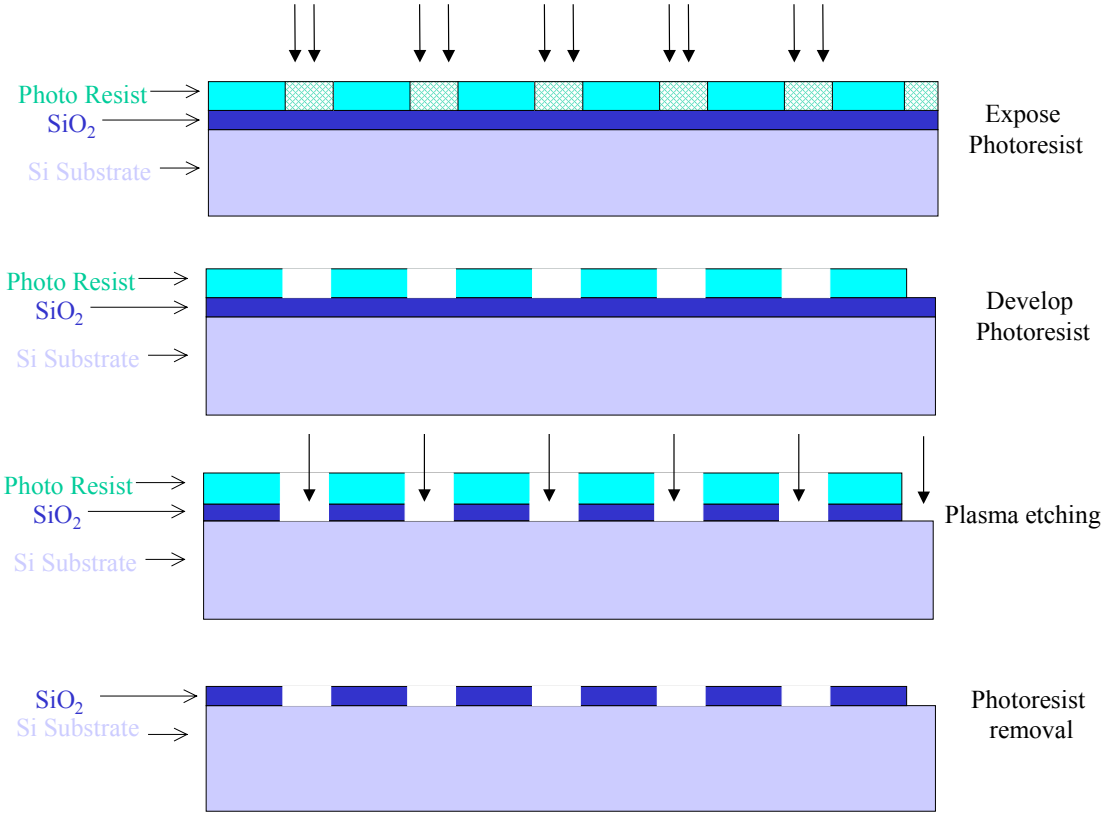
One other widely used approach is to fabricate silicon field emitter arrays using silicon etch and oxidation sharpening [3.3-3.6]. This is feasible due to the material properties of silicon and the well-developed silicon fabrication techniques and equipment. Silicon field emitter array fabrication processes are briefly described as follows: First, the masking dots, usually oxide dots, are defined on the silicon substrate. Next, the cone shape of silicon is formed under the mask by plasma isotropic etching. Then, the silicon cone is sharpened by thermal oxidation. Finally, the silicon sharp emitters are exposed by removing the covered oxide.

In this thesis, in order to simply the process for integrating the MOSFET devices with FEA devices, we make the devices on a silicon wafer. The second approach of fabricating sharp silicon emitters is used in this thesis. Well-controlled emitter formation process is extremely important because the non-uniform tips will result in the unreliable and uncontrollable results. Therefore, we will focus on how to fabricate uniform sharp silicon emitter in this chapter. We will discuss the process flow in detail using process

simulation [3.7]. We will especially discuss the three-dimensional oxidation of silicon and the mechanism of the oxidation sharpening by extensive use of TEM.

3.1 Fabrication of Sharp Silicon Emitters

The process flow for the fabrication of sharp and uniform silicon emitters is summarized in Figure 3-2. The fabrication starts with p-type (100) 4-inch silicon wafers. The emitter arrays have different sizes: 1, 10x10, and 20x20. The pitch of the emitter tip-to-tip distance is 4 μm to have reasonable array density with small interference between the field emitter tips.



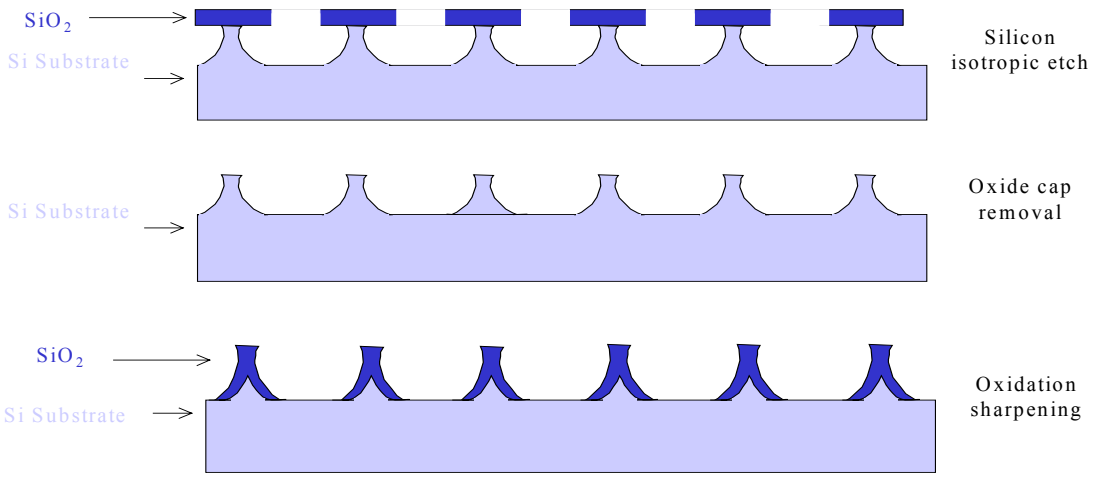


Figure 3-2. Process flow for fabricating sharp silicon emitters.

Photoresist Dot Definition

The first step of fabricating sharp silicon emitters is to define masking-dots on the silicon substrate. We used oxide disks as the hard mask for silicon etching. Here, the photoresist dots are used to define the oxide disks.

The wafers were first patterned by Array mask (Mask #1) and ion implanted with $2x10^{12}$/ $5x10^{12}$ cm^{-2} phosphorous at 180 KeV with 7 degree tilt [3.8]. The mask layout will be discussed in detail in Appendix B. The reason for this ion-implantation process is because p-type substrates were needed for NMOS and the field emitters have to be n-type to emit electrons without depletion (also used as a drain electrode in the integrated device). More details will be discussed in Chapter 4. The wafers were oxidized at 1000 ^{o}C for 30 minutes in a H_2O ambient to obtain an oxide layer with thickness of 250 nm, followed by a coat of 1.1 μm of photoresist [3.9]. The wafers were next exposed with Dot Mask (Mask #2) to define arrays of circular photoresist dots. The dots were defined

in the phosphorous doped well of the wafers. The photolithography steps were as follows: Hexamethyldisilazane (HMDS) vapor phase application – photoresist spin-coating – soft bake (115 ^{o}C, 1 minute) – exposure (in a 10x optical stepper) [3.10] – post exposure bake (115 ^{o}C, 1 minute) — develop – hard bake (130 ^{o}C, 1 minute). HMDS is widely used in the semiconductor industry to improve photoresist adhesion to silicon and to oxide [3.11]. Overexposure was employed in this process because overexposure of the photoresist leads to more uniform feature sizes across the wafer. On the other hand, it also shrinks the features depending on the overexpose condition. In order to have oxide disks with a diameter of 1 μm, the dot size on the mask was increased by 0.35 μm on a side according to several preliminary trial and errors. Post exposure bake at 115 ^{o}C was added in the standard photolithography step to reduce the effects of standing waves generated in the exposure step [3.12]. The standing wave would give the developed resist distinctly scalloped edges. This would be an issue in the smaller feature size patterns.

One monitor wafer completed with full photolithography process was examined in scanning electron microscope (SEM) with 5 KeV [3.13, 3.14]. The samples were coated with 5-10 nm Au/Pd to avoid charging effect in SEM. The ideal shape of the photoresist dots should be cylindrical with a height of 1.1 μm. However, Figure 3-3 (a) shows the cross-section image of a bell shape photoresist dot with a height much less than 1.1 μm. This might be due to the diffusion of the photoresist at high temperature in the baking steps of the photolithography process. However, one monitor wafer that did not have the hard bake also had the same bell shape as shown in Figure 3-3 (b). Therefore, the bell shape might come from the over-exposure or the post exposure bake before the develop process. The scalloped edge on the photoresist dots in both Figures 3-3 (a) and (b) shows that post-exposure bake did not fully eliminate the standing wave effect. Longer post-exposure time or higher post-exposure temperature is needed to reduce the effect but it would cause the further diffusion of the photoresist. The photoresist dot at the wafer center is 1.32 μm in diameter and 1.28 μm at the wafer edge. This 2.9% difference across the wafer is acceptable.

(a) (b)

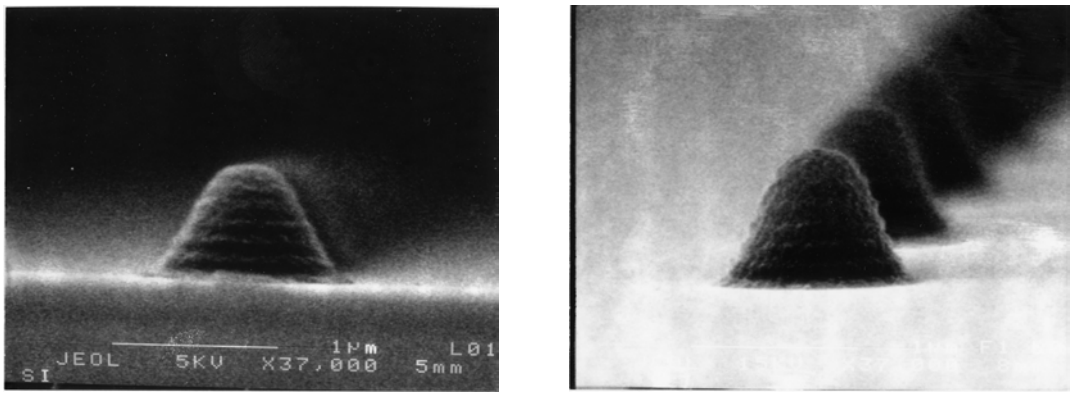


Figure 3-3. (a) Bell shape photoresist dots. (b) The shape has no difference without hard bake process.

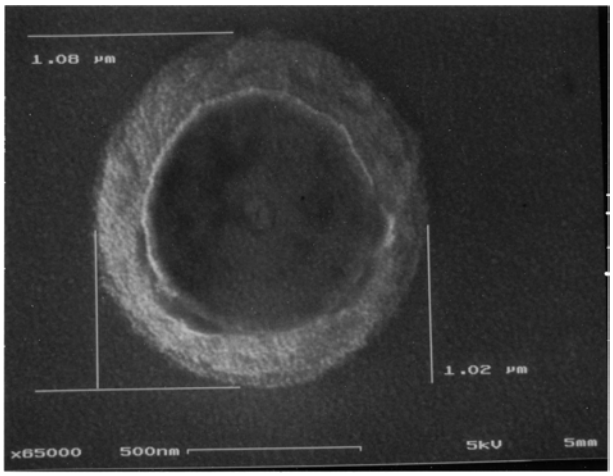
Oxide Dot Definition

Using these photoresist dots as etching masks, the silicon dioxide layer was anisotropically (directionally) etched in the plasma etcher [3.15] using two different recipes. Both recipes employed CF_4/CHF_3 but the gas condition of first recipe was 200 mT, 350 Watt and 12 mT, 250 Watt for the second recipe. The target oxide disk diameter was 1 μm. Oxygen was avoided in this process because oxygen would attack photoresist at the same time and result in sloped oxide feature. Chamber cleaning process was conducted before each oxide etching process to ensure the cleanness of the chamber because slight difference of gas mixture would change the oxide etching profile dramatically. After the oxide etching, the photoresist on the monitor wafers was etched away by the oxygen plasma stripper.

Two monitor wafers processed with the oxide etch recipes were examined in SEM. The samples were also coated with 5-10 nm Au/Pd to avoid charging effect. The cross-section images indicate the oxide sidewalls are sloped and the oxide patterns are not cylindrical. This is reasonable since the photoresist dots were sloped. However, the photoresist was severely attacked and resulted in larger slope in the first recipe. Hence, second recipe was used for our process. It is suspected that lower pressure and lower

power in the second recipe reduced the photoresist attack; therefore resulted in less sloped sidewalls. The oxide dot etched by the second recipe is 1.10 μm in diameter at the wafer center and is 1.16 μm at the wafer edge. It is a 5.5% difference across the wafer. Figure 3-4 (a) shows the plain-view of an oxide disk, the diameter is about 1.05 μm. The inner circle in the figure is the top of the oxide structure and the outer circle is the bottom of the oxide structure. Figure 3-4 (b) shows the cross-section of the oxide dot.

(a)



(b)

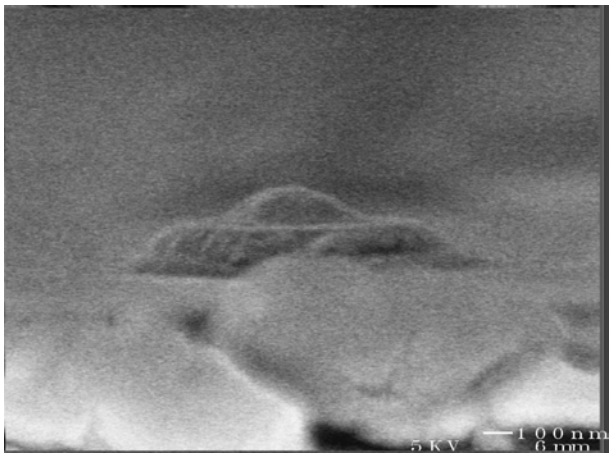


Figure 3-4. (a) Plain-view and (b) cross-section SEM images of an oxide dot.

Isotropic Silicon Etch

After uniform oxide dots were obtained, the wafers with oxide dots and remaining photoresist were loaded into oxide etch chamber for a 10% oxide over-etch. An over-etch process is necessary to clean the residual and native oxide on the silicon surface. Too much oxide over-etch would shrink the oxide dot feature because of the sloped sidewalls of the oxide dots and the photoresist dots. After over-etching, the wafers were sent to silicon etch chamber without breaking vacuum to avoid native oxide growth since silicon etch is very sensitive to the residual oxide. Using these oxide disks as hard masks, the underlying silicon was isotropically etched to form cones. The original silicon tip formation recipe was developed by Dr. Ham Kim in 1996 [3.16]. Currently, silicon etching is in a new plasma etch system, therefore, a thorough examination of the silicon etch process needs to be done. High pressure and low power of SF_6 gas was used for silicon isotropic etching. Several etching conditions were performed to obtain the most uniform silicon cone profile.

After several careful preliminary experiments, we decided to use the recipe with 175 mT, 100 Watt and 75 sccm of SF_6 to etch silicon isotropically. The vertical etch rate was 348.3 nm/min and the silicon surface remained smooth after etching. Figure 3-5 shows the silicon cone with oxide cap after silicon isotropic etch.

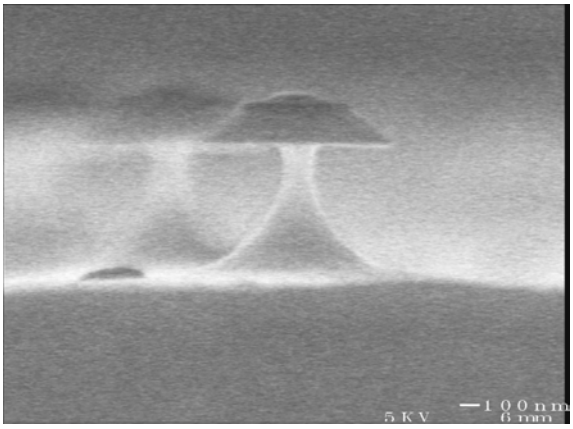
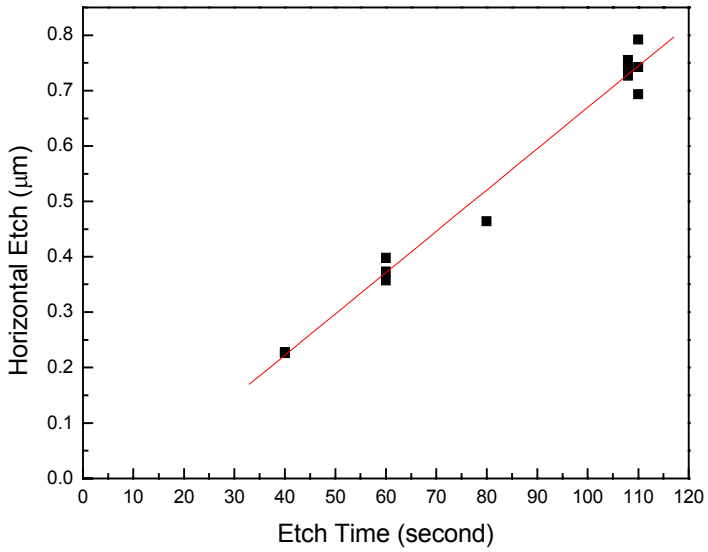


Figure 3-5. Silicon cone with oxide cap after silicon isotropic etch.

Silicon wafers were etched for different time periods to obtain the initiation time of the etching as shown in Figures 3-6 (a) and (b). The initial etch started from 10 and 5 seconds in horizontal and vertical etch, respectively. The etch ratio of horizontal to vertical etch is approximately 1:1.

(a)



(b)

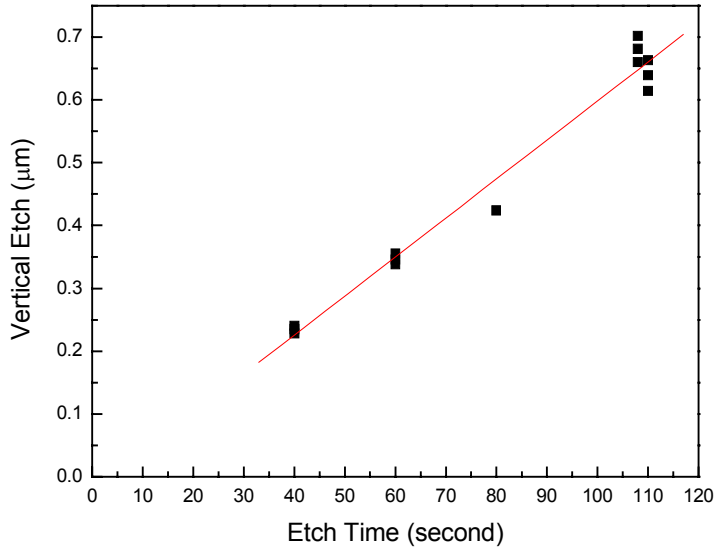


Figure 3-6. (a) Horizontal etching, and (b) Vertical etching as a function of time.

A target thickness for the neck of the silicon cone was ~ 100 nm. Further isotropic silicon etching would cause the oxide caps fall off and destroy the neck region of the silicon cone. However, the silicon cone height of ~ 0.5 μm after the isotropic silicon etch was insufficient. The short emitters would lead to thinner oxide insulator, which causes the large emitter gate leakage and early insulator breakdown. Anisotropic silicon etch was needed to increase the aspect ratio of the silicon emitter. An additional high-power (300 W) and low-pressure (30 mT) anisotropic silicon etching with Cl_2 and HBr gases was performed before oxidation sharpening and after isotropic silicon etching. Silicon tip height of ~ 1 μm was achieved. After the silicon etch step, the photoresist was etched away by the oxygen plasma stripper.

Oxidation Sharpening

The remaining oxide disks on top of the silicon cones were removed in buffered oxide etch (BOE) solution with HF: H_2O of 1:7 for 3 minutes. The thermal oxide etch rate in BOE is about 105 nm/min. The wafers were next oxidized to sharpen the tip area at 950 ^oC in 100% oxygen ambient for 15 hours. Oxidation sharpening is feasible for the tip formation process mainly due to the much slower oxide growth rate on the curved silicon surface [3.17]. This will be discussed in detail in Section 3.3. Dry oxidation was chosen due to its more severe retardation of curved silicon surface oxidation than wet oxidation. Oxidation at 950 ^oC was chosen because the oxide layer formed at or below this temperature is in the non-viscous oxide flow and the viscous stress would reduce the oxide growth rate of the curved silicon surface [3.17]. Oxidation at temperature lower than 950 ^oC would result in much longer oxidation time to achieve desired oxide thickness and tip sharpness. These oxidation temperatures and time periods were determined using process simulation. Figure 3-7 shows the process simulation result of silicon oxidized at 950 ^oC for 15 hours. The neck of the silicon cone is consumed in the oxidation process and a sharp silicon emitter is formed. Over-oxidation would result in short and blunt emitters. Silicon emitter features were examined by SEM and

transmission electron microscope (TEM) [3.18,3.19]. Figure 3-8 shows the SEM image of a sharpened silicon emitter after oxidation sharpening process and the oxide layer was removed by BOE. Details of the emitter tip radius will be presented in Section 3.2.

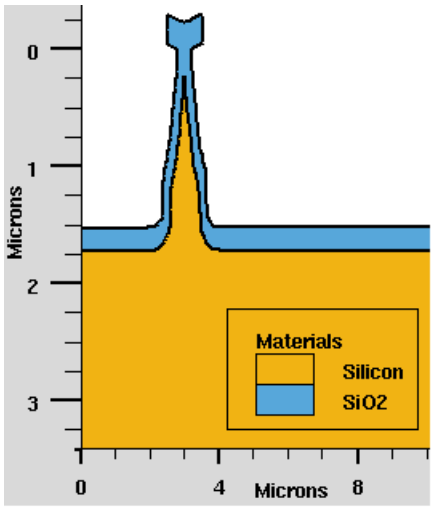


Figure 3-7. Simulation result of the oxidation sharpening process.

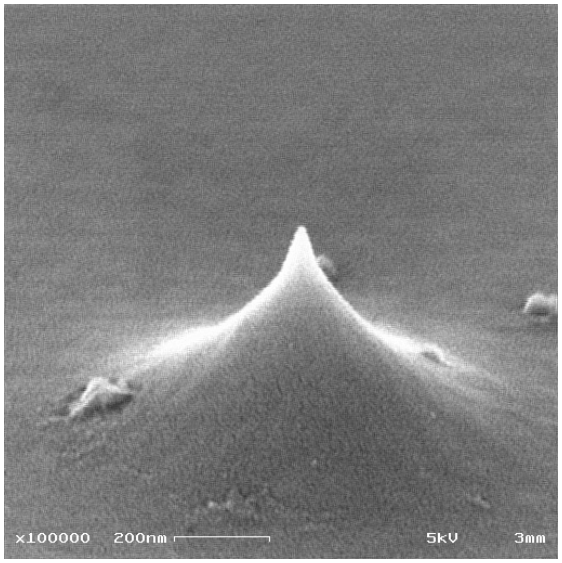


Figure 3-8. SEM image of a sharp silicon emitter after oxidation sharpening with oxide removal.

3.2 Structure Characterization

Tip radius of the sharp silicon emitter is a dominant parameter in the field emission process. The tip radius determines the electric field on the tip surface at an applied voltage and exponentially alters the emission current. Further studies of the structure of the sharp silicon emitters were conducted. TEM analysis of the tips were performed since it is capable of attaining 1 nm resolution with the uncertainty under ~0.8 nm. This is beyond the precision we need. Two sets of TEM images were taken. We will discuss the preparation and image-taking methods of these two sets of TEM images. The tip radius distribution will also be presented in this section.

TEM Sample Preparation

For the first set of images, samples were prepared using a standard TEM sample preparation. The silicon wafer piece with sharp emitters and a protection layer on top of the emitters was first glued with the other silicon wafer piece or a slide of glass by epoxy. The sharp emitters were inside the silicon/epoxy/silicon sandwich as shown in Figure 3-9. The sandwich structure was polished from two sides (parallel to the paper surface) until it reached less than 5 μm in thickness. This usually leaves only a row of the silicon emitters. Next, the sample was glued on to a copper grid, which provides better support to the fragile TEM sample. The length of the sample, which determines the numbers of the emitters that can be examined, is limited by the opening of the copper grid. It is about 1 mm in our case. The width of the sample has no significance for images taking because it is determined by the thickness of two silicon wafer pieces at the original sandwich structure. The sample was ion-milled until a hole is formed. The edge of the hole is extremely thin and is the best spot for TEM inspection. The TEM samples were prepared and imaged at Advanced Materials Engineering Research Inc. The images were taken in a JEOL 2010 TEM at 200 KeV. Due to the nature of this TEM sample preparation, all tips under investigation were within 1 mm^2. The first few emitters, usually less than 5

emitters, were imaged and then destroyed in ion-milling before the next few emitters were inspected. Less than 20 tips in total could be imaged in each sample preparation due to the array density in our design and it required continuous ion-milling in order to have very thin area.

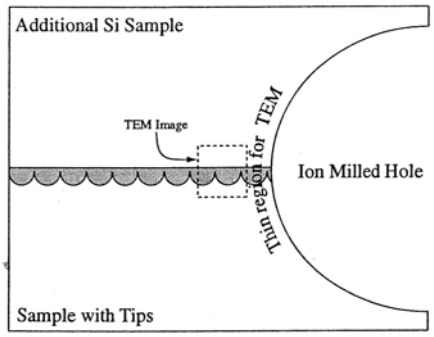


Figure 3-9. Sandwich structure of traditional TEM sample preparation [3.20].

The second set of images was taken using a sample holder that was designed to allow the mounting of a FEA array sample as shown in Figure 3-10 [3.20,3.21]. The sample was cut into a rectangular of 2 x 3 mm. The sample was mounted along the 3 mm edge. Since the holder was designed in a 70 degree tilted, the tip of emitter at the outer edge sticks out and can transmit electrons due to very small tip radius, usually around 10 nm. No further ion mill or polish was needed other than cutting and mounting the sample. Besides the short preparation time, the second technique allows a larger area to be sampled. In this technique, approximately 40 tips can be imaged each time. The yield of this technique is much higher than the first technique. The only concern is that we need to cut the sample carefully without touching/blunting the emitter tips. The images were taken in a JEOL 200 TEM at 200 KeV. Unfortunately, high-resolution images could not be obtained by JEOL 200 because the bulk holder could not be tilted into [110] direction, which is normal to the tip forming direction and the lattice image is not possible. If the holder were designed to be 90 degree the lattice image could be seen, but the images of the emitter tip would overlap. Even without the lattice image, this technique is still good for tip radius observation.

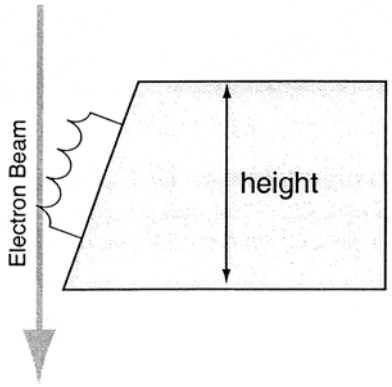


Figure 3-10. Sample mounting in the second TEM sample preparation [3.20].

Therefore, in this thesis, the traditional TEM preparation provides detail information about oxidation sharpening mechanism, which will be discussed in Section 3.3. High-resolution and larger magnification TEM images clearly show the interface of the silicon/oxide and the lattice images of silicon emitters. The second TEM preparation, which provides quick and large sampling, provides us the emitter tip radius distribution.

Tip Radius Distribution

The curvature of the tip apex can be represented by the smallest radius circle that coincides with the tip circumference. The radius of this fitting circle is the radius of curvature of the tip. Over 100 randomly sampled tips were examined using JEOL TEM 200. The tip radius distribution is shown in Figure 3-11. Similar to the tip distribution of Ding and Pflug's work [3.6,3.20], in which the emitters were fabricated in similar emitter fabrication processes in our lab, the tip radius shows log-normal distribution in the silicon emitters randomly sampled [3.22]. The tip radius ranges from 1.5 to 19 nm and the peak of the distribution is 6.2 nm with the width of 0.37 nm.

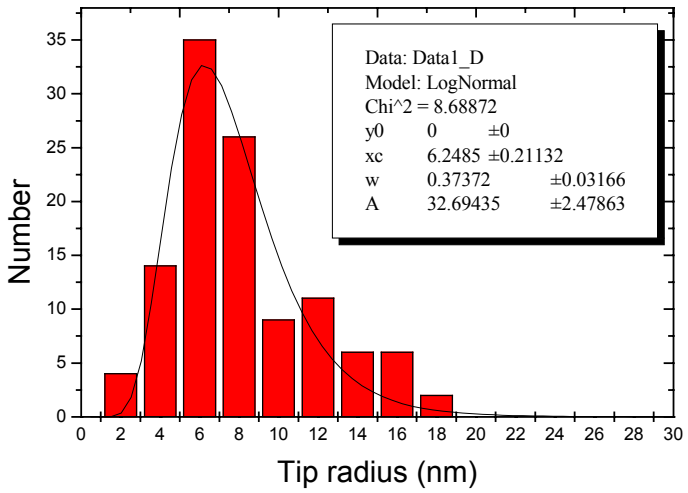


Figure 3-11. Tip radius distribution; peak of distribution r=6.2 nm, width of distribution=0.37 nm, average tip radius=7.6nm.

Even with very careful fabrication, we still have a log-normal distribution. The sources of this tip radius variation might come from the non-uniform performance of the fabrication tools employed to fabricate the emitters, such as photolithography, anisotropic oxide etching, and isotropic silicon etching. As we mentioned in Chapter 2, this would result in very large difference in emission current. We will discuss the details of emission current variation in Chapter 5.

3.3 Three-Dimensional Thermal Oxidation of Silicon-Oxidation Sharpening

Silicon oxidation mechanism first drew people's attention because of silicon dioxide's excellent properties for applications in silicon circuit technology. Silicon dioxide is chemically and thermally stable when it is in contact with silicon, which is the main material for the integrated circuit technology. There are several approaches to obtain silicon dioxide by either thermally growth or deposition. Thermally grown silicon dioxide has better adhesion to silicon and better dielectric properties compared with

deposited oxide. These excellent properties make thermally grown oxide a great candidate for gate oxide, protective layer, and insulator layer for integrated circuit devices. A better understanding of the silicon oxidation mechanism helps us better control the oxide growth. There have been many delicate studies on silicon oxidation mechanism especially in the planar silicon oxidation [3.23-3.25]. Two-dimensional silicon oxidation mechanism has also been studied due to its symmetry properties [3.17,3.26-3.28]. The objective of this project is to explore the three-dimensional thermal oxidation mechanism in the oxidation sharpening step for application to the formation of sharp silicon field emitter tips. Oxidation sharpening process was introduced to silicon field emitter tip fabrication because this process enhances the uniformity and sharpness of the emitter tips [3.29-3.33]. There is yet not much discussion on the three-dimensional thermal oxidation mechanism [3.34].

Silicon oxidation is a sensitive reaction process. Silicon dioxide is grown when the dry oxygen or water vapor is introduced to the silicon wafers at elevated temperature. Oxidation reaction occurs at the silicon/oxide interface. Once the oxide is formed on the silicon surface, oxygen molecules diffuse through the oxide layer and react with silicon atoms on the interface. The oxidation reaction is a strong function of silicon wafer orientation and weakly dependent on doping type and doping concentration. The key factors of oxidation are the oxidation temperatures and time durations.

The oxidation mechanism in the planar silicon wafer can be described as having two regimes. The first regime is the linear regime where the rate-limiting step is the interfacial reaction on the silicon/silicon dioxide interface. The second regime is the parabolic regime where the rate-limiting step is the diffusion of oxygen molecules across the grown oxide. When the second dimension is introduced, the stress builds up at the silicon surfaces with high curvature. This stress results in a suppression of interfacial reaction, hence, the oxidation rate slows down at the curved silicon surface. The stress configuration reduces the oxidation rate locally, probably through an increase in the energy barrier for the reaction [3.29-3.33]. The oxidation inhibition on the concave surface might also result from the lack of oxidizing species. Oxide thickness is therefore

a strong function of the radius of the curvature of the silicon surface: the smaller the radius is, the thinner the oxide grows. The retardation of oxidation is more pronounced at lower temperatures [3.17]. Oxide viscosity is high when the oxidation temperature is lower than around 965 ^{o}C. Above 965 ^{o}C, the oxide flows and relieves the stress buildup. The viscosity of dry oxides is estimated to be higher than that of wet oxides by 2 or 3 orders of magnitude [3.28].

Design of the Three-Dimension Oxidation Experiment

As the dimension of the silicon device decreases, the three-dimensional silicon oxidation mechanism becomes more important. The device can no longer be assumed to be one or two dimensions and all three dimensions should be taken into account. This is especially crucial to our silicon emitter fabrication process. We use this silicon oxidation sharpening technique to sharpen the silicon emitter tip and the sharpness of the emitter tip is the most important factor in field emission process. To further study the three-dimension silicon oxidation sharpening, a new set of experiments was designed. In these experiments, oxidation behavior of various sizes of silicon cones at different temperatures and oxidation time duration summarized in Table 3-1 will be investigated. The oxidation temperatures were selected such that the time duration was reasonable to achieve sharp silicon emitter. Oxidation at temperature lower than 900 ^{o}C would result in very long oxidation time and at temperature higher than 1000 ^{o}C would cause the diffusion tube to sag at the required time duration. The features on the mask were dots ranging from 1.5 μm to 2.5 μm in diameter and with the pitch of 4 μm (from dot center to next dot center). These patterns were transferred to oxide layer to form the oxide disks with diameter from 0.8 μm to 1.8 μm. This transfer ratio is due to the over-exposure of the photoresist as described in Section 3.1 to obtain uniform features across the wafer. Only dry oxidation was conducted in this set of experiments because this is what we used in our device process. Slower oxidation rate in dry oxidation should provide us much thinner oxide than wet oxidation, and wet oxidation is expected to have similar oxidation behavior.

Table 3-1. Oxidation conditions for three-dimensional oxidation study.

	900 ^{o}C	950 ^{o}C	1000 ^{o}C
5 hours		x	
10 hours	x	x	x
15 hours		x	

We used the same fabrication process as described in Section 3.1. The process started from 4-inch n-type (100) silicon wafers. N-type silicon wafers were chosen because in most of the silicon emitters reported in the literature were fabricated in n-type wafers. In our device wafers, the silicon emitters were fabricated on the n well of a p type wafer, which will be discussed in detail in Chapter 4. TEM and SEM were done at different process steps to explore the oxidation mechanism. Figures 3-12 and 3-13 show the SEM images of the photoresist dots and the oxide disks, respectively. Figure 3-14 (a)-(e) show the silicon cones before oxidation sharpening. After removing the oxide caps, the wafers were ready for oxidation experiments at different temperatures and time durations. A complete process simulation of this oxidation experiment is shown in Appendix D. The simulated oxide thickness in the flat region and the tip height will also be presented in Appendix D.

(a) (b)

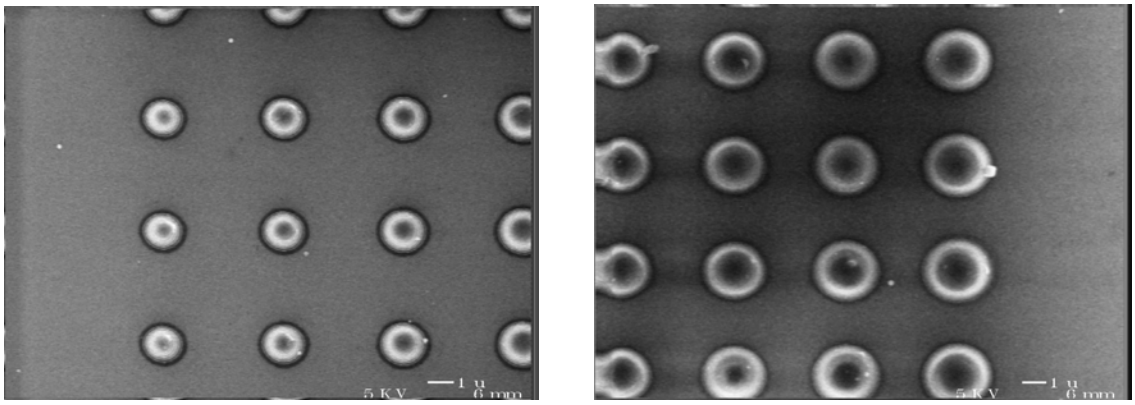


Figure 3-12. SEM images of the photoresist dots (a) Dots # 1-4. (b) Dots # 8-11. #1 is the smallest dot with a diameter of 1.5 μm and # 11 is the largest dot with a diameter of 2.5 μm.

(a) (b)

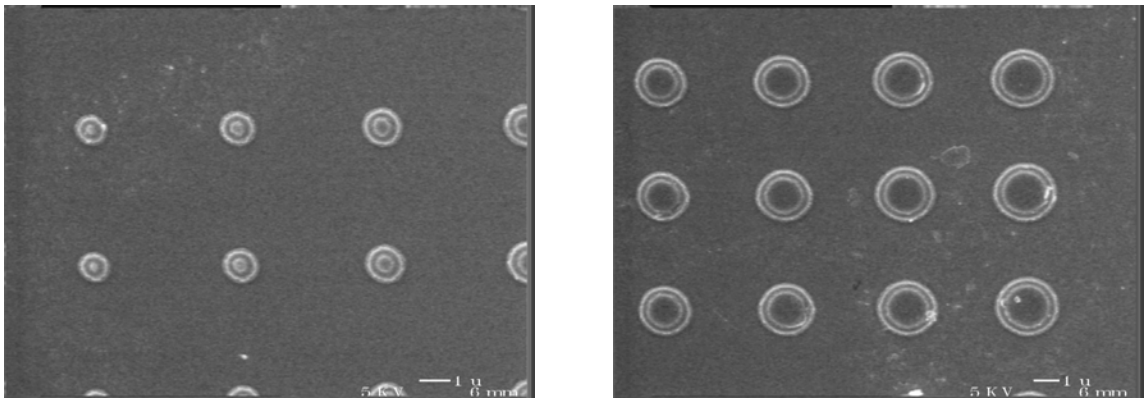
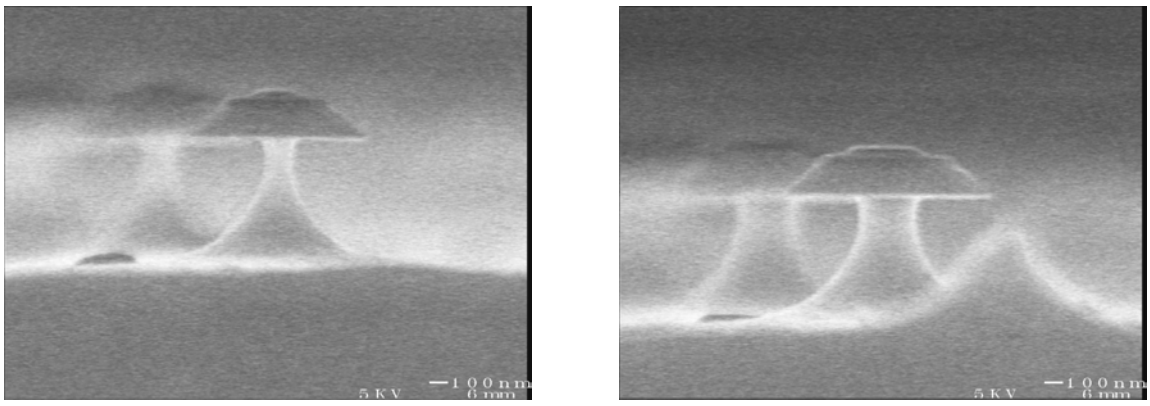
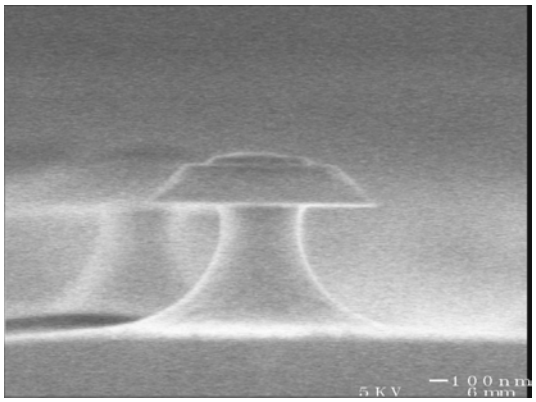


Figure 3-13. SEM images of the oxide disks (a) Dots # 1-4. (b) Dots # 8-11.

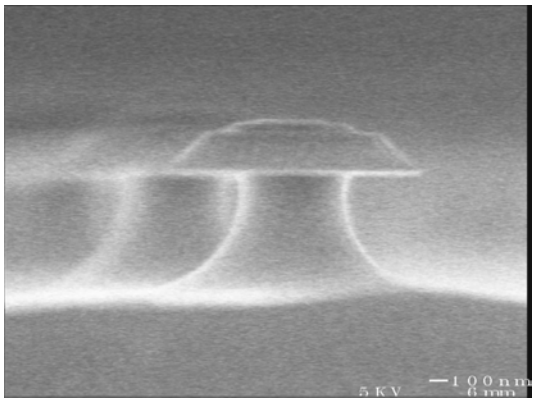
(a) (b)



(c)



(d)



(e)

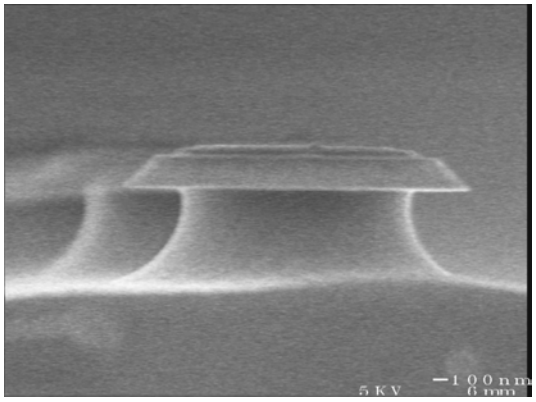


Figure 3-14. SEM images of silicon emitter cones before oxidation. The original oxide cap diameter is (a) 0.8 μm, (b) 0.9 μm, (c) 1.0 μm, (d) 1.1μm, and (e) 1.8 μm.

Results and Analysis

A. Oxide thickness at the flat area

The oxide thickness in the flat area away from the silicon emitter was measured by a spectroscopic ellipsometer (UV 1280). Table 3-2 summarizes the oxide thickness at different oxidation temperatures and time durations. Comparing Table 3-2 with Table D-2, the oxide thickness obtained from process simulation, the simulated results in flat area fit with the experiment data very well. The oxide is thicker at higher temperature and longer oxidation time as expected.

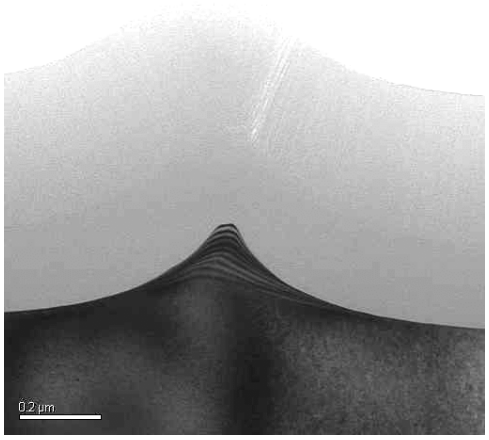
Table 3-2. Oxide thickness in different oxidation temperatures and time durations.

	900 ^{o}C	950 ^{o}C	1000 ^{o}C
5 hr		898.8 A	
10 hr	861.4 A	1449 A	2343.65 A
15 hr		1928.8 A	

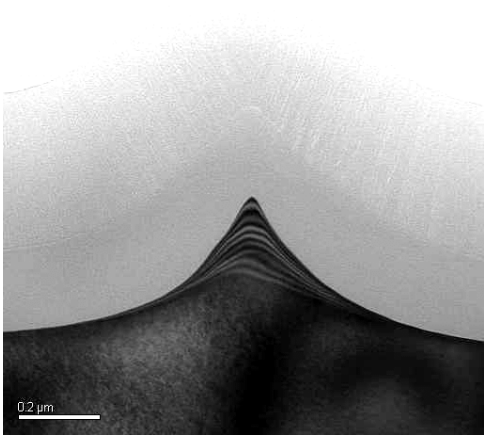
B. Oxidation study using TEM

TEM was used extensively to study the oxidation behavior. The oxide was kept on the silicon cones after oxidation sharpening and the first technique described in Section 3.2 was used to prepare the TEM samples. The electrons can transmit through both silicon dioxide and silicon if the sample is thinner than 10 μm, and the contrast between silicon and silicon dioxide is good enough to distinguish the layers because silicon is single crystal and silicon dioxide is amorphous. Figures 3-15 (a)-(k) show one complete set of TEM images of the silicon emitter features after oxidation in dry oxygen at 950 ^{o}C for 15 hours. TEM images under other oxidation conditions will be presented in Appendix E. The outmost layer of the features shown in the TEM images is the e-beam deposited 200 nm-amorphous silicon. This amorphous silicon layer serves as the protective layer during sample preparation because the tip region of the emitter is very fragile and the oxide could easily be damaged during polishing. We observed that part of the protective layers was polished away during the sample preparation. Fortunately, the oxide layers are well preserved in this set of the TEM images. Amorphous silicon provides sufficient contrast to silicon dioxide under TEM inspection even though both layers are amorphous. Other protective layers were also used for other sets of TEM sample preparation.

(a)



(b)



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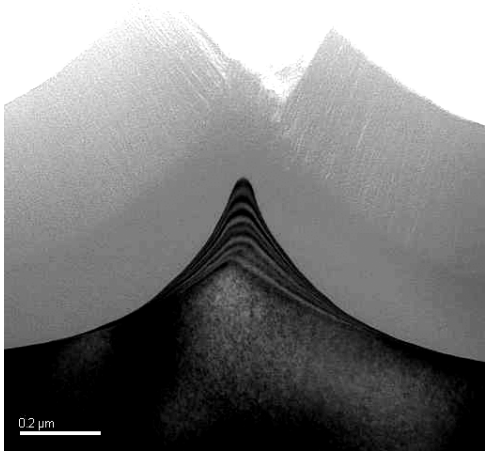

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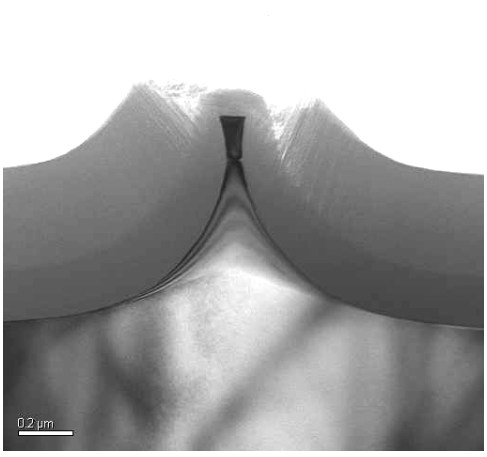
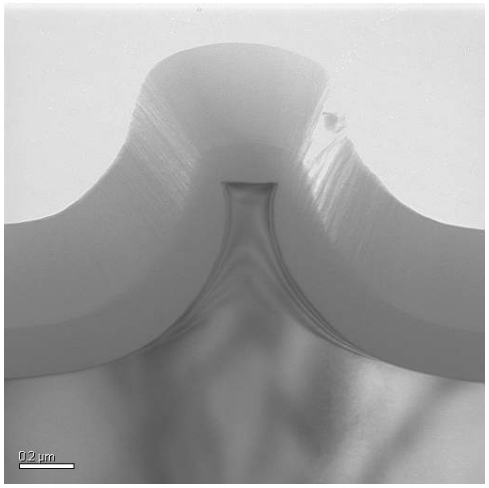


(e)



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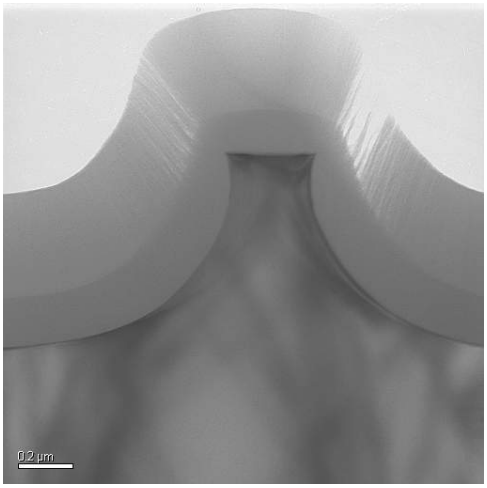
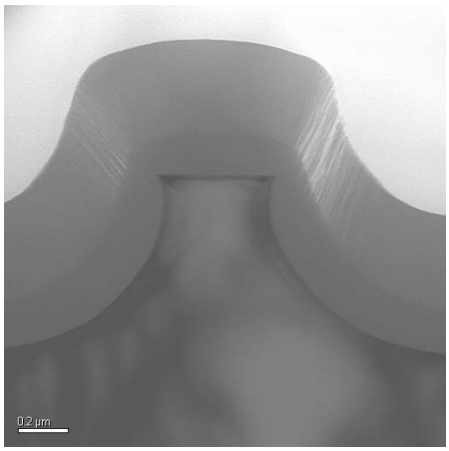
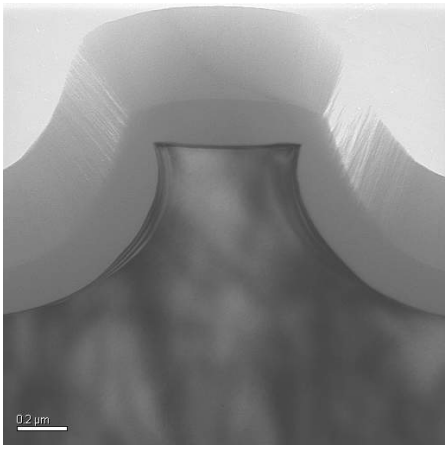


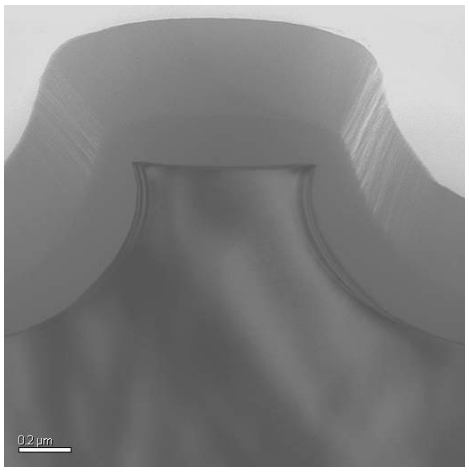
(g)



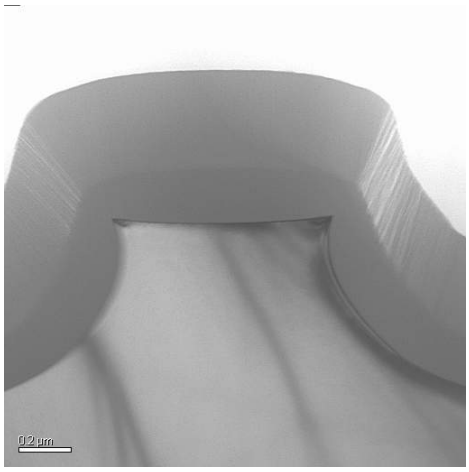
(h)



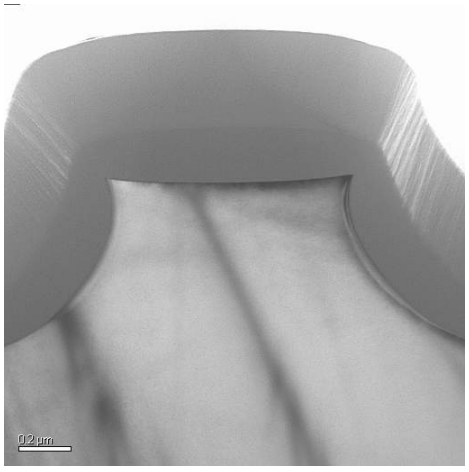
(i)



(j)



(k)



(l)

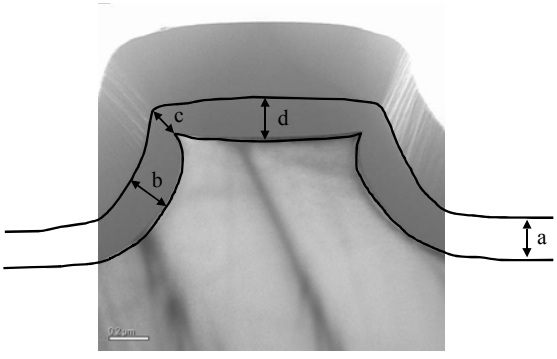


Figure 3-15. (a)-(k). TEM images of the silicon features with the thermal oxide on top. The features were oxidized in dry oxygen at 950 ^{o}C for 15 hours. The initial oxide cap sizes range from 0.8 μm to 1.8 μm in diameter. Figure 3-15 (l). Position labels.

C. Neck breaking and sharp tip formation mechanism

For the samples shown in Figures 3-15 (a)-(k), the diameters of the initial oxide cap sizes before silicon etching range from 0.8 μm to 1.8 μm in increment of 0.1 μm. The objective is to study the different oxidizing stages in the silicon emitter sharpening process. Small oxide disk would result in over-oxidized silicon tip neck and large oxide disk would result in under-oxidized silicon tip neck. Silicon tips are sharpened by oxidation as shown in Figure 3-15 (a)-(c) if the diameter of the original oxide cap equals or is smaller than 1 μm. It is usually believed that the silicon tip is sharpened in a continuous oxidation process -- As silicon is consumed during oxidation, the silicon/oxide interface at the neck region eventually merges and forms a sharp tip [3.29,3.30]. However, Figure 3-15 (d) shows that the silicon neck region breaks before the silicon/oxide interfaces could merge. It is suspected that the break of the silicon neck is due to the stress generated in the neck region. The stress built-up at the neck region forms the microcracks at the neck surface. Once the microcracks are formed at high temperature, oxidation would occur in these microcracks and result in faster oxidation in the (100) face, along the neck cross-section. Faster oxidation at this additional direction helps the separation of the neck and forms the sharp emitter. During the thermal oxidation process, the new oxide forms at the silicon/oxide interface. The volume of a silicon atom is 20$Å^3$ and the volume of an oxide molecule is 45 $Å^3$ [3.17,3.35,3.36]. The volume expansion of the oxide usually goes in the direction normal to the interface. The mismatch results in silicon dioxide compressive stress. However, the silicon at the silicon/oxide interface constrains the expansion of the silicon dioxide layer and the tensile stress results at the silicon neck. The stress is of the order of 10^9 dyn/cm^2. The exact value of the stress depends on the oxidation atmosphere, temperature, time duration, and the radius of the curvature on the silicon feature [3.28]. This tensile stress caused by volume difference is the one of the possible stresses that forms the microcracks at the neck surface during oxidation. One other possible source that may form the microcracks around the silicon neck is the cool-down stress. Oxidation is always carried out at a high

temperature and cool-down to room temperature results in a further increase in the stress because of the differences in the thermal expansion coefficient of silicon and silicon dioxide ($2.6x10^{-6}$/K and $5x10^{-7}$/K, respectively). Silicon has larger thermal expansion coefficient than silicon dioxide. Therefore, as the sample is cooled down to room temperature from elevated oxidation temperature, silicon shrinks faster than silicon dioxide. It results in tensile stress in silicon and compressive stress in silicon dioxide. This cool-down interfacial stress is about $2\text{-}4x10^{9}$ dyn/cm^2 [3.11]. This cool-down stress is about the same order as the volume difference stress, and both of the stresses could contribute to the initial silicon neck breaking. The volume difference stress occurs earlier than cool-down stress because the volume difference stress starts at high temperature once oxide is grown. From high-resolution TEM images of the neck region in silicon emitters shown in Figures 3-16 (a) and (b), oxide is formed around the neck area. This tells us that the initial formation of microcracks occurs at high temperature due to volume difference stress and oxide grows into the cracks right after the formation of the cracks. It is suspected that if the neck region is too thick for the volume difference stress to break the silicon bond, the combination of both volume difference stress and cool-down stress might be able to break the silicon neck at lower temperature. Since oxidation rate is very slow at lower temperature, micro-voids should be found around neck region. In the sharp emitter formation process, the microcracks formed by volume difference is more important because the neck needs to be further consumed by oxidation at high temperature.

(a) (b)

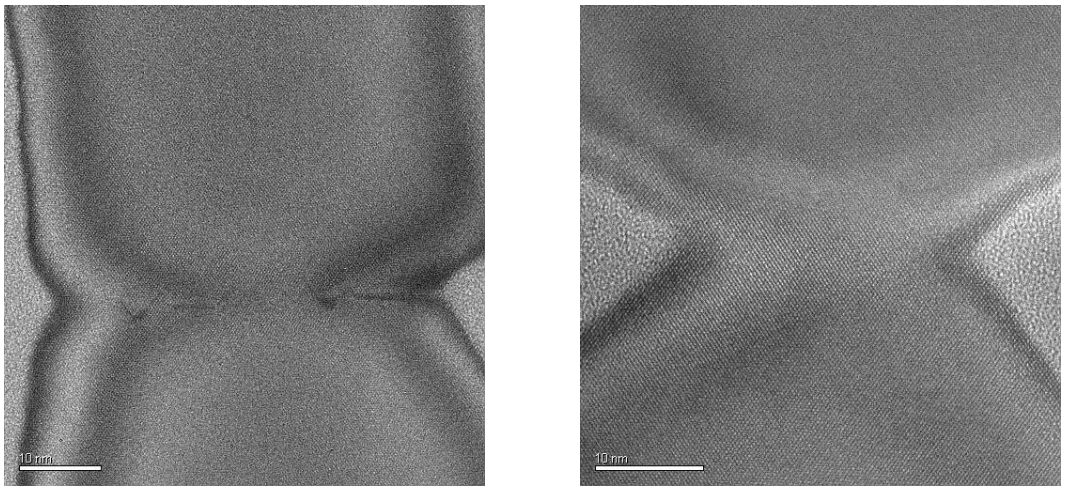


Figure 3-16. (a) High-resolution TEM image of the silicon feature in Figure 3-15 (d). (b) Silicon feature of the same size of oxide cap in a different array.

Figures 3-16 (a) and (b) show the high-resolution TEM images of the neck region in silicon emitters in two different arrays. The diameters of the original oxide caps of both silicon emitters are 1.1 μm. The small difference in the neck regions in Figures 3-16 (a) and (b) is due to the small non-uniformity in silicon neck width before the oxidation sharpening. The silicon emitter in Figure 3-16 (b) before oxidation has smaller neck width than that in Figure 3-16 (a). The tensile stress in silicon neck region creates the cracks -- the groves and the darker lines in the neck area in Figure 3-16 (a). The theoretical fracture strength ($\sigma_{bond\_strength}$) for silicon is about 28 GN/m^2 [3.37]. The microcracks at the neck surface starts to form when the neck width (the diameter of the neck area) is around 45 nm. Theoretically, this critical neck area with initial microcracks can be predicted by the force balance at the neck region:

$$\sigma_{TOTAL} \times A_{surface} = \sigma_{bond\_strength} \times A_{neck}, \tag{3.1}$$

$$\sigma_{TOTAL} = \sigma_{volume\_stress} \times \cos\theta, \tag{3.2}$$

If the microcracks occur at high temperature, which is what we observed,

$$A_{neck} = \pi r_{neck}^{2}, \tag{3.3}$$

where σ_{TOTAL} is the sum of tensile stress normal to the neck cross-session, $A_{surface}$ is the silicon post surface area, and A_{neck} is the neck cross-section area. σ_{volume_stress} is the tensile stress along the interface due to volume mismatch between Si and SiO_2, θ is the angle between the normal direction to the neck area and the Si/SiO_2 interface, and r_{neck} is the estimated radius of the neck area. The shape of the silicon feature is actually the combination of one big downside funnel and one small upside funnel. The total surface area can be simplified to approximately two conical frustums without the base area:

$$A_{surface} = \pi\left(r_{top} + r_{neck}\right)\sqrt{\left(r_{top} - r_{neck}\right)^2 + h_1^{\,2}} + \pi\left(r_{bottom} + r_{neck}\right)\sqrt{\left(r_{bottom} - r_{neck}\right)^2 + h_2^{\,2}} \quad [3.38], \qquad (3.4)$$

where r_{top} is the radius of the top of the silicon feature, r_{bottom} is the radius of the silicon feature base, h_1 is the height of the top conical frustum, and h_2 is the height of the bottom conical frustum. In our silicon feature,

$\theta = 5^o$,

$r_{top} = 50$ nm,

$r_{bottom} = 421.5$ nm,

$h_1 = 161$ nm,

$h_2 = 561$ nm.

By substituting the numbers, we obtain the estimated r_{neck} of 7.5 nm. Therefore, the estimated diameter of the neck (15 nm) is 1/3 of the actual diameter of the initial neck breaking (45 nm). If the silicon feature was not simplified to two conical frustum structures, the estimated diameter should be closer to the actual diameter of the neck breaking area. This earlier crack formation (the microcracks occur at the neck area larger than the expected) might be due to an imperfect crystal structure at the neck area either coming from the oxidation process or the surface tension created during the isotropic silicon etching before oxidation sharpening. Figure 3-17 (a) and (b) show the TEM images of the silicon neck region with the defects formed along the (111) direction. However, no fracture is observed along this (111) slip plane.

(a) (b)

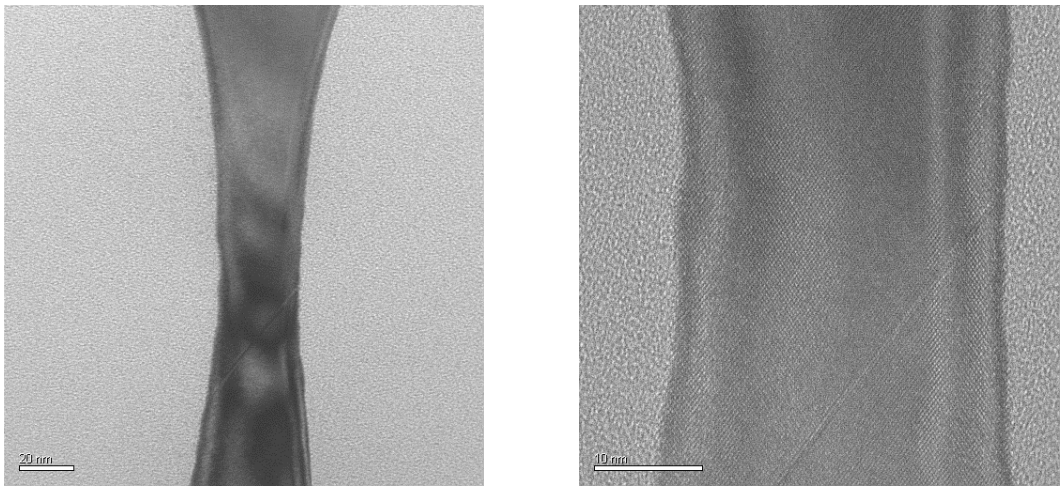


Figure 3-17. (a) TEM image of the defect along the (111) direction at the neck region. (b) The high-resolution TEM image of (a).

If we consider when the initial microcracks occur at low temperature,

$$\sigma_{TOTAL} = \left(\sigma_{volume\_stress} + \sigma_{thermal\_stress}\right) \times \cos\theta \,, \tag{3.5}$$

where $\sigma_{thermal\_stress}$ is the tensile stress along the interface due to thermal expansion difference between Si and SiO_2. The estimated diameter of the neck area is 21 nm. When the diameter is between 15 nm and 21 nm, only volume difference stress could not initialize the formation of microcracks. The neck breaking should start during cool down. However, when the diameter is larger than 21 nm, the silicon would not break without defects even at low temperature.

The neck breaking in the emitter formation process was not observed by other research groups due to two main reasons: (i) The neck breaking window is very small and it is difficult to be observed [3.4, 3.32]. (ii) If the silicon feature before oxidation sharpening has no neck area, the smallest silicon cross-section is at the topmost part of the silicon feature, there should be no neck breaking in oxidation sharpening and the oxidation is a self-limiting process [3.29-3.30].

After the formation of microcracks at the neck surface, a new silicon/oxide interface forms, and further oxidation would round up the newly formed interface. Silicon cone can be further sharpened by oxidation after the neck breaking stage due to the slow oxidation rate at the silicon feature with small radius of curvature. The neck region in Figure 3-16 (b) is concave with rather small radius of curvature. The slow oxide growth rate at the neck region would continuously sharpen the emitter until the silicon neck was fully separated by oxide, and the bottom part of the silicon cone formed the sharp silicon emitter. Further oxidation after the silicon neck is fully separated would be expected to form the sharpest silicon emitter tip. Figures 3-18 (a) and (b) show the high-resolution TEM images of the tip apex area in Figures 3-15 (b) and (c), respectively. The tip radii of both emitters are almost the same even though the emitter in Figure 3-18 (a) was a little over-oxidized compared with the one in Figure 3-18 (b). Right after the separation of the silicon neck, the sharp tip radius would result in lower oxidation rate at the tip apex than along the emitter sidewall due to the stress built-up at the tip apex; therefore, the sharpness of the tip can be sustained. The over-oxidation shortens the emitter without altering the tip radius much as shown in Figure 3-15 (b), where the emitter is shorter than the one in Figure 3-15 (c). Extensive over-oxidation would shorten and blunt the emitter at the same time as shown in Figure 3-15 (a).

(a) (b)

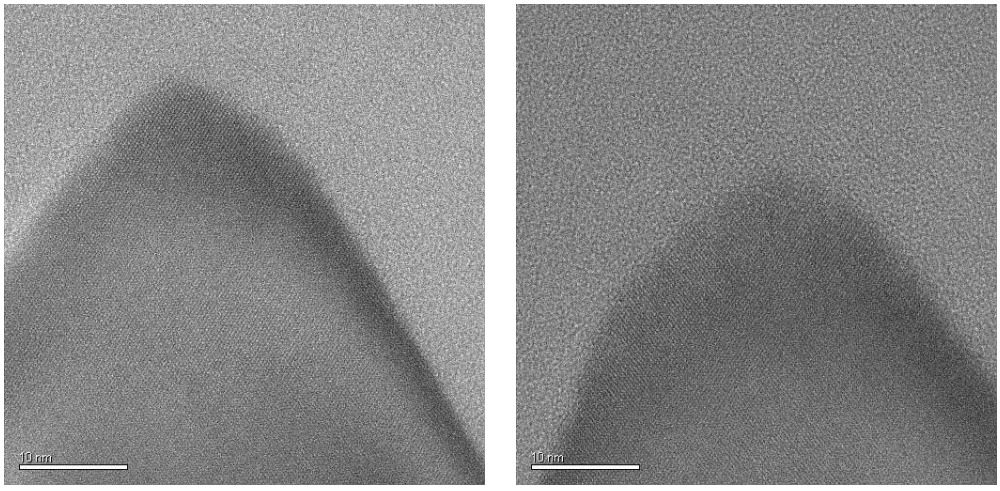


Figure 3-18. (a) High-resolution TEM image of the silicon feature in Figure 3-15 (b). (b) High-resolution TEM image of the silicon feature in Figure 3-15 (c).

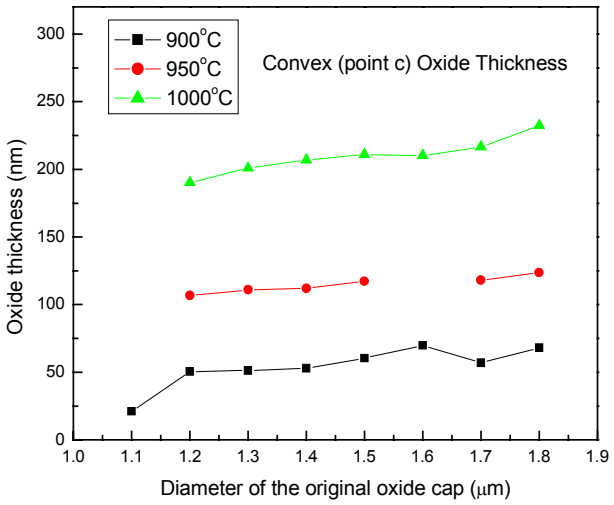
D. 3D-oxidation behavior

Oxide thickness in the flat area on the wafer was measured by an ellipsometer. However, the oxide thickness at the silicon features can only be observed in TEM images because the silicon feature sizes are smaller than the resolution of the ellipsometer. The silicon emitter is perpendicular to the (100) silicon wafer. We have to make sure that the TEM images are taken along the (110) direction to obtain the correct oxide thickness information. Table E-1 summarizes the emitter height and emitter tip radius, and oxide thickness at different positions at different oxidation conditions obtained from TEM images. The positions of a-d is labeled in Figure 3-15 (l), where a is the flat area near the emitter, b is the sidewall, c is the emitter edge, and d is the top of the emitter.

The oxidation behavior before the silicon emitter is sharpened, shown in Figure 3-15 (d)-(k), is similar to what was reported in previous work [3.28-3.30]. The edge of the silicon features has lower oxidation rate due to stress effect. The normal stress on the convex area increases the activation energy of the oxidation reaction hence reduces the oxide growth rate. The oxide thickness ratio at the edge (c) to the flat area (a) is always smaller than 1. In other words, the oxidation at the convex edge is reaction controlled, and the effect of stress is on B/A, the linear rate constant. At the same oxidation condition, the smaller the silicon feature, the thinner the oxide thickness at the convex edge (c) is as shown in Figures 3-19 (a) and (b). This is because the stress in the smaller feature is more difficult to relieve when the top area of the emitter is small and the edges are very close. The oxide thickness ratio, c/a, is the highest when oxidation occurs at 1000 ^{o}C for 10 hours as shown in Figure 3-20 (a). The ratio is about 0.99 for the largest feature under this oxidation condition. In other words, there is almost no stress effect. It is because oxide flows at temperatures higher than 950 ^{o}C- 965 ^{o}C in dry oxidation and viscous flow of the oxide relieves stress. The c/a ratio is lowest when oxidized at 900 ^{o}C than 950 ^{o}C because the stress increases as the oxidation temperature decreases. Figure 3-20 (b)

shows that the c/a ratio increases (closer to 1) as the oxidation time decreases at 950 ^{o}C due to smaller stress in thinner oxide.

(a)



(b)

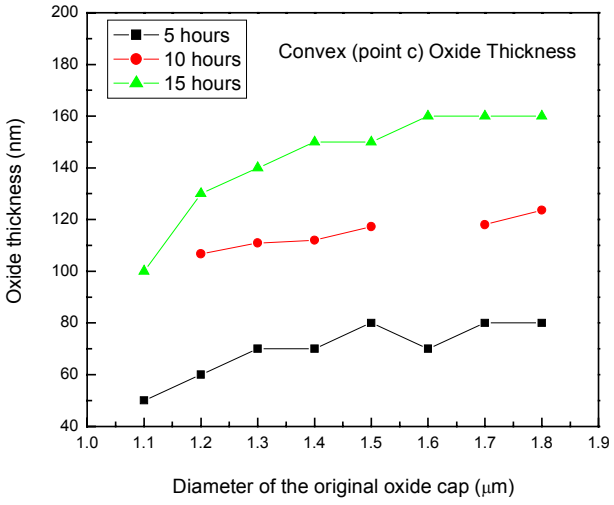
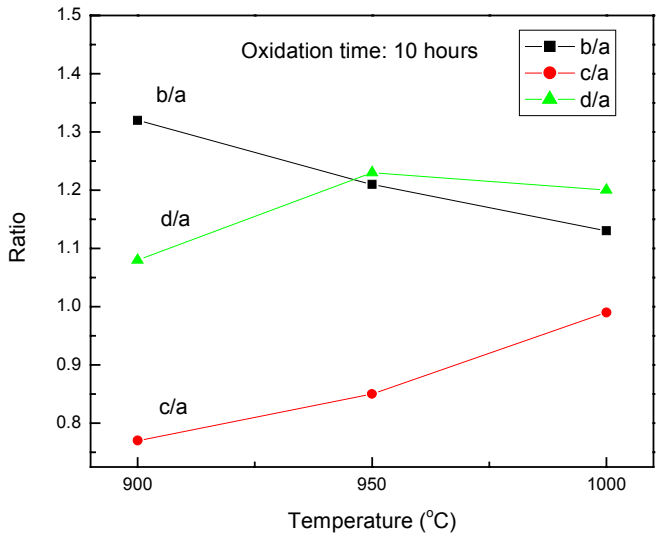


Figure 3-19. The oxide thickness at the convex edge (point c) (a) at different oxidation temperatures for 10 hours, and (b) in different oxidation time at 950^{o}C.

(a)



(b)

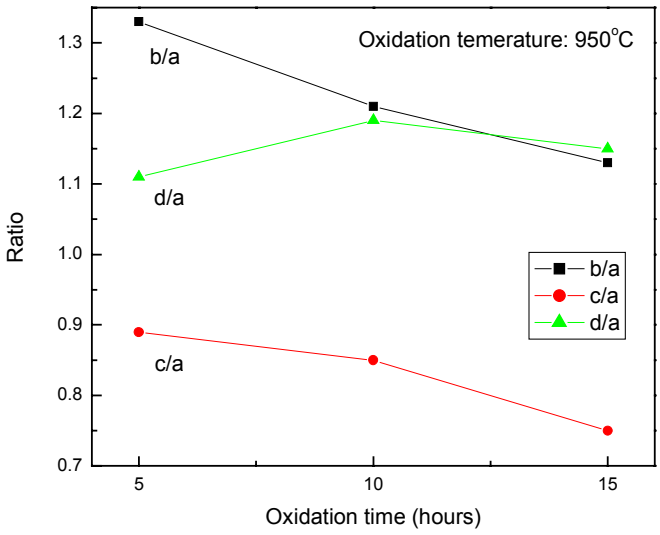


Figure 3-20. The oxide thickness ratio at different location (points b,c,d) to flat area (point a) at the largest silicon features (a) at different oxidation temperatures for 10 hours, and (b) in different oxidation time at 950°C.

The oxide on the sidewall is thicker than the oxide in the flat area, but the difference in the thickness is not profound. According to the previous research, there is always a slower growth rate in the concave region. The sidewall of our silicon emitter is concave, but the oxide is thicker on the sidewall. The reason for the apparently contradictory results might come from the large radius of curvature on the sidewall of our silicon emitter. The concave stress effect should vanish when the radius of curvature gets larger. Kao *et al.* reported that the stress vanishes when the radius of curvature is larger than 8 μm when oxidation was carried out at 800 ^{o}C in wet oxygen for 1050 minutes [3.28]. The oxidation condition is different in our case. However, it is still expected to have very small stress on the sidewalls, which have the radii obviously much larger than 8 μm. The small increase in oxide thickness could have resulted from the different oxidation rate on oxidation surface with different crystal orientation. The flat surface (100) has the slowest oxidation rate due to the loosely packed atomic structure of silicon on (100) face. The sidewall could have slightly higher oxidation rate because the silicon feature sidewall is curved with more atomic steps to increase the reaction surface area and also the oxidation surface orientation transition from (100) to (110). Figures 3-20 (a) and (b) both show that b/a ratio deviation from unity is higher in thin oxides when oxidizing at lower temperature or shorter time duration. This suggests that it is a phenomenon linked to the linear oxidation rate constant and the interfacial reaction. For thin oxides, the oxidation process is more reaction limited since oxidant diffusion to the interface is easy. Therefore, the faster oxidation reaction is more profound in thinner oxide. The thicker oxide on the sidewall than the flat surface might lead to more compressive stress in the oxide and tensile stress in silicon and contribute to the neck breaking mechanism.

The oxide caps were removed before the oxidation sharpening process, and the top of the silicon features before oxidation was flat as shown in Figure 3-21. However, the top surface became concave after oxidation. When the oxidation occurs on flat silicon surfaces, oxide stress bows the wafer because the silicon/oxide interface constrains the expansion of oxide at the interface. The oxidized interface becomes convex [3.11]. The concave top surface of our silicon emitter is mainly due to the stress-induced growth rate reduction at the sharp edges of the silicon feature. Figure 3-22 shows the result of

digitized the top surface of the largest silicon feature after oxidizing at 950 ^{o}C for 15 hours and its polynomial fit. The center of the top surface is used as the reference point. The x-axis is the horizontal distance from the reference point along the top surface and the y-axis is the vertical distance from the reference point. The top surface shows parabolic decay starting from the edge and going towards the center. The slowest oxide growth rate on the silicon feature occurs at the upper edge because the silicon reaction rate is reduced by the stress at the convex edge. The stress gradually decreases away from the convex edge, and the oxidation rate increases toward the center. The oxide growth rate at the center should be the largest along the upper surface and the difference in oxide growth rate results in concave structure. If the convex edges are separated further apart as shown in Figure 3-15 (j) and (k), the stress can be completely relieved at the center of the upper surface. The stress free region at the center of the upper surface should have the same oxide thickness as the flat region, but it is actually a little thicker than the flat region in the larger silicon features. This could be explained by the diffusion of oxidant along the silicon/oxide interface from the convex regions to the center of the top surface hence increasing the oxidation rate at the center of the top surface. Two-dimensional simulations show that the oxidant concentration at the interface is high in convex region than the flat surface [3.28]. However, the oxidation rate in the convex region is reduced due to stress-increased activation barrier of the oxidation reaction. Excess oxidants at the convex region diffuse along the interface toward the center of the top surface due to concentration difference hence increase the oxidation rate at the center of the top surface. Figure 3-20 (a) shows that d/a is temperature dependent and it increases with temperature. Even though the amount of excess oxidants is larger when oxidized at lower temperature due to more retarded oxidation, the reaction rate of excess oxidants is much higher at higher temperature and result in higher d/a. In other words, for the top surface of the silicon post, the oxidation is reaction controlled even though the oxide is thicker because the amount of oxidants that diffused to the reaction interface is sufficient. The oxidation on the top surface is reaction controlled, and the effect of stress is on B/A, the linear rate constant. When oxidized at 950 ^{o}C and 1000 ^{o}C, the ratios (d/a) in both conditions are almost the same. It is speculated that the larger amount of excess oxidants in 950 ^{o}C condition compensates the lower reaction rate of excess oxidants.

This argument could also apply to the larger oxide thickness on the sidewall. However, we believe that the dependence of oxidation rate on crystal orientation plays a larger role in the oxidation of the sidewall, especially at lower oxidation temperature.

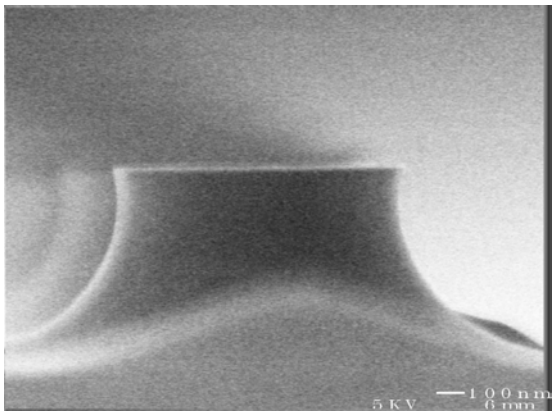


Figure 3-21. SEM image of silicon emitter before oxidation and after oxide cap removal. The original oxide cap diameter is 1.6 μm.

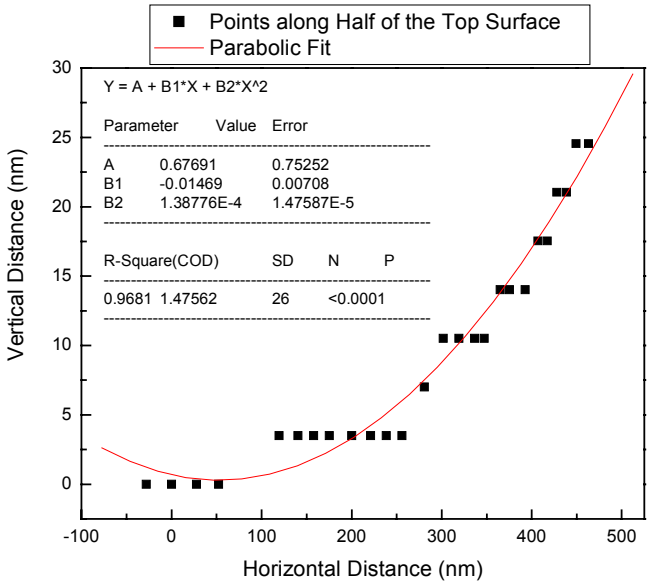
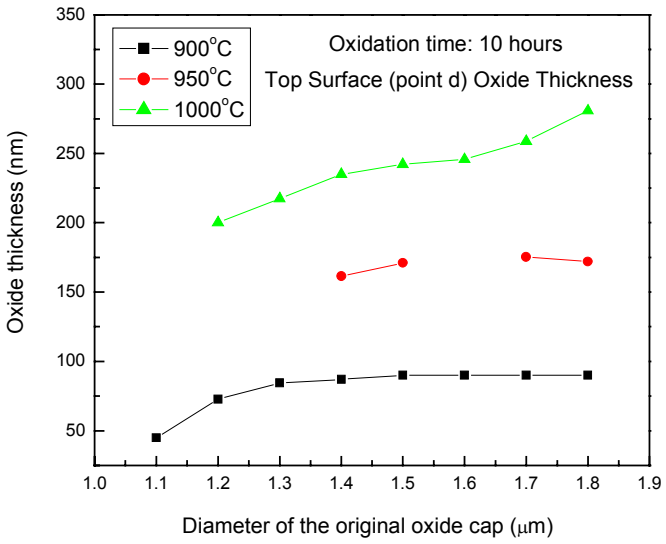


Figure 3-22. Digitized result of the top surface of the largest silicon feature after oxidizing at 950 ^{o}C for 15 hours and its polynomial fit. The reference point is the center of the top surface. The x-axis is the horizontal distance from the reference point and the y-axis is the vertical distance from the reference point.

If the convex edges are closer, as shown in Figure 3-15 (d) and (e), the stress at the center of the top area is high and the oxidation rate is still low. It results in thinner oxide at the center as the silicon feature gets smaller as shown in Figures 3-23 (a) and (b). As the stress difference between the center and edge becomes smaller, the radius of curvature on the top surface becomes larger. Figure 3-24 summarizes the trend of the oxide thickness at the center of the top surface changing with the diameter of the top surface, L. There are three regimes: in the first regime as L is small, $d/a < 1$ because the oxidation reaction is limited by the stress. In the second regime, $d/a > 1$. There are two oxidant concentration fluxes in this regime, one is the original oxidant flux from the top ($\varphi_{\perp}$) and the other is the excess oxidant flux from the side ($\varphi_{//}$). The oxidation rate in this regime is enhanced because $\varphi_{//} + \varphi_{\perp} > \varphi_{\perp}$. The maximum value of d/a observed is ~ 1.2, which means that $\varphi_{\perp} \sim 0.2\ \varphi_{//}$ at L ~ 0.8μm. In the third regime where L is very large, there is no stress and $\varphi_{\perp} >> \varphi_{//}$, therefore, $d/a \rightarrow 1$. In other words, the value of $\varphi_{//}$ and $\varphi_{\perp}$ should be comparable to have $d/a > 1$. The peak of the d/a is expected to occur at L of the order of 1 μm. It is because the oxide thickness is the order of 0.1 μm and the amount of oxidants from the top is expected to be much more than the excess oxidants from the edge of the silicon feature. It is expected that $\varphi_{\perp} >> \varphi_{//}$ at L of several μm. Figures 3-23 fall in the first regime and second regime around the peak of Figure 3-24, the oxide thickness at the center of the top surface decreases and the radius of curvature increases as the top area diameter decreases. Figure 3-15 (d) is an extreme case of where the top oxide thickness is the same as the convex oxide thickness and the top surface is almost flat. In other words, the characteristic length, which is defined as the radius of "equal-stress circle" with the same stress as the convex point, is 50 nm, half of the diameter of the top surface. The concave curvature of the top surface is much larger when oxidation occurs at 1000 ^{o}C than that at 950 ^{o}C as shown in Figures 3-25 (a) and (b) because the oxide viscous flow at 1000 ^{o}C partially relieves the stress. When oxidation occurs at 950 ^{o}C or 900 ^{o}C, there is no viscous flow to relieve the stress. The normal stress is low in thin oxide and increases in thicker oxide. Therefore, the concave curvature of the top surface is smaller when the oxide is thicker. For example, the curvature of the concave

top surface is smaller when oxidation occurs at 950 °C for 15 hours than at 950 °C for 5 hours as shown in Figures 3-25 (a) and (c).

(a)



(b)

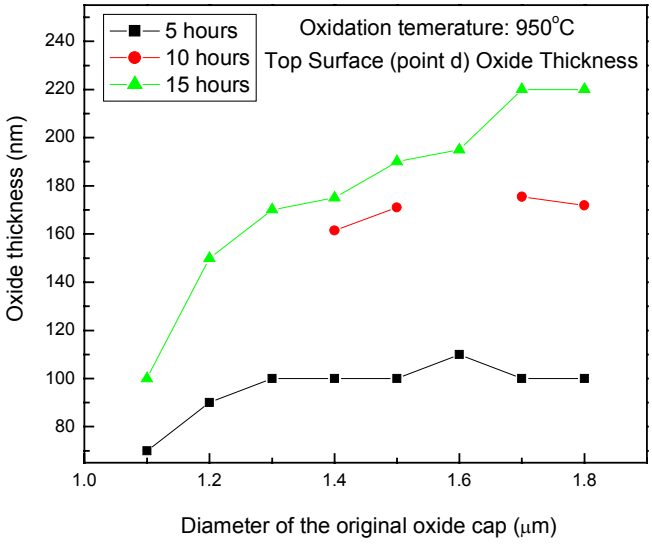


Figure 3-23. The oxide thickness at the center of the top surface (point d) (a) at different oxidation temperatures for 10 hours, and (b) in different oxidation time at 950°C.

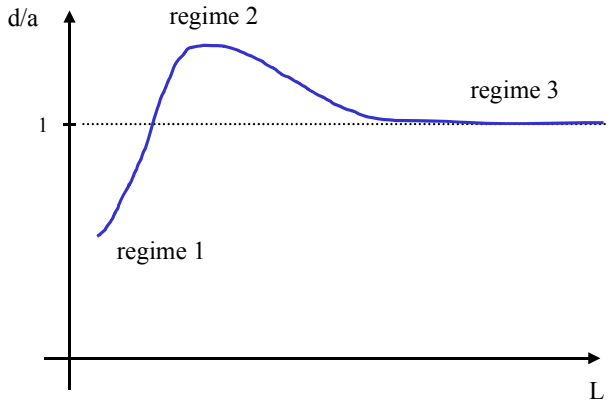
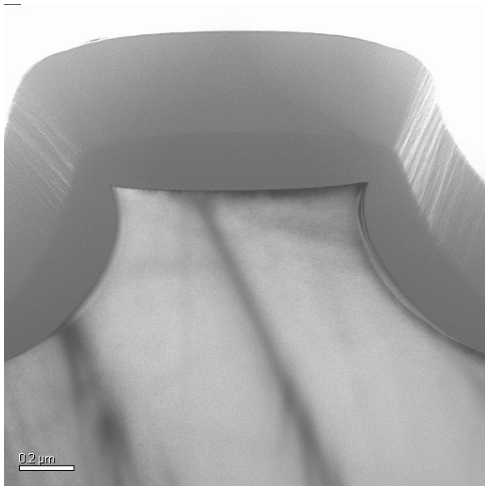
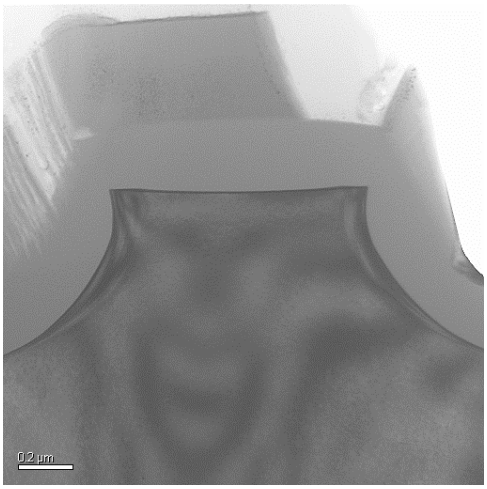


Figure 3-24. The trend of the oxide thickness at the center of the top surface changing with the diameter of the silicon feature top surface, L.

(a)



(b)



(c)

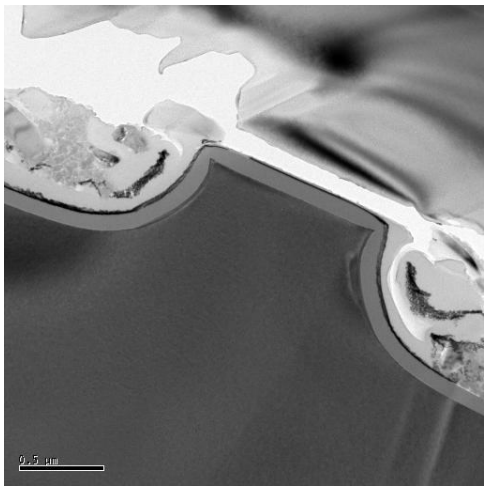


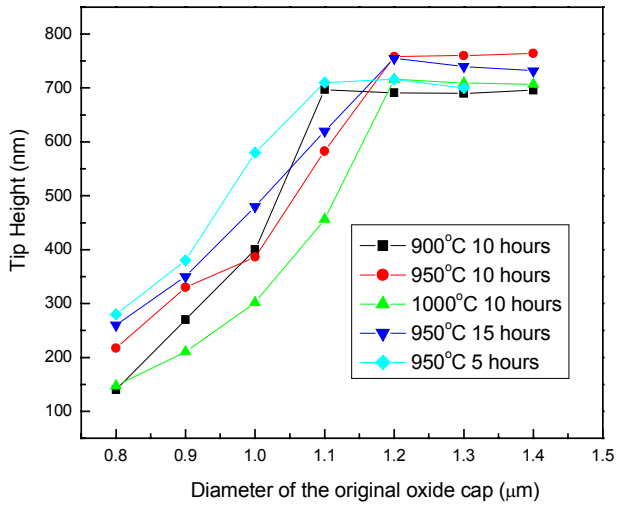
Figure 3-25. TEM images of the largest silicon features (original oxide cap size is 1.8 μm) oxidized at (a) 950 ^{o}C for 15 hours and (b) 1000 ^{o}C for 10 hours (c) 950 ^{o}C for 5 hours. Silicon dioxide is thicker in (b), but the top surface is more curved in (a) due to stress relief.

The oxidation behavior is similar at different oxidation temperatures and time duration. Unfortunately, the neck breaking process is only shown in the oxidation at 950 ^{o}C for 15 hours. The neck breaking process appears to have a very small process window. If the difference of the original oxide cap diameter were smaller in our design, the neck breaking process should be seen in all oxidation conditions. Meanwhile, characteristic length can also be measured on silicon post with the onset of the neck breaking in the oxidation at 950 ^{o}C for 15 hours. It is suspected that these two observations are related.

The tip heights and tip sharpness in these oxidation experiments are shown in Figures 3-26 (a) and (b). It is difficult to compare between different oxidation temperatures and time duration. It is because the experiments were done on different wafers and the silicon features before oxidation have small variation among these wafers even they were from the same batch of the fabrication processes. For example, the silicon features (original oxide cap is 1.1 μm) are still in the neck breaking stage when oxidizing at 950 ^{o}C for 15 hours while the silicon emitters are formed on the silicon features with the same original oxide cap size if oxidized at 950 ^{o}C for 10 hours. It is obvious that the silicon features

before oxidation sharpening are a little over-etched on the later wafer. A more thorough experiment needs to be designed to quantitatively study the stress effect on the three-dimensional oxidation mechanism. In this thesis, we present a qualitative study of the three-dimensional oxidation mechanism.

(a)



(b)

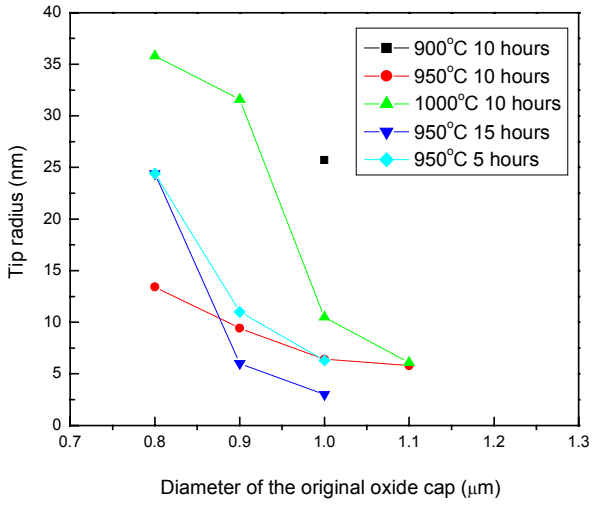


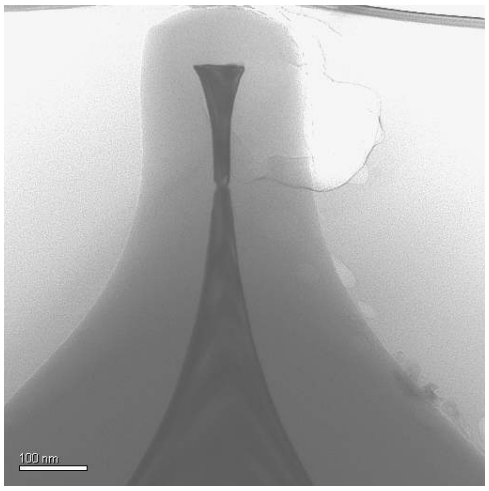
Figure 3-26. (a) The tip height and (b) tip radius at different oxidation conditions.

The mechanism of three-dimensional oxidation is very similar to two-dimensional oxidation as previously reported [3.17, 3.26-3.28]. Stress plays an important role in the oxidation mechanism. It is more profound in three-dimensional oxidation with one more degree of freedom. Furthermore, both the oxidant diffusion and Si/SiO_2 interface reaction are also more complicated in three-dimensional oxidation.

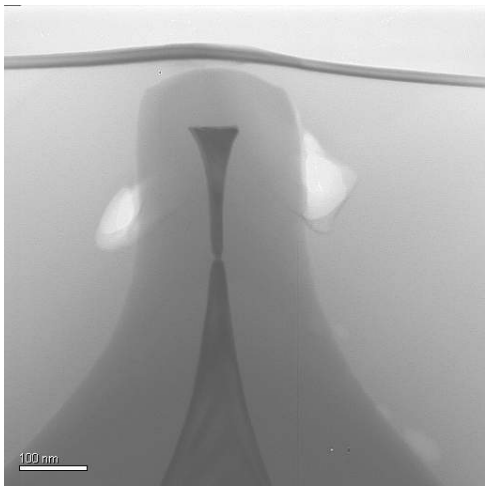
Oxidation Process in the Device Wafer

Monitor wafers with partially sharpened emitters were examined by high resolution JEOL 2010 TEM at 200 KeV [3.19] to confirm the mechanism of oxidation sharpening process for emitter formation. These monitor wafers were the same batch as the device wafers with the same etch processes, oxidation temperature and time duration as discussed in Section 3.1. However, due to the non-uniformity of the fabrication process, these wafers had a bit larger silicon neck than the device wafer before oxidation sharpening and this produces some non-fully sharpened emitters. Figures 3-27 (a)-(c) show the TEM images of the partially sharpened emitters and provide very good information of how the silicon neck region was consumed to form very sharp tip. The thermal oxide layer was kept on the emitter and the oxide was well preserved by the epoxy. Figure 3-27 (a) shows that the silicon neck starts to break and the groves are shown at the neck region. Figure 3-27 (b) shows the larger groves at the neck region and the neck width along with the whole silicon feature become thinner. Figure 3-27 (c) shows that the silicon neck finally breaks completely and the sharp emitter tip is formed. This series of tip formation images confirms that the emitter is formed by oxidation sharpening with the neck breaking stage instead of a continuous oxidation process.

(a)



(b)



(c)

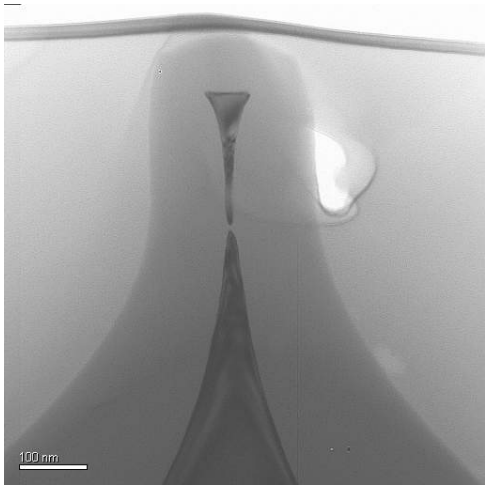


Figure 3-27 (a)-(c). TEM images of how the silicon neck region was consumed to form sharp tip.

3.4 Chapter Summary

In this chapter, we presented the process flow to fabricate uniform and sharp silicon field emitters. We discussed the following: photolithography process, oxide disks definition, isotropic silicon etch, and oxidation sharpening. The emitter structure was next characterized by extensive TEM observation. The tip radius observed in over 100 randomly sampled emitters had a log-normal distribution: the tip radius ranges from 1.5

to 19 nm and the peak of the distribution is 6.2 nm with the width of 0.37 nm. Three-dimensional thermal oxidation for the silicon emitter sharpening process was discussed in detail: Five different oxidation conditions at different oxidation temperatures and time duration were carried out to study the oxidation behavior. Oxide growth rate at the convex region on the silicon feature slowed down due to stress. Oxide growth rate at the large curvature concave region was not affected due to the relief of the stress. Viscous flow which occurs at $\geq$ 965 ^{o}C relieves the stress during oxide growth. A new sharp emitter tip formation mechanism is proposed. Rather than a continuous oxidation process, a neck breaking stage occurs before the sharp emitter tip is formed. Stress from volume difference of silicon and silicon dioxide is the main cause for the emitter neck breaking. Over-oxidation would shorten and blunt the emitters, but a slight over-oxidation would shorten the emitter without altering the tip radius. The tip formation mechanism was again confirmed by the emitters fabricated on the device wafers.

4. Device Design and Fabrication

To realize the goals for this thesis, careful design and fabrication of device is needed. In this chapter, the design of the device and the device fabrication process flow are presented.

4.1 Device Design

As we mentioned in Chapter 2, one of the approaches to control the field emission device with the electron supply is to add a current source to the field emission device. In this thesis, we use a MOSFET connected to the emitter circuit as a voltage controlled current source because of its well-known device physics and mature device fabrication process. There are several literature reports on MOSFET control of the field emission device [4.1] and there have been other reports of integrating other current sources with the field emission device [4.2-4.4]. In this work, we fabricate the MOSFET on the cathode side of the field emission device [4.5]. In other words, the MOSFET device is in series with the field emission arrays on the same substrate.

Device Structure

The integrated MOSFET/FEA device structure is shown in Figure 4-1. It is a four terminal (tetrode) device consisting of a MOSFET and a field emission array. The field emission array (single tip shown in Figure 4-1) is the drain of the MOSFET. The device is similar in concept to the device reported by Electrotechnical Laboratory [4.6-4.8] except that the MOSFET drain is lightly doped to increase the voltage that can be applied to the device. The four external electrodes are the MOSFET source, the MOSFET gate, the FEA extraction gate, and the FEA anode. We only fabricated the substrate part of the four-terminal device. The anode was not fabricated or packaged with the substrate in this

thesis. The MOSFET drain and the FEA emitter form an internal floating node with the voltage between the FEA gate and the MOSFET source divided between the MOSFET drain-to-source voltage and the FEA extraction gate-to-emitter voltage. The emission current of the device is modulated by either the FEA extraction gate (with the MOSFET gate voltage held constant) or the MOSFET gate (with the FEA extraction gate voltage held constant).

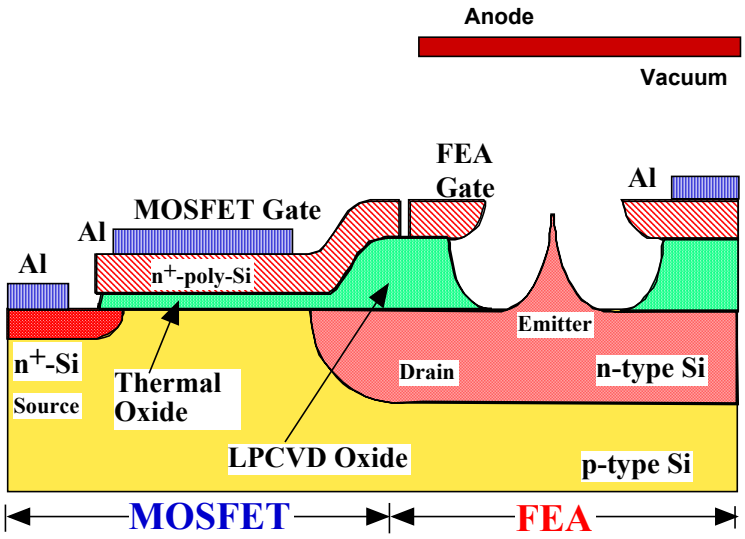


Figure 4-1. A LD-MOSFET/FEA device structure.

Device Operation

The MOSFET device supplies electrons from the source of the MOSFET to the emitting surface, which is the drain of the MOSFET, through an inversion layer formed in the MOSFET channel. The carrier density in the inversion layer is controlled by the gate voltage of the MOSFET. The electron transmission at the emitting surface is determined by the width of the barrier and hence the applied voltage to the FEA gate. In order for the FEA surface to have a high transmission, the extraction gate voltage needs to be very high. Consequently, the MOSFET must be able to withstand high voltages between its drain and source electrodes, implying that it must have a high drain-to-source breakdown voltage.

Material and Process Selection

The devices were fabricated on 4-inch p-doped (100) silicon wafers with resistivity of 10-20 ohm-cm substrates. P-type silicon wafers were selected to fabricate NMOS devices on the p substrates. This substrate resistivity was chosen to allow ion implantation of an n-well for the emitter formation while not degrading MOSFET properties such as threshold voltage and device isolation.

The n-well provides electrons to the emitters, which would be formed within the well. Electrons are supplied either from the n-well when the field emitters are operated without MOSFET or from the MOSFET channel in the integrated MOSFET/FEA devices. The n-well doping concentration should be high enough to supply sufficient electrons to the emitters but should not be too high as to allow MOSFET breakdown due to high field at the drain region. A conventional MOSFET is unable to sustain the high drain-to-source voltages required for electron extraction because of the high electric field at the drain/channel pn junction. High drain doping results in high electric fields and consequently high electron velocities and energy transfer between the electrons and the silicon lattice. If the field is high enough, impact ionization occurs leading to Avalanche multiplication, rapid rise in current, and breakdown. Our approach for increasing the voltage at which breakdown occurs is to reduce Avalanche multiplication and impact ionization by decreasing the electric field in the drain/channel pn junction. This is accomplished by reducing the drain doping. Thus, our device uses a lightly doped drain (LDD) to reduce the drain electric field, leading to reduced impact ionization and higher drain voltages [4.9-4.17]. The phosphorous doses of $2x10^{12}$ and $5x10^{12}$ cm^{-2} were both selected to have the target doping for the drain region of $\approx 1 \times 10^{16}$ cm^{-3} and it should result in a drain breakdown voltage of $\approx$ 60 V [4.18]. When there is no MOSFET channel threshold voltage adjustment, the substrate (p) with doping concentration of $\approx 1 \times 10^{15}$ cm^{-3} surrounds the drain region (n). The breakdown voltage of the MOSFET is determined by the substrate doping because the lightly doped side of the pn junction

dominates the breakdown voltage; therefore the breakdown voltage is larger than 100 V. However, when the MOSFET channel is implanted with higher doping concentration than the substrate doping to adjust the threshold voltage, which is the standard CMOS process, the doping concentration of the drain would determine the breakdown voltage if the channel doping is higher than the drain doping. Since the emitters need to be formed inside the n well and the emitter formation process requires an etched-down of the substrate of up to 1 μm, high-energy implantation is needed to form deep enough n well to accommodate silicon loss due to oxidation and etch. 180 KeV phosphorous implantation should provide > 2 μm n well according to the process simulation. The target doping for the drain region of ~ 1 x 10^{16} cm^{-3} is sustained up to ~ 1 μm in the n well.

Emitter formation follows the process and structure selection described in Chapter 3. The substrate resistance was too low for device isolation and the source-drain leakage was high in the preliminary test. There are two approaches to solve this source-drain leakage problem: one is to increase the original substrate dopant concentration, and the other is to employ extra implantation steps. The drawback of the first approach is that it would be difficult to control the n- implantation used to define the lightly doping region of the LD-MOSFET. On the other hand, the advantage is that we do not need two extra implantation steps, one for device isolation and the other for threshold voltage change. Our decision was to avoid the possible n- implantation issues, go for low dopant concentration substrate, and use extra boron implantation steps. The wafers should be implanted with 3.5x10^{13} cm^{-2} dose of boron to achieve target doping for the non-active region of 1 x 10^{18} cm^{-3} and device simulation shows that it should result in the threshold voltage of above 120 V.

Next, we need an oxide layer with a thickness approximately of the silicon emitter height as the gate insulator layer. The breakdown voltage of low temperature oxide (LTO) after densification at high temperature is similar to that of thermal oxide [4.19]. A thinner oxide layer would result in lower oxide breakdown voltage, while a thicker oxide layer would result in a tip below the gate electrode leading to gate leakage in operation. The

thickness chosen is to make sure that the emitter tip apex could be surrounded by the gate electrode in the final device structure. This oxide needs to be removed and re-grown in the MOSFET channel region to have thinner and better oxide. Between the removal of deposited oxide and the re-grow of a thermal oxide, we need to add an implantation step to adjust the MOSFET threshold voltage. The MOSFET was originally designed to be a normally off device. However, boron in the p type substrate is preferentially incorporated into the silicon dioxide layer due to its relatively small segregation coefficient (~ 0.15 to 0.3), where the segregation coefficient is defined as the ratio of the equilibrium concentration of the impurity in silicon to its equilibrium concentration in the oxide [4.20]. It resulted in slightly negative threshold voltage observed in the preliminary experiment. Our target doping for this threshold voltage adjustment implantation was 4 x 10^{17} cm^{-3} and it should result in the threshold voltage of 2.8 V according to our simulation. A very shallow junction is needed for the channel; therefore, low energy is used in this implantation. Process simulation shows that 10 KeV boron implantation can provide ~ 0.13 μm junction depth. Rapid thermal annealing (RTA) should be adopted in the annealing step after this ion implantation because this would be the third implantation in the whole LD-MOSFET/FEA fabrication process and we do not want to alter the doping profile from the previous implantation/annealing. The subsequent annealing processes should all be done in RTA. The gate oxide thickness is ≈ 50 nm to have better control of the MOSFET. Lower MOSFET gate voltage, V_G, is required to turn on the MOSFET channel if the gate oxide becomes thinner. The oxide thickness was picked arbitrary to be thin enough but not so thin to cause oxide breakdown. The critical electrical field of gate oxide layer is 7 x 10^6 V/cm [4.21]. In other words, if the maximum applied field across gate oxide is 10 V, the oxide thickness must be larger than 15 nm to avoid oxide breakdown.

Polysilicon was chosen as the gate material for both MOSFET and FEA. Thickness of the polysilicon layer is not critical. The best thickness is to have the emitter tip apex surrounded by the gate electrode in the final device structure. The only concern is that we should have a final thickness larger than 100 nm at the gate electrodes after CMP and

plasma etch. We also need the polysilicon gates to be conductive. We can either implant the polysilicon layer or dope the layer in the furnace.

FEA gate aperture needs to be opened. We used chemical-mechanical polishing (CMP) to planarize the silicon surface and meanwhile open the FEA gate aperture. Using CMP to fabricate field emission device was first developed at Micron Display Technology. It was employed to address the issues of scalability and application to high-volume manufacturing [4.25]. CMP could produce self-aligned extraction grids (gates) around each tip without a mask and photolithography step.

The MOSFET source needs to be ion implanted with arsenic of $7x10^{15}$ cm^{-2}. A high dose of arsenic ions was chosen according to the standard CMOS baseline to have a shallow and heavily doped source area. Low resistivity is needed to the source contact. Aluminum, which is the most common metal for the standard CMOS process was selected as the metal contact. Ti and TiN are needed underneath the Al as diffusion barriers to avoid the spikes between aluminum layer and silicon substrate [4.22-4.24]. TiN is a popular barrier layer, and its electrical resistivity is low enough for being used as a contact material. However, the contact resistance to silicon is somewhat higher than that of Ti or $TiSi_2$. Therefore, TiN is usually used in a bi-layer structure with TiN on top of Ti, where Ti usually reacts to form $TiSi_2$ for a better contact. Ti also serves as an adhesion layer between TiN and Si.

Device Dimension Selection

The goal of this thesis is to use the MOSFET to control emission current from the FEA. As we mentioned in Chapter 2, the operating point of the integrated MOSFET/FEA device is when emission current of the FEA equals the drain saturation current of the MOSFET. The dimension of the LD-MOSFET was chosen to have saturation current that is compatible with the FEA emission current. When modulating the electron supply to control the emission process, the extraction gate voltage is usually kept constant and

MOSFET gate is used to switch the integrated device. The extraction gate voltage should be kept high to ensure the high transmission probability but not too high as to increase the energy stored in the field emission device that results in short device life time.

Recall the equations from Chapter 2,

$$I_D = \mu_n C_{OX} \frac{W}{L}\left[(V_{GS} - V_T) \times V_{DS} - \frac{V_{DS}^{\ 2}}{2}\right]; \qquad V_{DS} < V_{GS} - V_T \tag{4.1}$$

$$= \frac{1}{2}\mu_n C_{OX} \frac{W}{L}\left[V_{GS} - V_T\right]^2; \qquad V_{DS} > V_{GS} - V_T \tag{4.2}$$

$$I_E = a_{FN} V_{GE}^{\ 2} \exp\left[\frac{-b_{FN}}{V_{GE}}\right], \tag{4.3}$$

$$I_A = I_E = I_D, \tag{4.4}$$

and

$$V_{GFEA} = V_{GE} + V_{DS}. \tag{4.5}$$

Our material design results in

C_{ox} = 6.9 x 10 $^{-8}$ farad (MOSFET gate oxide thickness is 50 nm),

μ_n = 480 cm^2/V-s (channel doping is 4x10^{-17} cm^{-3}),

r ~10 nm,

a_{FN} = 1.5 x 10 $^{-4}$,

b_{FN} = 530.

For a 10x10 FEA, if we want to have the MOSFET control regime occur in a reasonable voltage range, for example ≈ 50 V, in other words, $V_{GFEA\_saturation} \approx 50$ V, by assuming ΔV (V_{GFET}-V_T) = 1 V, $V_{DS\_sat} \approx 1$ V and $V_{GE\_saturation} \approx 49$ V,

$I_E \sim 720$ μA (if electrons emit equally for the 100 emitters),

the MOSFET should have a W/L ≈ 40. If only 1 % of the emitters can emit or in a single emitter, $I_E \approx 7.2$ μA and W/L ≈ 0.4. Therefore, in our design, the MOSFET devices have different width/length (W/L) ratios of 10 (100 μm/10μm), 1 (100 μm/100 μm), and 0.1 (10 μm/100 μm) in order to have the operating points at low FEA extraction gate voltage, usually lower than 100 V. 100 μm/10 μm were chosen to have a reasonable length. 1

μm is pushing the limit of the photolithography system and 1000 μm would result in higher resistance and sacrifice the device density.

4.2 Device Fabrication

We present the fabrication process flow for integrating the silicon field emitter arrays with LD-MOSFET in this section. Process simulation is always required before fabrication to determine the parameters of the fabrication steps, such as doping, oxidation/annealing temperature and time, etc. Careful process simulation could avoid extensive trial and errors during fabrication. Simulation results are presented along with the fabrication processes in this section.

This fabrication process consists of nine mask photolithography steps. The main fabrication steps are: post doping, silicon tip formation, insulation layer deposition, MOSFET threshold voltage adjustment, gate layer deposition and definition, MOSFET source opening/implantation, passivation layer deposition and contact opening, metal layer deposition and definition, and tip exposure.

The fabrication process is described below and Figure 4-2 is a schematic description of the process flow. The detail of the mask layout is presented in Appendix B and the process flow chart is shown in Appendix C.

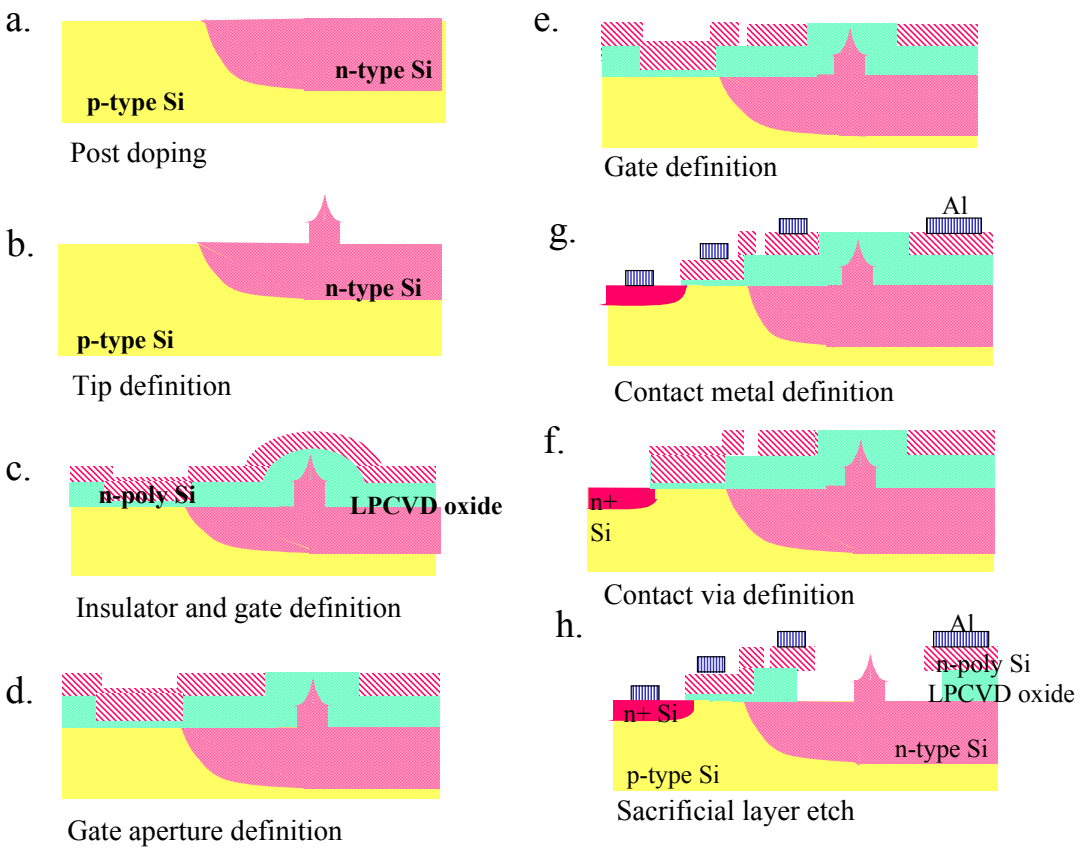


Figure 4-2. Process flow for fabricating the integrated LD-MOSFET/FEA device.

Post Doping

The process began with 4-inch p-doped (100) silicon wafers. The resistivity of the p-type wafer was 10-20 ohm-cm. First, the lightly doped drain of the MOSFET, which is also the emitter of the FEA, was defined by ion implantation. A thin layer of 0.05 μm thermal oxide was grown at 950 ^{o}C in H_2O ambient. This thermal oxide layer was necessary to avoid wafer damage in the following ion implantation step. Before the wafers were implanted, alignment marks had to be defined on the wafers. These permanent alignment marks were needed because the first photolithography step is ion implantation and would not leave any topographical marks on the wafer. Array Mask (Mask #1), which defines the n-doped area for the drain of the MOSFET and emitter of the FEA, was used for the permanent alignment mark definition. Only dies (6,1) and (6,8) on the wafers were

exposed. The standard photolithography steps were similar to the process described in Section 3.1 without the post exposure bake. Permanent alignment marks were then formed by etching oxide with BOE and etching silicon with anisotropic reactive ion etch (RIE).

The photoresist was stripped using plasma photoresist stripper. The wafers were next patterned again by Array Mask (Mask #1) and ion implanted with $2x10^{12}$/ $5x10^{12}$ cm^{-2} phosphorous at 180 KeV with 7 degree tilt. Our target doping for the drain region was ~ 1 x 10^{16} cm^{-3}. After stripping the photoresist, the implant was driven-in to 2 μm depth and activated through the growth of 0.2 μm thermal oxide in an annealing tube at 1000 ^{o}C in O_2, and H_2O ambient followed by 1150 ^{o}C in N_2 (Figure 4-2 a). Figure 4-3 shows the simulation results of the post doping profile (phosphorous dose is $5x10^{12}$ cm^{-2}) after drive-in process. It shows that the dopant concentration is ~ 2 x 10^{16} cm^{-3} at the depth of 1 μm into the n well. Figures 4-4 (a) and (b) show the phosphorous concentration profiles after drive in process from the secondary ion mass spectrometry (SIMS) [4.26], the target phosphorous doses are $2x10^{12}$ cm^{-2} and $5x10^{12}$ cm^{-2} respectively. Both of the junction depths are > 2 μm and the doping concentration of the n well is 1 x 10^{16} cm^{-3} and 1.5 x 10^{16} cm^{-3} at the depth of 1 μm into the n well, respectively.

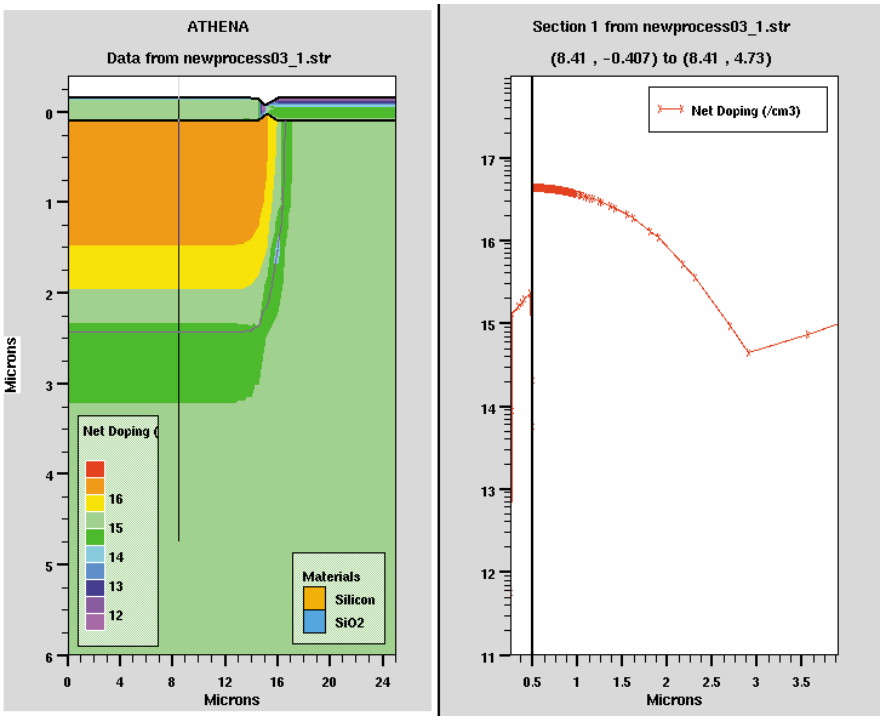
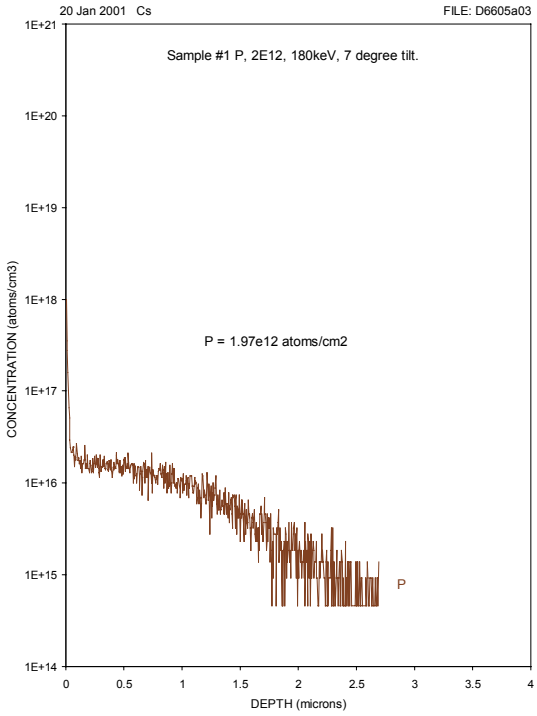


Figure 4-3. Process simulation results of the n- post doping. Dose of the phosphorous in this simulation is $5x10^{12}$ cm^{-2}. The left part of the figure is the cross-section of the wafer and the right is the doping profile after drive-in process.

(a)



(b)

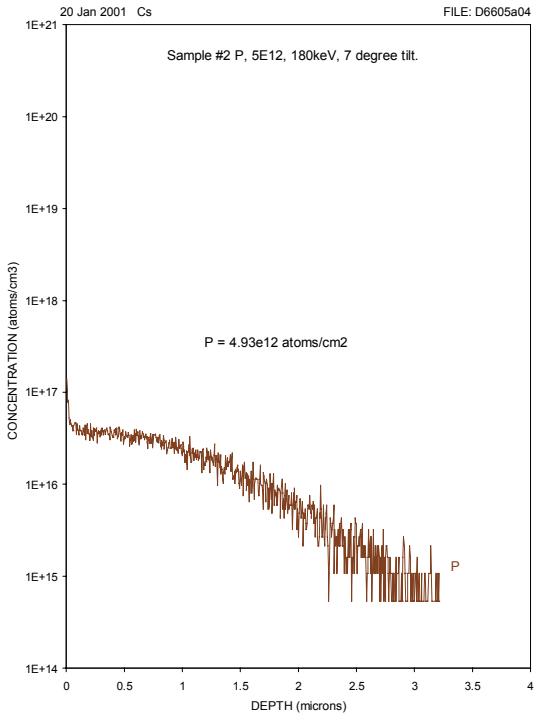


Figure 4-4. SIMS of the n- post doping. (a) Target phosphorous dose = $2x10^{12}$ cm^{-2}. (b) Target phosphorous dose = $5x10^{12}$ cm^{-2}.

Formation of Silicon Tip

Next, the wafers, coated with photoresist, were exposed with Dot Mask (Mask #2) to define arrays of circular photoresist dots on the lightly phosphorous-doped drain region. The details of forming the silicon tip and oxidation sharpening were presented in Chapter 3. Silicon tip height of ~ 1 μm was achieved as shown in Figure 4-5 (Figure 4-2 b). Figure 4-6 (a) shows one TEM image of the silicon emitter after oxidation sharpening. Figure 4-6 (b) is the close-up of the Figure 4-6 (a). The top region of the silicon is separated from the underneath silicon sharp tip by a thin oxide layer.

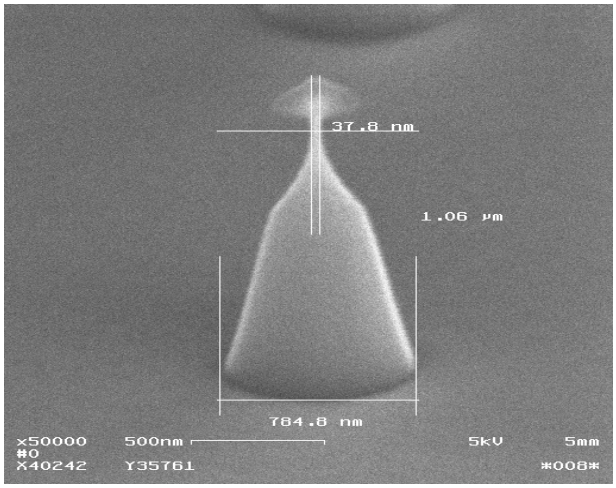
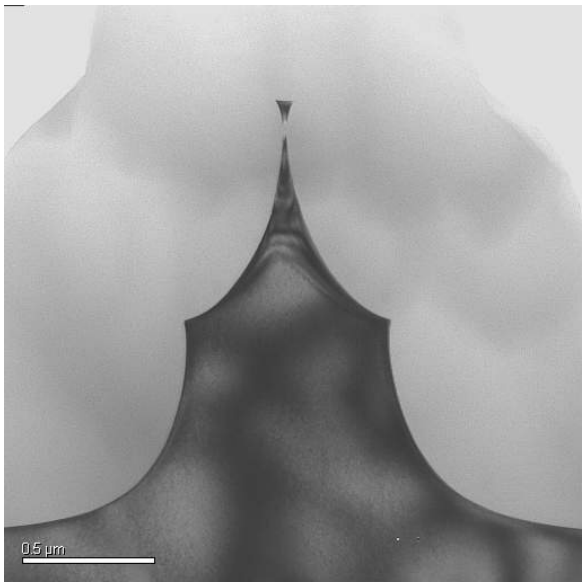


Figure 4-5. SEM image showing the silicon cone under the oxide cap.

(a)



(b)

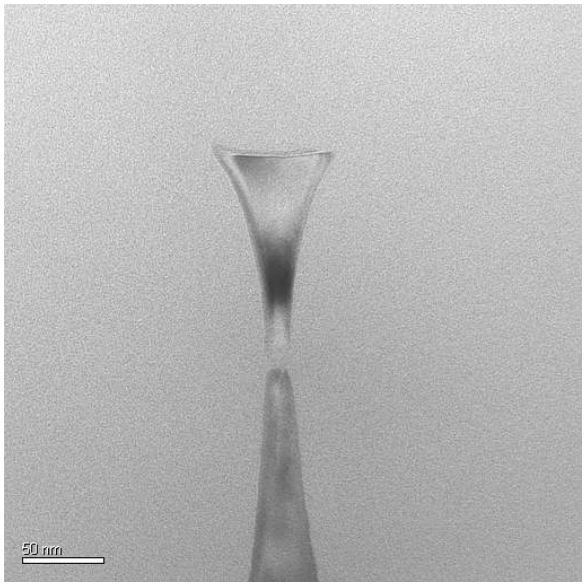


Figure 4-6. (a) TEM image of one silicon emitter after oxidation sharpening. (b) The TEM image of the close-up of (a).

Some of the SEM images were taken on the device wafer in the clean room. This SEM allowed us to monitor the whole device wafer without breaking it into pieces and without coating with Au/Pt. We could monitor the process, and only wafer cleaning by piranha solution (sulfuric acid to hydrogen peroxide of 3 to 1) was required before putting the

wafer back into the process. This SEM quality was not as good as the one outside the clean room and charging effect may be seen in the images of oxide and photoresist. However, this SEM provided us quick information on our device wafers. Better quality SEM images were taken either in Center for Materials Science and Engineering or Nanostructure Laboratory [4.27]. The monitor wafers were removed from the process flow for careful SEM inspection.

Ion Implantation for Isolation between Devices

The substrate resistance was too low for device isolation and the source and drain leakage was high in the preliminary test, therefore, Isolation Mask (Mask #9) was used to define the boron implantation area outside the device region. The wafers were implanted with 80 KeV, 3.5×10^{13} cm^{-2} dose of boron at 7-degree tilt [4.28]. Our target doping for the isolation region was 1×10^{18} cm^{-3}. The annealing and boron ion activation processes were combined with the following process.

Insulation Layer Deposition and Threshold Voltage Adjustment

A conformal, 700 nm thick oxide layer which serves as the extraction gate insulator was deposited by low-pressure chemical vapor deposition (LPCVD). The top surface of the oxide in the flat region is approximately level with the top of the emitter tips. In other words, the deposited oxide thickness is approximately the silicon cone height. The process was followed by oxide densification at 1000 ^{o}C in N_2 ambient for 20 minutes. The thermal oxide layer grown in the oxidation-sharpening step was not removed before low temperature oxide (LTO) deposition. This is because the dielectric strength of the thermal grown oxide is better than that of the deposited oxide. It also provides better quality of silicon/oxide interface with less interface defects, and it is necessary for good breakdown characteristics [4.29]. The boron ions from the last implantation for device

isolation were activated during the oxide densification process. Figure 4-7 shows the SIMS of boron doping profile after annealing. Junction depth is about 0.7 μm.

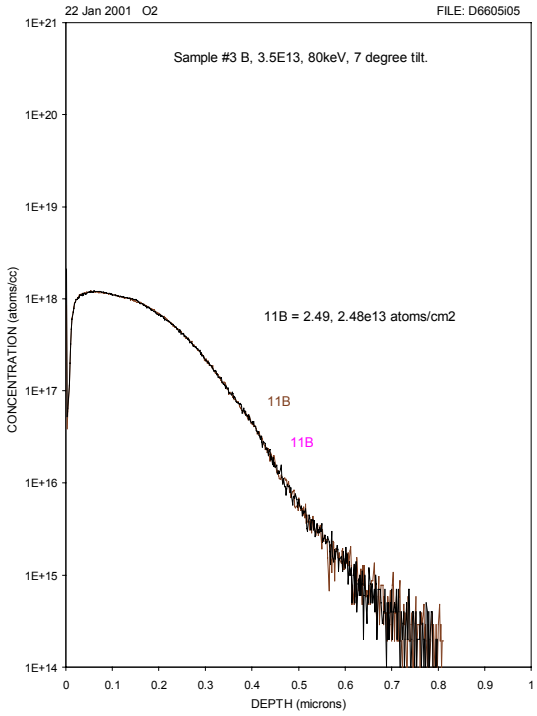


Figure 4-7. SIMS of boron doping profile from device isolation implantation. Target boron dose = 3.5×10^{12} cm^{-2}.

Next, the MOSFET channel area was defined by MOSFET Channel Mask (Mask #3) and the thick oxide in the MOSFET channel area was removed by BOE. Photoresist was removed and the wafers were oxidized to grow thin thermal oxide serving as a buffer layer in the MOSFET channel area for the threshold voltage adjustment implantation. Boron of 10 KeV and 5×10^{12} cm^{-2} was implanted in the channel region [4.28]. This implantation increases the threshold voltage from slightly negative to slightly positive value. Our target doping for this threshold voltage adjustment implantation was 4×10^{17} cm^{-3}. The wafers were annealed in the rapid thermal annealing (RTA) at 1000 ^{o}C for 20 seconds. SIMS of boron doping profile after RTA annealing is shown in Figure 4-8. The junction depth is about 0.15 μm. The buffering oxide was stripped after implantation and annealing. The MOSFET gate oxide was then re-grown in the channel region. The gate

oxide thickness is 45 nm. Figure 4-9 shows the process simulation of the insulator layer deposition and implantation processes.

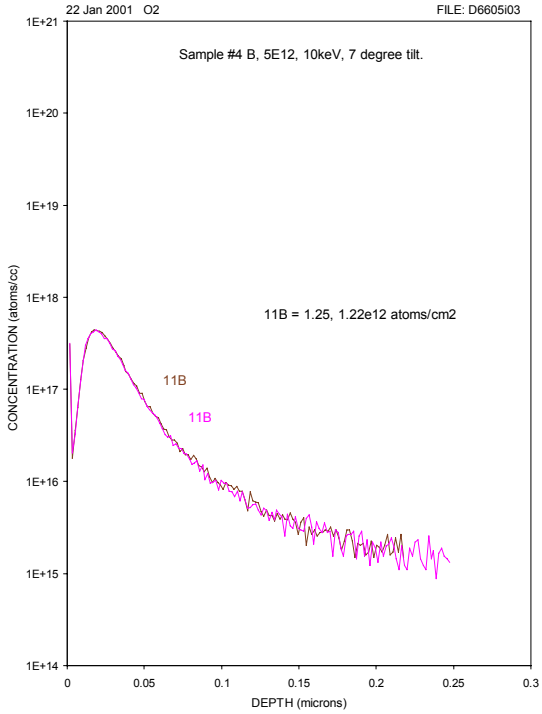


Figure 4-8. SIMS of boron doping profile from threshold voltage adjustment implantation. Target boron dose = $1x10^{15}$ cm^{-2}.

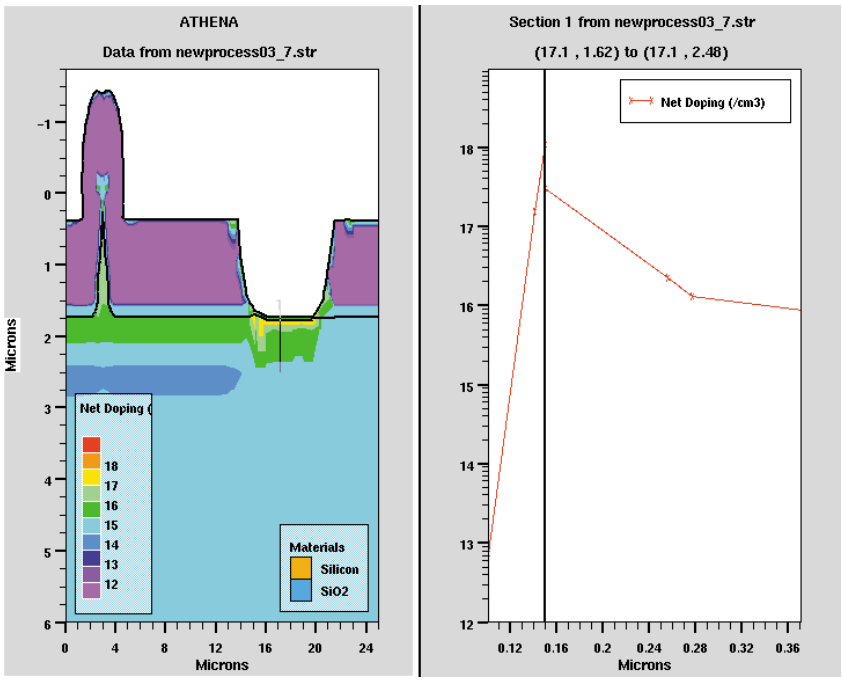


Figure 4-9. Simulation of the boron implantation process. The left part of the figure is the cross-section of the wafer and the right part is the doping profile in the MOSFET channel region.

Gate Deposition, Definition, and MOSFET Source Definition

A layer of 400 nm thick polysilicon was subsequently deposited by LPCVD as the gate electrode (Figure 4-2 c). After insulation layer and gate deposition, a blunt bump was formed above every single emitter as shown in Figure 4-10.

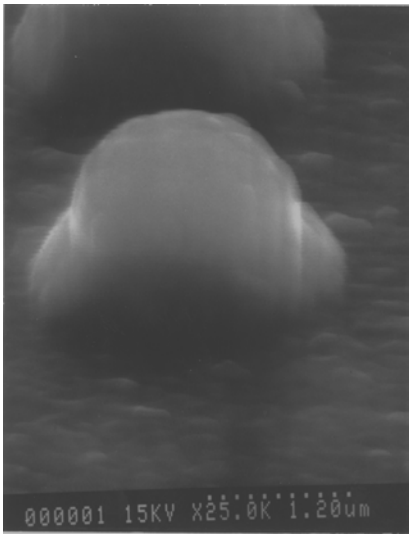


Figure 4-10. Silicon emitters were covered by LTO and polysilicon, and formed bumps on the wafer surface.

The polysilicon layer was next doped with phosphorous to increase its conductivity. The phosphorous ions were diffused into the wafer at 925 ^{o}C in $POCl_3$ for 100 minutes. $POCl_3$ gas doping process generated a thin oxide layer on top of the polysilicon layer, thus a quick BOE dip was necessary afterward. Figure 4-11 shows the simulation of the bump formation above the emitter after polysilicon deposition.

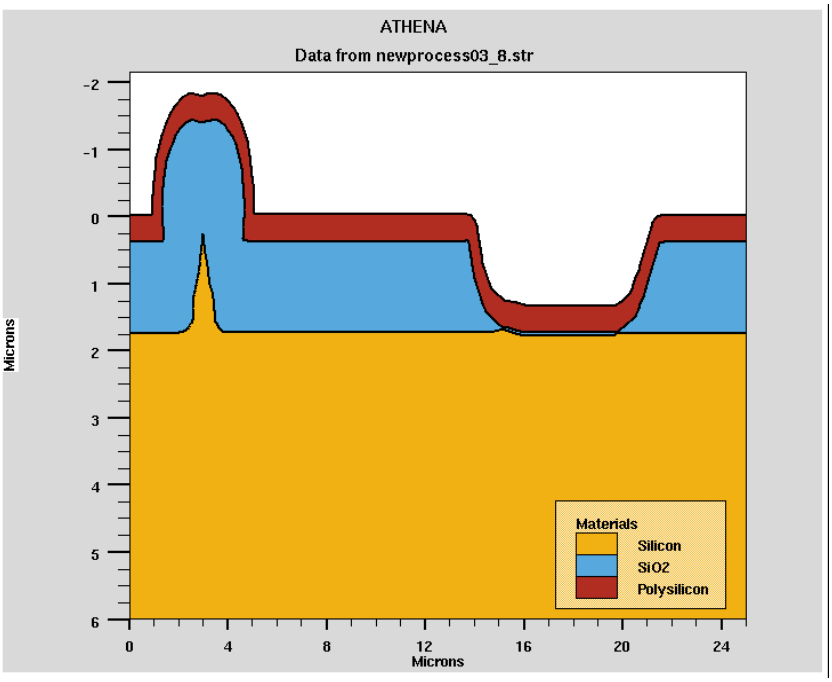


Figure 4-11. Simulation of the bump formation above the emitter after polysilicon deposition. The left part of the wafer cross-section shows the emitter area and the right part of the cross-section shows the MOSFET channel.

The wafers were chemical-mechanical polished (CMPed) to remove the bumps on the wafer surface, planarize the wafer, and reveal the FEA extraction gate aperture [4.19, 4.25] as shown in Figures 4-12 and 4-13 (Figure 4-2 d). This was the most delicate part of the whole process and careful SEM monitoring was required. Over-polishing in CMP would damage the silicon tip. On the other hand, under-polishing would form an emitter structure with silo-gate structure and silicon emitter tip would be below the extraction gate as shown in Figure 4-14. When silicon emitter tip is under the gate, the emission current could easily be intercepted by the gate instead of the anode if the gate aperture is not large enough. Polysilicon layer thickness was also monitored during the CMP processes. To remove the bump completely and make the emitter tip level with the extraction gate, the polysilicon layer in the flat area usually was over-polished due to the nature of CMP. Since part of the polysilicon layer in the flat region would serve as the MOSFET gates, a thickness of over 150 nm is required. Therefore, in order to get a polysilicon layer thicker than 150 nm, the bumps need to be slightly under-polished as

shown in Figure 4-14 and result in silo-shaped gate in our devices. The FEA gate aperture was 1.3 μm in diameter.

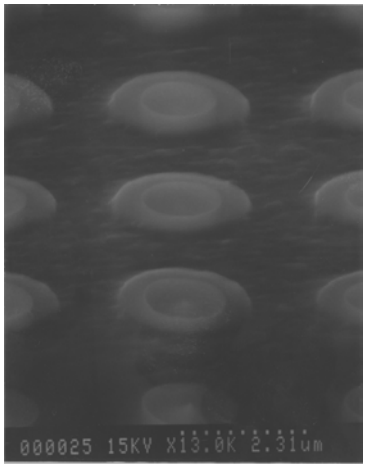


Figure 4-12. Wafers went through CMP and the FEA extraction gate apertures were opened.

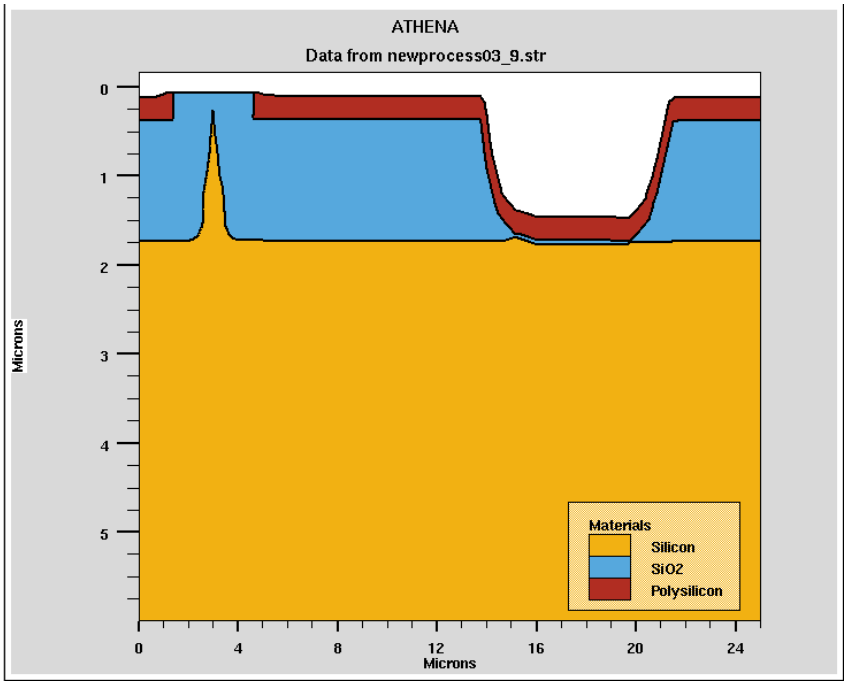


Figure 4-13. Simulation of CMP. Bump above the emitter is removed.

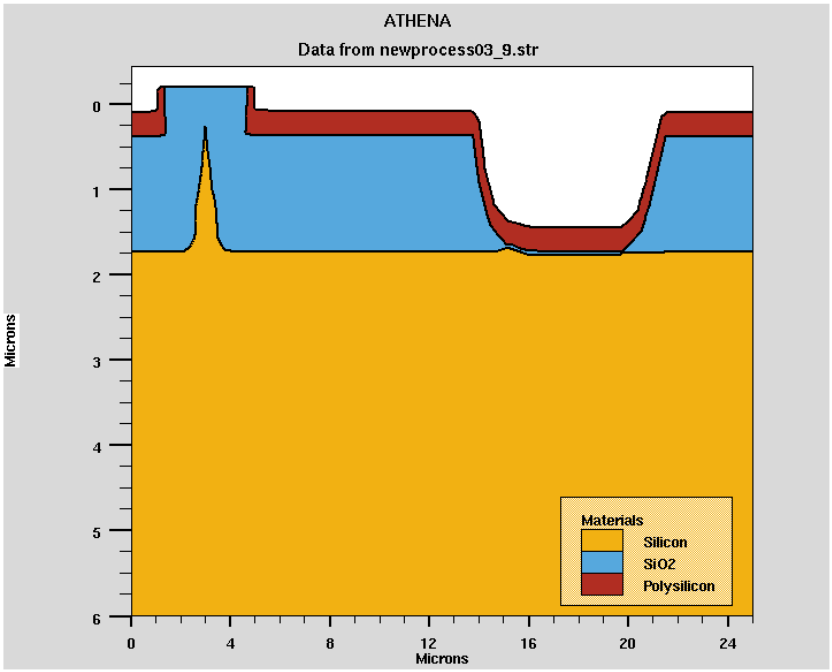


Figure 4-14. Simulation of CMP when it is under-polished.

The MOSFET gate was subsequently defined by MOSFET Gate Mask (Mask #4). Standard photolithography was employed followed by RIE plasma etching (Figure 4-2 e). The backside polysilicon and silicon dioxide layers were then stripped after the definition of FEA extraction gate and MOSFET gate. The removal of the oxide would allow us to electrically ground the substrate from the backside of the wafer. The front side of the wafer was covered by photoresist and the backside of the wafer was then etched by RIE to remove polysilicon followed by BOE to remove silicon dioxide. The reason to remove the backside polysilicon and oxide after CMP is to ensure the wafer is flat during the CMP process. If the oxide is removed right after the insulator deposition, we do not have to worry about the backside polysilicon since it is also conductive. However, it would cause stress-induced bowing of the wafer due to the relief of the stress at the backside. This would result in the non-uniform polishing by CMP.

The MOSFET source was next defined by MOSFET Source Mask (Mask #5) and was opened by removing silicon dioxide using BOE. In the preliminary experiment, RIE plasma etching was used for removing silicon dioxide layer. However, the polysilicon gate layer was also etched away because the selectivity of silicon to silicon dioxide is not

good enough for the thickness difference of 100-nm polysilicon layer and 500-nm silicon dioxide layer. Next, the MOSFET source was ion implanted with arsenic of $7x10^{15}$ cm^{-2} at 90 KeV (Figure 4-2 f). MOSFET source implantation was done before MOSFET Source Mask photoresist removal. Therefore, only the source region was doped with arsenic. To maintain the other implantation profiles, the arsenic implant was annealed in RTA at 1000 ^{o}C for 20 seconds. The simulation result and the SIMS profile of arsenic doping profile after RTA annealing are shown in Figures 4-15 and 4-16. The junction depth is about 0.25 μm. The spreading resistance analysis of the monitor wafer is shown in Figures 4-17 (a) and (b). Photoresist removal should be done carefully because it is difficult to remove due to high voltage and high dose implantation. Double piranha (piranha photoresist stripping and piranha cleaning) and plasma photoresist stripper were used to ensure the complete photoresist removal.

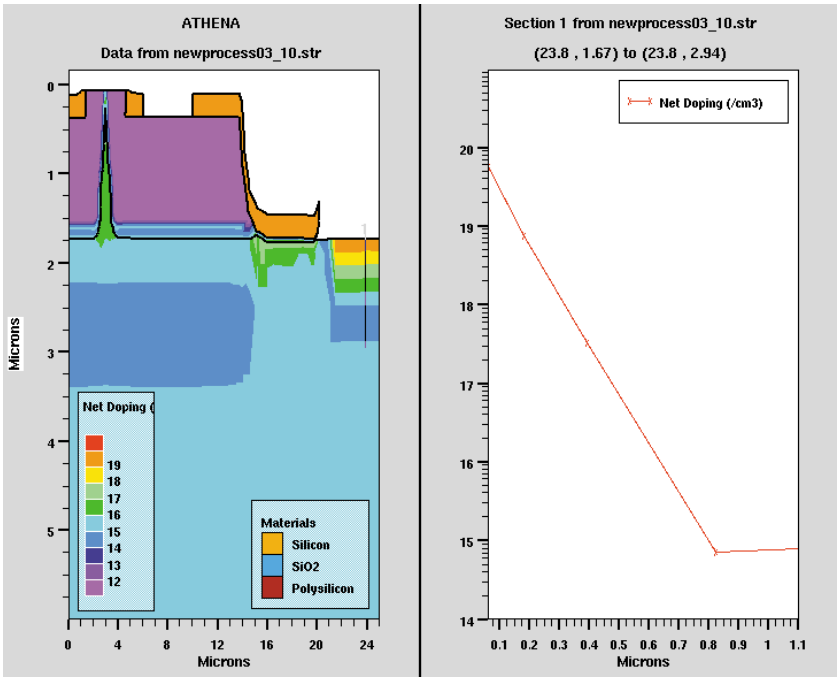


Figure 4-15. Simulation result of MOSFET source n+ implantation.

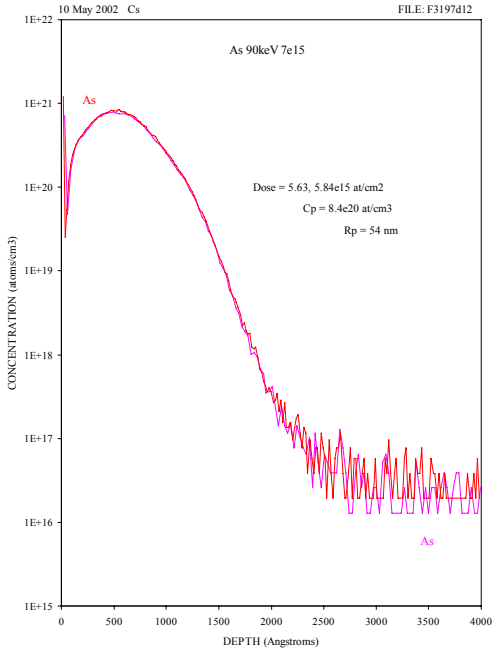
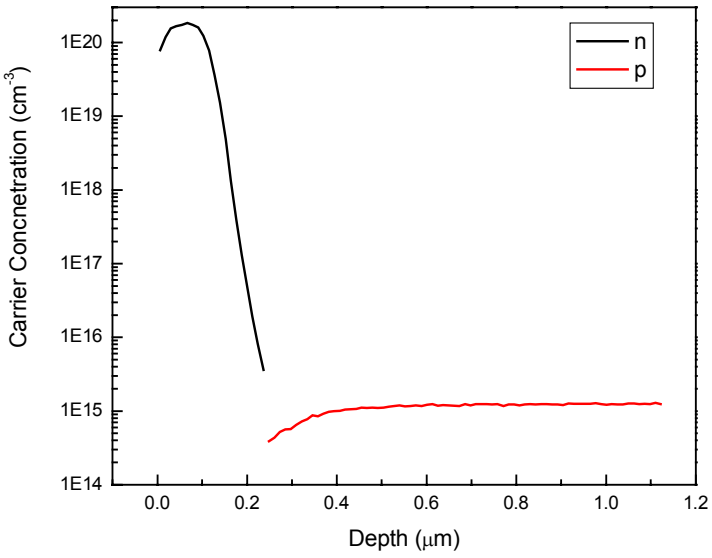


Figure 4-16. SIMS of the MOSFET source n+ implantation. Target phosphorous dose = $7x10^{15}$ cm^{-2}.

(a)



(b)

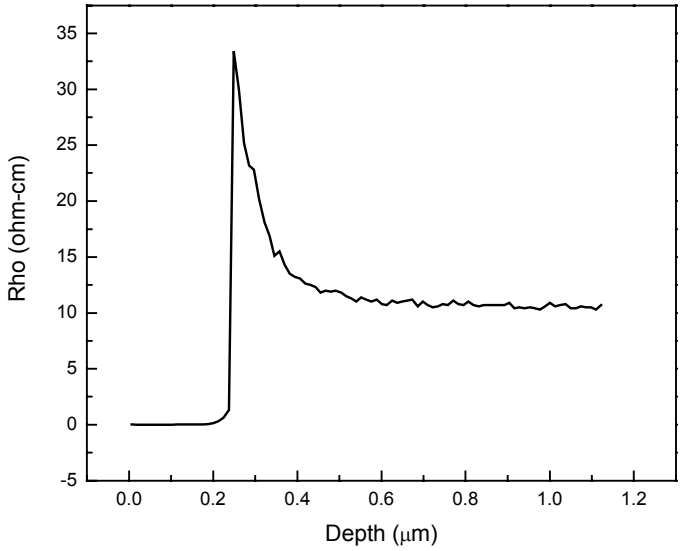


Figure 4-17. (a) Carrier concentration of the n+ doping wafer. (b) Spreading resistance.

Passivation Layer Deposition and Contact Hole Opening

A layer of 300 nm silicon dioxide was deposited on top of the wafer by LPCVD as a passivation layer. To make contact to the devices, contact hole was defined by Mask 8 and passivation oxide was removed by BOE.

Metal Layer Deposition and Contact Definition

Aluminum was next deposited by sputtering [4.30] as the metal contact after contact hole opening. Ti (10 nm) and TiN (50 nm) were deposited underneath the Al as diffusion barriers. The sputter machine is designed for 6-inch wafers and our 4-inch wafers need to be put on wafer-carriers (pucks) for deposition. The Al metal pads were defined by Metal Mask (Mask #6) with plasma etch using BCl_3 and Cl_2 [4.31] (Figure 4-2 g). This etch was done at a power of 350 W and a pressure of 20 mT. The gas flow of BCl_3 was

90 sccm and gas flow of Cl_2 was 130 sccm with 40 sccm of Ar and 8 sccm of He flowing. The etched wafers needed to go through water rinse to remove the chlorine materials on the photoresist before photoresist stripping because the chlorine would react with oxygen in the photoresist stripper and make it difficult to remove the photoresist. This also prevents the corrosion of Al by chlorine. After photoresist removal, the wafers were sintered in N_2 and H_2 at 400 ^oC for 30 minutes to enhance the metal contact with silicon substrate. Figure 4-18 shows the simulation result after passivation layer deposition, contact opening, and metal definition.

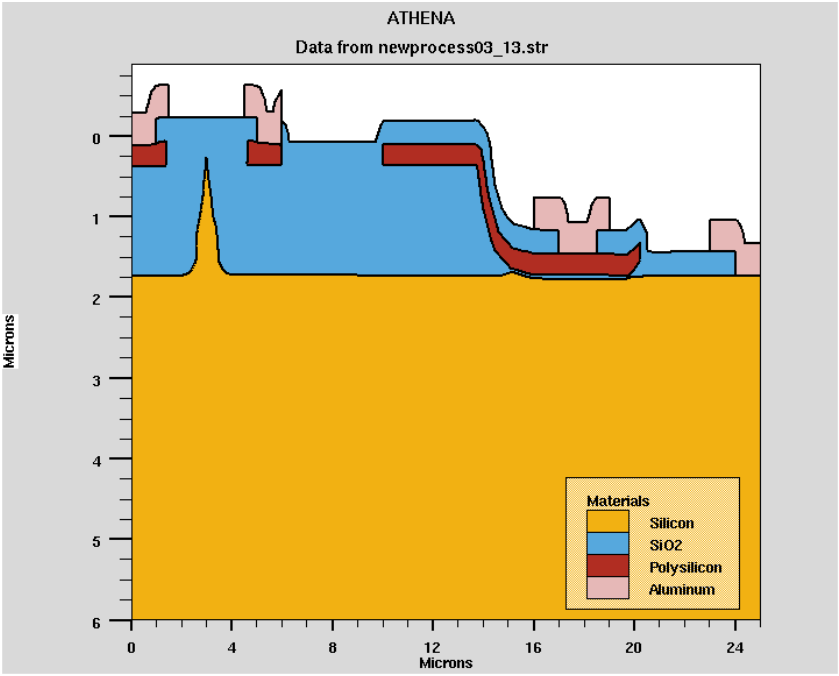


Figure 4-18. Simulation result after passivation layer deposition, contact opening, and metal definition.

Tip Exposure

The process was finally completed by exposing the silicon emitters. The wafers were defined with the Tip Exposure Mask (Mask #7) and dipped in BOE for several minutes to isotropically remove the sacrificial oxide and expose the tips (Figure 4-2 h). Until this point, the sharpened silicon emitters were protected by oxide from possible damage

during the subsequent processing steps after oxidation sharpening. We would like to expose the emitter as much as possible to increase the electron leakage path from the emitter though the oxide to the gate but without removing too much oxide under the extraction gate between two adjacent emitters due to undercut. Oxide is needed under the extraction gate for support. Figure 4-19 shows the simulation of the oxide etching. Photoresist was carefully removed using acetone, iso-propanol, and methanol sequentially for 5 seconds each instead of using plasma photoresist stripper. It is to avoid the plasma damage to the very sharp silicon tip region and the re-oxidation of the tip area due to oxygen in the plasma stripper. After stripping the photoresist, the wafer was investigated under the fluoroscope to make sure the photoresist was completely removed.

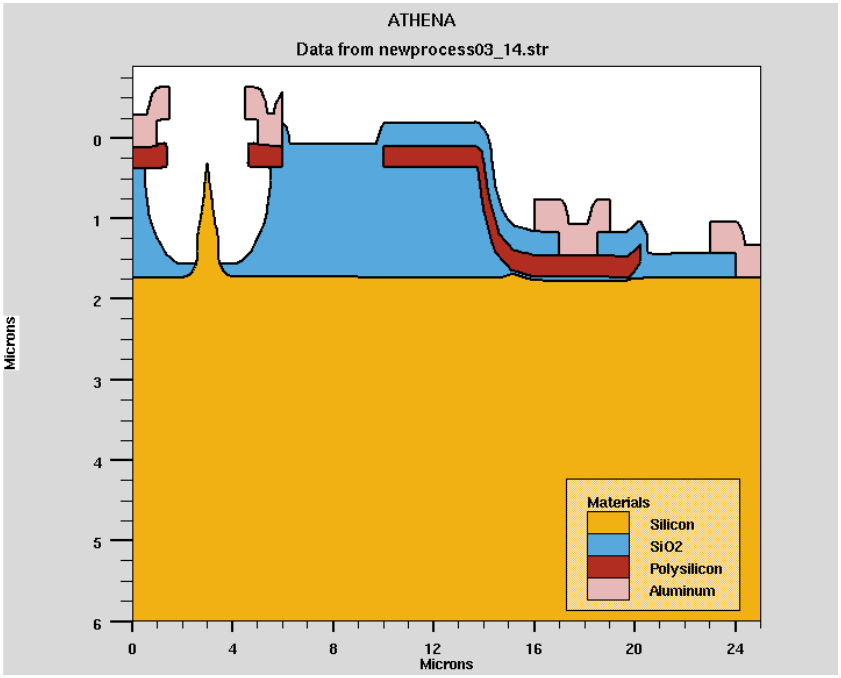


Figure 4-19. Simulation result of the final oxide etching to expose the emitter.

Completed Device

Figures 4-20 (a)-(d) show the optical microscope photos and TEM photos of the final structure of the LD-MOSFET/FEA device. The integrated device in Figure 4-20 (a) has

the FEA with 20x20 emitters and the LD-MOSFET with dimensions of 10 μm width, 100 μm length, and 100 μm drift length. The LD-MOSFET devices fabricated in this thesis are considered to be large compared to state of the art MOSFET devices. Figure 4-20 (b) shows the close-up of the FEA area. The circles are the polysilicon gates, and there is one emitter inside each of the polysilicon gate apertures. Figure 4-20 (c) is the TEM of the tower structured silicon emitter and Figure 4-20 (d) shows the lattice images of the tip area on the silicon emitter obtained by high-resolution TEM. In Figure 4-20 (d), the atomic lattice structure of the {111} face of silicon with a spacing of 3.13 A can be observed and the tip radius is approximately 3.5 nm. Our photolithography steps resulted in less than 1 μm misalignment, which is satisfactory for this thesis.

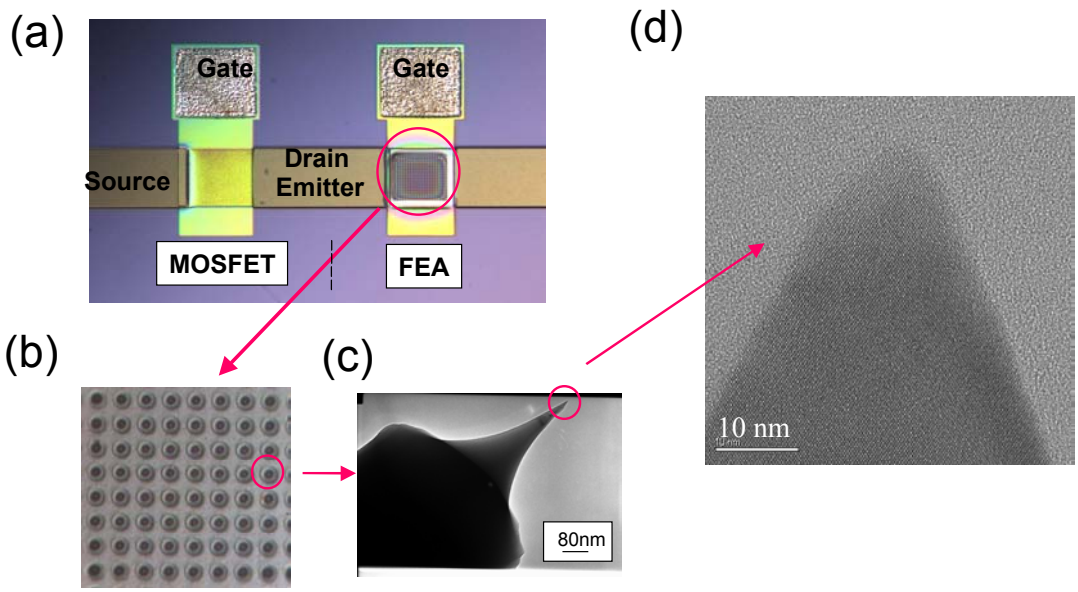


Figure 4-20. (a) Optical microscope photograph of the integrated device. (b) Close up of the FEA area. (c) TEM image of the silicon emitter. (d) Lattice image of the tip.

Suggestion for Future Process

This process has been modified several times to reach this final version. However, it is still not perfect. Here are the suggestions for modifying the process. First CMP needs to be optimized. In our lab, CMP is not uniform or well-controlled. Instead of one CMP step, multiple LTO deposition – CMP -- BOE etchback processes should be employed as stated in L. Dvorson's Ph. D. Thesis [4.32]. It should provide better control on the uniformity. Second, the emitter tips could be made taller to allow larger thickness of the insulator. This can improve the oxide breakdown, increase the electron leakage path along oxide surface, and reduce the FEA capacitance to increase the device switching frequency. Third, the uniformity of the silicon emitters could be further enhanced by more up to date photolithography and plasma-etching instruments. The uniformity of the silicon emitters is not good enough but it is already the limit of the current fabrication instruments.

Literature Comparison of Integrated Transistor/FEA Design

There are several papers in the literature that reported modulation of the field emission device by controlling the electron supply of the emission process with transistors. Yokoo *et al.* [4.5] reported integrating field emitter arrays with a commercially available MOSFET. Itoh *et al.* [4.2] and Lee *et al.* [4.33] integrated amorphous silicon thin film transistor (a-Si TFT) with the field emitter arrays, and Hashiguchi *et al.* [4.3] reported the integration of polycrystalline silicon thin film transistor (poly-Si TFT) with polycrystalline silicon field emitters. Moreover, Shimawaki *et al.* [4.4] reported a monolithic FEA integrated with a junction field effect transistor (JFET).

The integrated MOSFET/FEA devices reported by Itoh *et al.* [4.6-4.8, 4.16-4.17] are most similar to our structure and device design. However, the fabrication process is somewhat different. CMP was used in our process to open up the FEA extraction gate but plasma etch was used to define the extraction gate aperture for Itoh's devices. The

lightly doped drain for the integrated devices was shown in their more recent reports, and the implantation was done after the emitter formation. The emitters were not ion-implanted unlike our devices, the n well was first formed and the emitters were fabricated inside the well. We used dry etch to etch silicon isotropically to form silicon cones, but they used wet etch (ethlenediamine-pyrocathchol-water) to perform isotropic silicon etch. Oxidation sharpening was carried out at 900^{o}C to form 0.15 μm oxide, which was used as MOSFET gate oxide in their design. Some of the materials selections and the device dimensions for both MOSFET and FEA are also different. The diameter of the oxide mask for emitter formation is 0.5 μm for Itoh's device, and we have 1 μm diameter oxide mask. The doping materials and parameters for MOSFET threshold voltage adjustment and source/drain were different from our devices. Itoh used Nb as the FEA extraction gate electrode material, but the MOSFET gate electrode material remains polysilicon. The typical length of their MOSFET is 30 μm. The performance of their MOSFET-FEA devices will be presented and compared with our integrated LD-MOSFET/FEA devices in Chapter 6.

4.3 Chapter Summary

In this chapter, we introduced MOSFET as a voltage controlled current source to modulate current in field emission devices. We demonstrated how to integrate two individual devices and how this integrated device works. We also presented the design of the integrated MOSFET/FEA device with materials selection and device dimension selection. Lightly doped drain was adopted in the MOSFET device to enhance the breakdown voltage of the integrated devices. After presenting the design of the integrated device, the process flow for fabricating this integrated LD-MOSFET/FEA device was described in detail. This chapter was concluded with the photos of the completed device and presented some suggestions for future fabrication process modifications: optimize CMP, increase silicon emitter height, and enhance the silicon emitter uniformity by using other fabrication instruments. Our device structure was compared with the literature at the end of this chapter.

5. Field Emission Device Characterization and Analysis

Electrical characterization of FEA, MOSFET, and integrated LD-MOSFET/FEA were performed respectively. The details of the characterization results of FEA, a three-terminal device, are reported and analyzed in this chapter. Three terminal measurements refer to current and voltage measurements of the cathode, extraction gate and anode. The details of the characterization on the LD-MOSFET/FEA, a four-terminal device (cathode, FEA extraction gate, MOSFET gate, and anode) are presented in the following chapter.

5.1 Measurement Setup

Electrical characterization of the FEA devices was conducted in an ultra-high vacuum (UHV) chamber at pressures of about $2x10^{-9}$ Torr without bake out or field forming. Figure 5-1 is the photograph of the test station. The chamber on the left is the main test chamber, and the chamber on the right is the loadlock chamber. A high-resolution camera placed above the wafer stage outside the main test chamber magnifies the image of the wafer surface. The UHV chamber was mounted on a floating optical table. Instruments include four source-measure units (*Keithley 237*), capable of simultaneously sourcing voltage and measuring current; and *Labview* [5.1], a computer interface program that provides remote control of the instruments and collects the data over the GPIB. The configuration of the FEA test system is shown in Figure 5-2. The devices were probed on-wafer with very sharp tungsten probes, and the emitter current, anode current, and FEA extraction gate currents were monitored simultaneously. Electrical contact to the device was done with the aid of the microscope and micromanipulators. The backside of the wafer was in contact with the metallic stage, which was always grounded. Shielded tri-axial cables were used for all signals to minimize noise and interference. The anode was a nickel ball with a radius of 1 mm. The anode voltage was fixed at 1000 V and the

anode-substrate distance was fixed at 3 mm. In the preliminary emission characterization, a slab of Pt-coated silicon wafer was used for anode. Theoretically, the result of a silicon plate or a nickel ball should be the same. However, the size of the silicon plate was about 1 cm x 3 cm, and it was too large to be very close to the wafer surface (the minimum distance is 8 mm) because it would touch the other probes. Furthermore, the probe leads would pick up some electrons that were supposed to be collected by the silicon plate since the plate was above other probes. Therefore, the nickel ball instead of silicon slab was used as the anode for the electrical characterization. The measurements were performed in the dark to avoid photoemission.

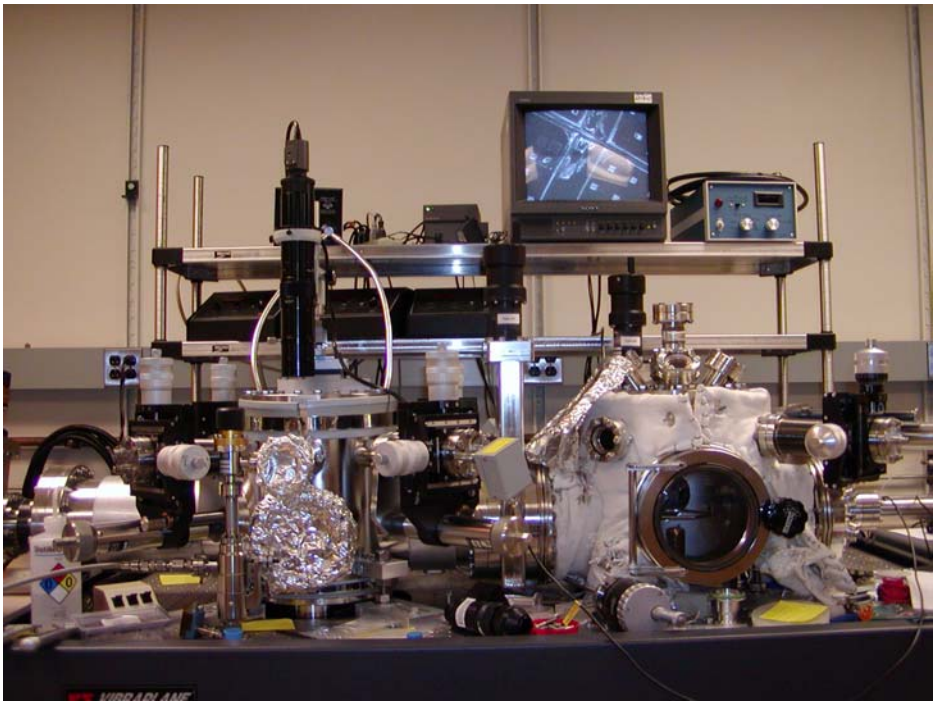


Figure 5-1. The photograph of the ultra high vacuum characterization station.

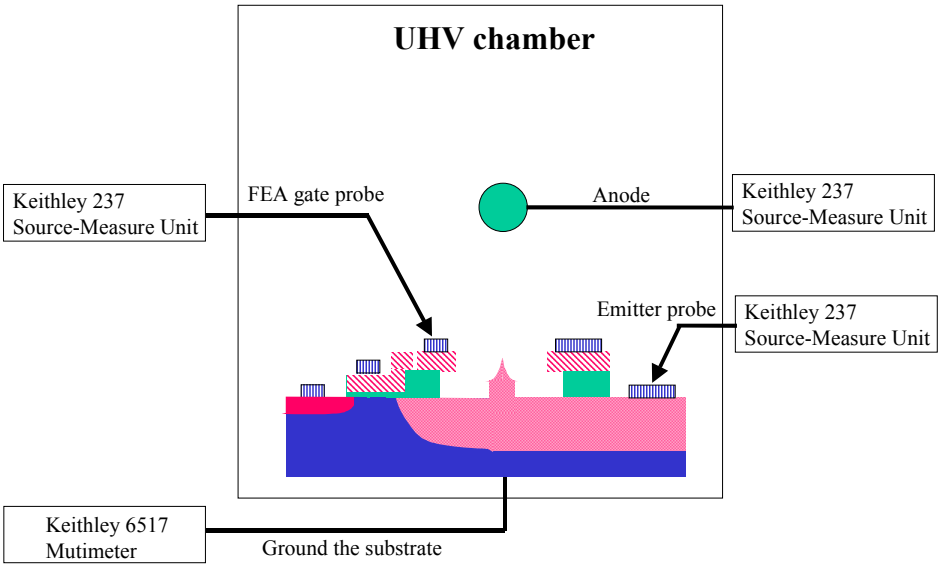


Figure 5-2. The schematic of the main testing chamber and the electronics setup.

The wafer went through a quick HF dip before loading into the vacuum chamber to remove the native oxide that is believed to affect the electron emission phenomena. The solution is 100:1 H_2O:HF and the etching rate of the native oxide is estimated as 10 nm/min. The etching time of the wafer is 30 seconds.

5.2 Device Characterization

Field Emission and Fowler-Nordheim Theory

21 up-down current-voltage (I-V) sweeps were performed on a 10x10 FEA in which the anode current was monitored as the FEA extraction gate voltage was swept up and down between 0 and 55 V as shown in Figure 5-3. The first ten and last ten sweeps recorded single measurement current values at each extraction gate voltage during the upward and downward ramps. The 11^{th} I-V sweep averaged 20 current data points at each extraction

gate voltage. These repeated I-V sweeps ensure that the result of this measurement could represent the field emission device behavior. We analyzed the I-V data obtained during the 11th I-V sweep. Figure 5-4 (a) shows the linear I-V characteristics of the 11th I-V sweep. This particular sweep was selected because it was in the middle of the 21 sweeps and the peak current of the 11th I-V sweep is between the highest and lowest peak currents, as shown in Figure 5-3. Furthermore, it was the only one sweep that averaged 20 data points at each voltage step. We defined the turn-on voltage as the voltage at which the current is 1 pA/tip, and the turn-on voltage for this device was 24V, which is consistent with the small tip radius and the relatively large gate aperture. Since the emitter tips in the array were 4 μm apart, the emitting area was 36x36 μm^2 in this 10x10 FEA. Using the Fowler-Nordheim (FN) equation shown below we extracted the parameters: a_{FN} and b_{FN}.

$$\mathbf{I} = \mathbf{a_{FN}}\, \mathbf{V_g^2}\, \exp\left(\frac{-\mathbf{b_{FN}}}{\mathbf{V_g}}\right) \tag{5.1}$$

FN analysis as shown in Figure 5-4 (b) gives the following parameters: a_{FN} = (3.14±0.3) x 10^{-7} and b_{FN} = 369±4. The parameters a_{FN} and b_{FN} can be obtained from the intercept and the slope of the FN plot which is a plot of $\ln(I/Vg^2)$ vs. 1/Vg. A similar analysis of the complete data set (all 21 sweeps) gave almost identical results: a_{FN} = (3.01±0.1) x 10^{-7} and b_{FN} = 370±1. With these relatively small difference between the 11th peak and the complete data set in the FN coefficients (a_{FN} and b_{FN}), it can be concluded that the 11th peak is quite representative of the device behavior. These small errors in both the 11th peak and the complete data set indicate that this device shows good Fowler-Nordheim characteristics. Using the ball-in-a-sphere electrostatic model, which assumes that the field factor $\beta = 1/r$ (r in cm), we deduced a tip radius of 6.9 nm from the slope of the FN plot under the assumption that the work function of n-type silicon is its electron affinity, χ=4.05 eV [5.2]. This tip radius value is similar to the tip radius at the peak of the distribution shown in Figure 3-11. α of 3.17×10^{-15} cm^2 can also be obtained by substituting constants A and B ($A = 1.54 \times 10^{-6}$ **and** $B = 6.87 \times 10^{7}$) in equation

$$a_{FN} = \frac{\alpha A \beta^2}{1.1\phi} \exp\left[\frac{B\left(1.44\ x10^{-7}\right)}{\phi^{1/2}}\right]. \tag{5.2}$$

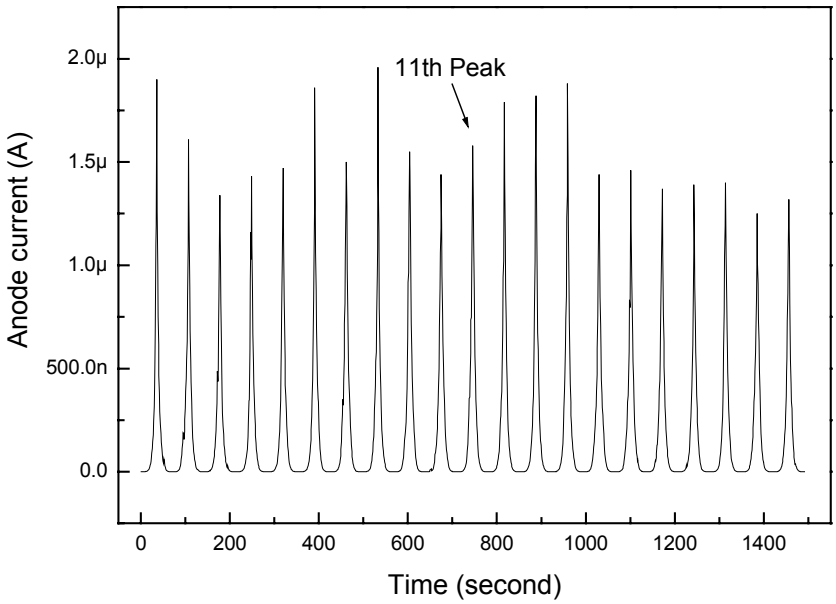
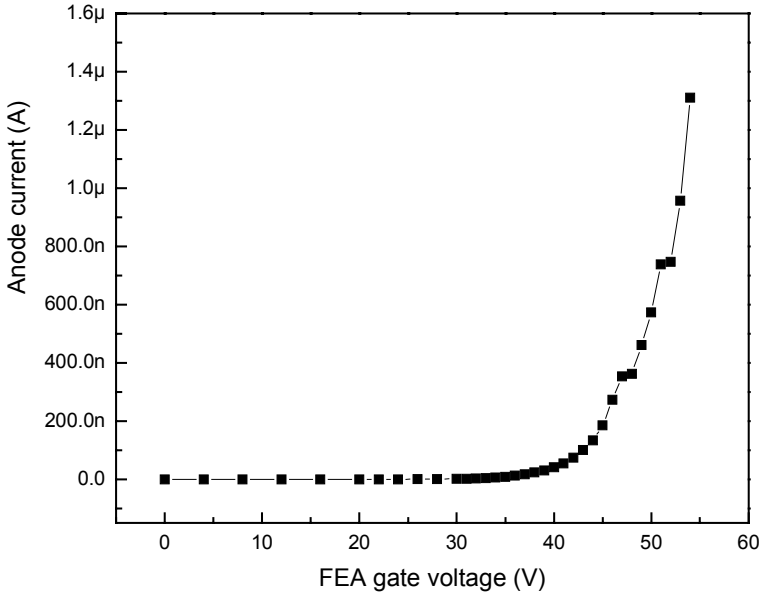


Figure 5-3. I-V sweeps of a 10x10 FEA.

(a)



(b)

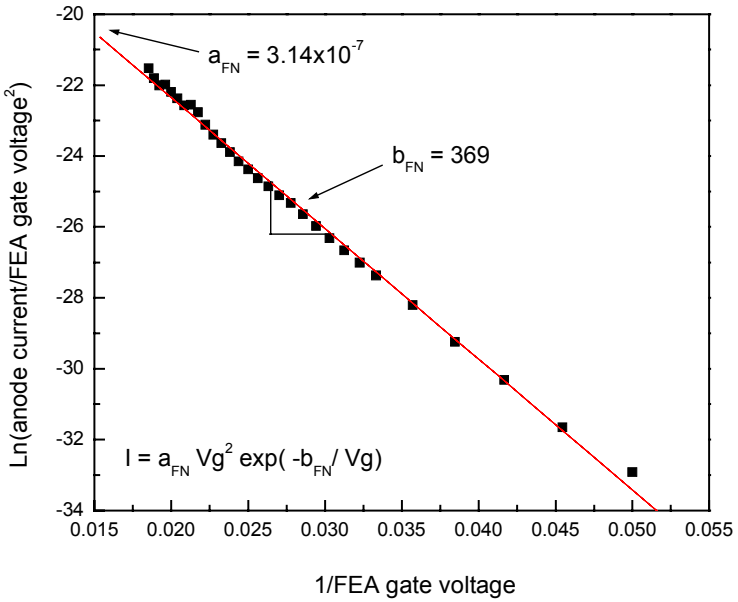


Figure 5-4. (a) Linear plot and (b) Fowler-Nordheim plot of the 11th peak in Figure 5-3.

However, "ball in a sphere" model is a relatively simplified electrostatic model. The above conclusion is rather misleading because a distribution of tip radius between 1.5 and 19 nm shown in Figure 3-11 would lead to big differences in the current emission capability and the slope of the FN plot, b_{FN}, obtained at each tip radius. It is expected in such cases that the lower end of the tip radius distribution would dominate. An analysis using an approach similar to the numerical simulation of the device structure conducted by Ding, *et al* [5.2] and Pflug [5.3] based on a two dimensional axial symmetric Laplace equation solver was executed. This method takes the actual structure of the field emitter into consideration. Using the following emitter structure parameters: emitter height = 1150 nm, oxide thickness = 790 nm, polysilicon gate thickness = 385 nm, gate aperture = 1030 nm, and emitter tip angle = 38^{o}, the simulation results are shown in the scatter data points in Figure 5-5. Fitting of the data indicates that the field factor β varies with tip radius r as $\beta = \frac{2.18x10^{6}}{r^{0.73}}$ (r in nm). Using this value of β we obtained from FN slope analysis, the corresponding tip radius is 1.8 nm. This analysis would suggest that the

smaller tip radius in the distribution shown in Figure 3-11 dominated the emission current, consistent with the work of Pflug [5.3] and Ding [5.2].

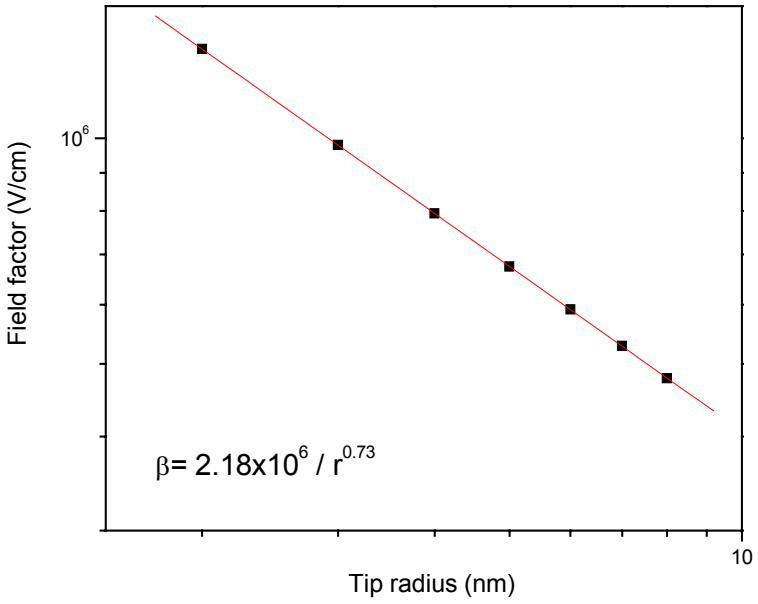


Figure 5-5. Dependence of field factor on the tip radius using numerical simulation.

Although it is known that the sharper the emitter, the higher the field that can be generated on the tip surface, it does not imply that we can get a larger current from the emitter tip by arbitrarily reducing the tip radius down to atomic scale [5.4]. The effective emitting area on the tip also decreases as the tip radius decreases. According to H. C. Lee *et al.*, the highest emission current we can get is from the emitter with tip radius of 1.2 nm. Therefore, the emitter tip radius fabricated by the process in this thesis is good enough for most of the field emission devices. It would be even better to narrow down the tip radius distribution. More experimental data sets are shown in Appendix G.

Temporal Stability

The principal sources of random variation of the emission current are the adsorption and desorption of foreign molecules on the emitter tip surface. Adsorption and desorption of molecules leads to variation in the electron transmission probability through fluctuations of the local work function (barrier height) or the local field factor (barrier width). The emission current is exponentially dependent on the changes in either barrier width or height; hence, small changes in work function lead to large changes in emission current. I-V sweeps were conducted in order to assess systematic distortions of the data collection [5.5]. The 21 up-down I-V sweeps mentioned in the last section were to assess emission current fluctuations due to relatively longer time constant absorption-desorption processes. The 11th I-V sweep was done in order to assess emission current fluctuations due to relatively shorter time constant adsorption-desorption processes. It was observed that the I-V curves from the up-sweep measurements are indistinguishable from the I-V curves from the down-sweep measurements as shown in Figure 5-6. The horizontal dotted line in Figure 5-6 shows that the voltages range over which a constant current of 0.1 μA could be obtained is ~ 4 V. In other words, a gate-emitter voltage variation of ~ 4 V is required in order to maintain a constant emission current of 0.1 μA, if there is fluctuation. Note that this ΔV = 4 V is what we observed for a 10x10 array. ΔV might be larger for a 1x1 array. This will be shown in the following section. This also implies that a voltage controlled current source such as a MOSFET in saturation requires a saturation region of at least 4 V. The work function difference corresponds to this voltage range could be obtained by solving the FN equation:

$$I = a_{FN} V^2 \exp(-b_{FN}/V), \tag{5.3}$$

$$a_{FN} = \frac{\alpha A \beta^2}{1.1\phi} \exp\left[\frac{B\left(1.44\ x10^{-7}\right)}{\phi^{1/2}}\right], \tag{5.4}$$

and

$$b_{FN} = \frac{0.95\, B \phi^{3/2}}{\beta}. \qquad (5.5)$$

Since I is constant (0.1 μA) and V changes as work function changes, by substituting

$$A = 1.54 \times 10^{-6},$$

$$B = 6.87 \times 10^{7},$$

assuming β = 1/r (r in cm) for simplicity,

r = 6.9 nm,

and α = 3.17 x 10^{-15} cm^2 from previous section,

the work function difference is 0.25 eV.

Noted that if we use $\beta = \frac{2.18x10^6}{r^{0.73}}$ (r in nm) and r =1.8 nm instead, β should be the same.

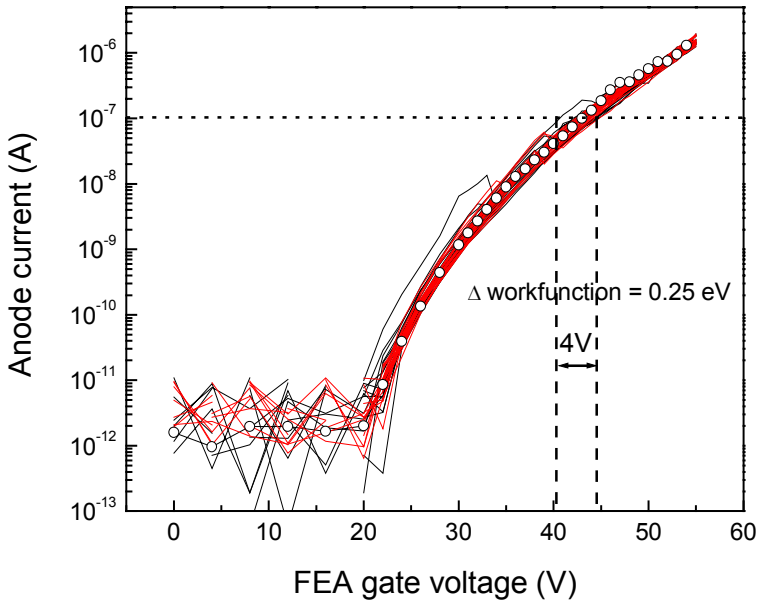


Figure 5-6. I-V characteristics of a 10x10 FEA. Lines are the up and down sweep measurements and the open circles represent the I-V sweep of the 11th peak. The voltage range over which a constant current of 0.1 μA could be obtained is ~ 4V. This voltage range corresponds to a work function difference of 0.25 eV.

The vertical dotted line in Figure 5-7 shows that the current range over which a constant voltage of 40 V could be obtained is form $2.5x10^{-8}$ A to $7.5x10^{-8}$ A ($\Delta I \sim 5x10^{-8}$ A). In other words, if the field emission device is operated at the extraction gate voltage of 40 V, the current variation could be at the range of $5x10^{-8}$ A over the operation time. This current range corresponds to a work function difference of 0.26 eV using the same method stated.

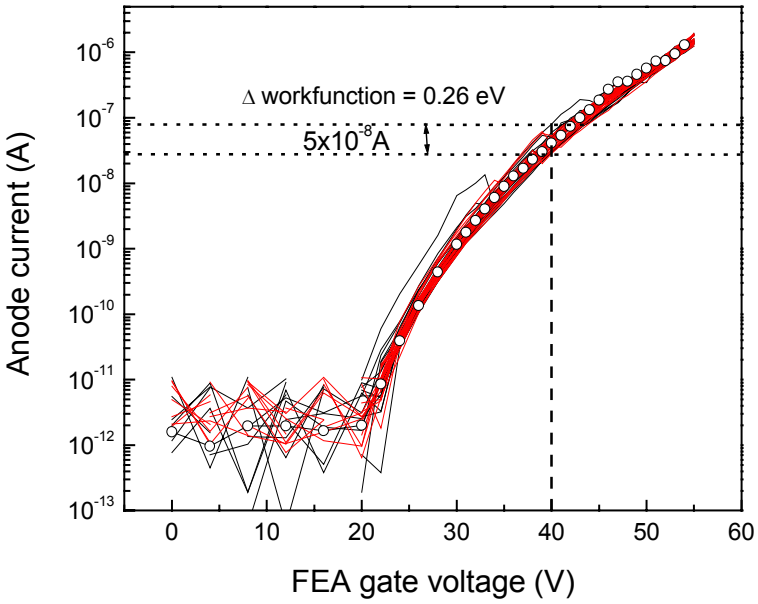


Figure 5-7. I-V characteristics of a 10x10 FEA. The current range over which a constant voltage of 40 V could be obtained is ~ $5x10^{-8}$ A. This current range corresponds to a work function difference of 0.26 eV.

The emission current of a 10x10 FEA at a constant FEA extraction gate voltage was monitored for one hour to demonstrate the current fluctuation over time. Figure 5-8 shows that the FEA has low emission current and large current fluctuation as turned on. The current increases with time and becomes more stable after operating the device for more than 10 minutes. The first 10 minutes of this anode current monitoring is known as the burn-in period [5.5]. The emission current is low because contamination particles or residual oxide on the emitter surface increase the work function. It is believed that the contamination and residual oxide on the emitters are removed or desorb in this burn-in

period. After the burn-in period, the anode current would increase and stabilize with the removal of contamination particles and residual oxide. Current fluctuations after the burn-in period are due to the absorption and desorption of the residual gas molecules in the UHV Chamber. The burn-in period duration depends on the cleanness of the emitter surface. The FEA device only goes through the burn-in period once if it stays in the UHV system. The HF dip before loading the wafer into the UHV chamber also helps to reduce the burn-in time. Over a 60-minute period, emission current fluctuation $\Delta I/I$ of this 10x10 FEA is 29.3%, where $\Delta I/I$ is extracted as the standard deviation of current/mean current. If the first 10 minutes is excluded, the emission current fluctuation drops to 19.8%. In this thesis, the anode current was collected after the burn-in period if not specified.

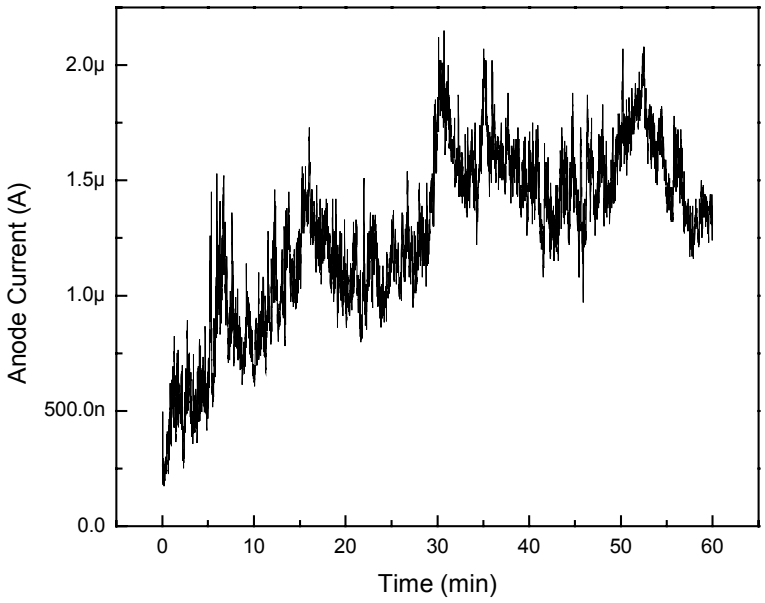


Figure 5-8. Anode current of a 10x10 FEA was monitored in a 60-minute period.

We also monitored the anode currents at three different current levels for 10 minutes as shown in Figure 5-9. The current fluctuations are 18.3%, 11.8%, and 16.9% as the average anode currents are 464 nA, 1.21 µA and 1.76 µA. The FEA extraction voltages

were biased at 50 V, 53.5 V, and 55 V, respectively. The current data was taken about once per 0.5 second.

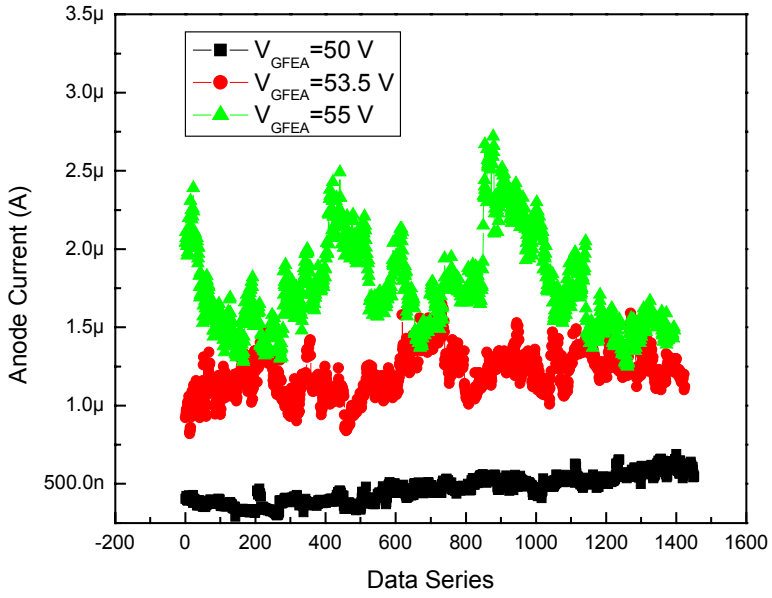


Figure 5-9. Anode current of a 20x20 FEA was monitored in a 10-minute period at three different current levels.

The current data distribution was re-plotted from current-voltage characteristics as shown in Figure 5-10. Work function distribution was obtained qualitatively in this measurement as shown in Figure 5-11. The work function was extracted using similar method as presented earlier in this section by solving the FN equation:

$$I = a_{FN} V^2 \exp\left[-b_{FN}/V\right], \tag{5.6}$$

$$a_{FN} = \frac{\alpha A \beta^2}{1.1\phi} \exp\left[\frac{B\left(1.44\ x10^{-7}\right)}{\phi^{1/2}}\right], \tag{5.7}$$

and

$$b_{FN} = \frac{0.95\, B\, \phi^{3/2}}{\beta}. \tag{5.8}$$

Since V_{GFEA} is constant and different currents correspond to different work function, by substituting

$$A = 1.54 \times 10^{-6},$$

$$B = 6.87 \times 10^{7},$$

assuming $\beta = 1/r$ for simplicity,

$$r = 6.9 \text{ nm},$$

and $\alpha = 3.17 \times 10^{-15}$ cm^2 from previous section, we can obtain the corresponding work function.

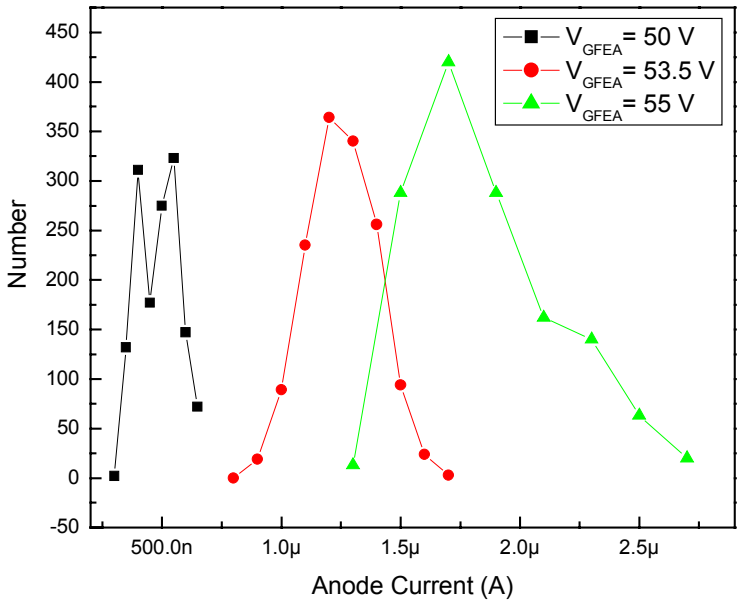


Figure 5-10. Anode current distribution as the anode current data of a 20x20 FEA was taken once per 0.5 second in a 10-minute period at three different current levels.

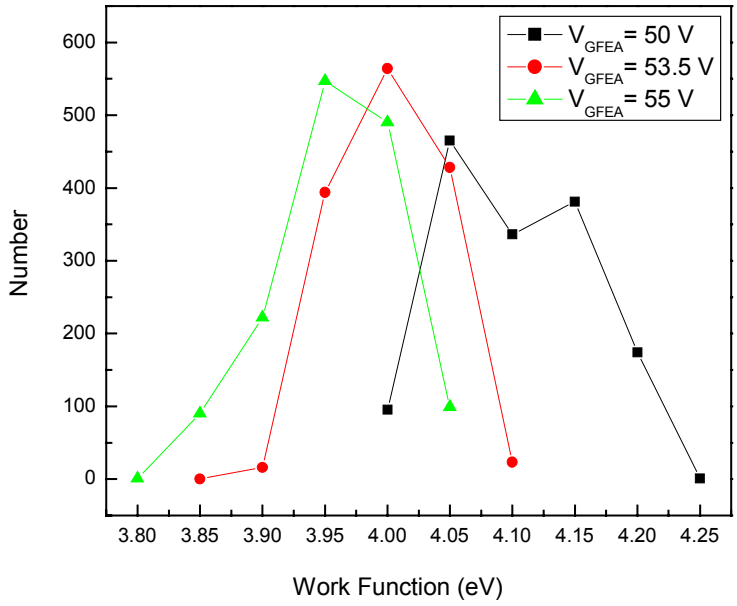


Figure 5-11. Work function distribution as the anode current data of a 20x20 FEA was taken once per 0.5 second in a 10-minute period at three different current levels.

More accurate work function distribution could be extracted by using the tip distribution. The work functions at three different gate voltages all show the Gauss-like distribution. It is noticed that the work function was lowered when the extraction gate voltage was increased. Theoretically, the work function should be the same if there is no surface change because the measurement was done on the same device with unchanged emitter structure. The shift of the work function might due to heat induced desorption. The emitter was slightly heated up when the extraction gate voltage was increased.

Three average anode currents of 464 nA, 1.21 μA and 1.76 μA correspond to three average work function 4.06 eV, 3.96 eV, and 3.92 eV, respectively. As we discussed in Chapter 2, current fluctuates with work function changes following the equation:

$$\frac{\Delta I}{I} = \frac{\partial I / \partial \phi}{I} \times \Delta\phi = \left[\frac{-1}{\phi} - \frac{0.72 \times 10^{-7} B}{\phi^{3/2}} - \frac{1.425 \phi^{1/2} B}{\beta V} \right] \times \Delta\phi \,. \qquad (5.9)$$

Current fluctuations at three current levels are 18.3%, 11.8%, and 16.9%. By substituting three different ϕ, r = 6.9 nm, and $\beta \sim 1/r$, $\frac{\partial I / \partial \phi}{I}$ at three current levels are -3.57, -3.39, -3.32, and averaged $\Delta\phi$ are 0.051 eV, 0.035 eV, and 0.051 eV, respectively.

Effect of Gasses

Field emission device is a vacuum device, and the required operating vacuum level is usually up to 10^{-10} Torr. The absorption and desorption of the gas molecules could change the work function, therefore, the emission current [5.6-5.12]. The I-V characteristics of the field emission device were done in different gas conditions to study how the gas molecules affect the emission current.

The response of emission current to hydrogen gas is shown in Figure 5-12. Hydrogen was admitted into the UHV chamber through a leak valve while the ion pump was turned off. Hydrogen was continuously admitted into the chamber while the diffusion pump was used to keep the pressure at a desired level. The anode current of the FEA device was first monitored at $5x10^{-8}$ Torr without hydrogen. Residual gas molecules in the UHV chamber randomly absorbed/desorbed at the emission surface and caused the fluctuation of emission current. Next hydrogen was introduced into the system at $1x10^{-7}$ Torr followed by $5x10^{-7}$ Torr. The FEA emission current was lower in the presence of hydrogen because there were more hydrogen molecules sticking to the emission surface, increasing the work function and hence reducing the emission current. Then hydrogen gas supply was turned off and the vacuum level was brought back to $5x10^{-8}$ Torr. However, the emission current remained low because the gas molecules stayed at the emission surface. The emission current level was restored after stopping the measurement and restarting. It is believed that the molecules are polarized by the electrostatic field and those gas molecules are released from the emission surface only after turning off the electric field. Sometimes the emission current level would be restored only after turning the extraction gate voltage to higher than the original value

then bringing the voltage back to the original value. This might be due to the heating-induced desorption [5.5].

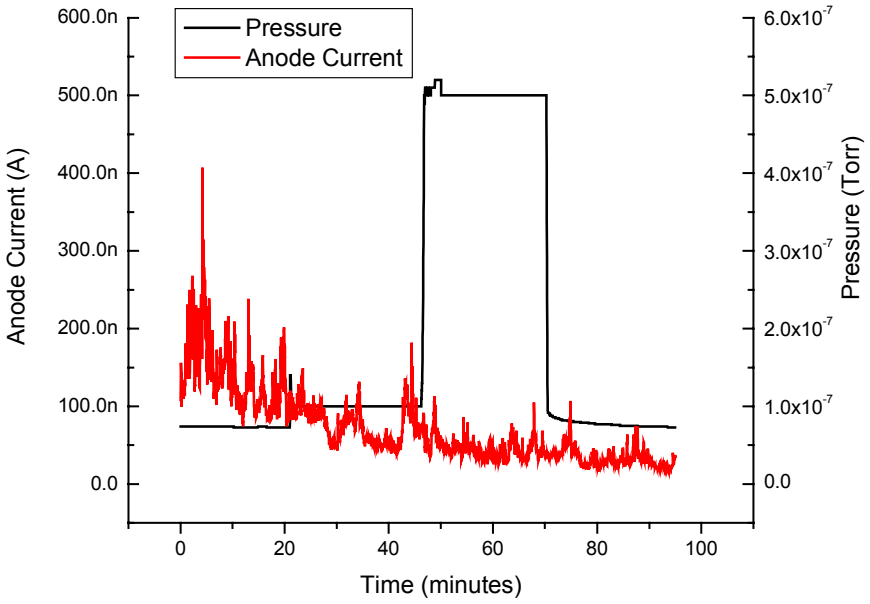


Figure 5-12. Anode current stability of a FEA with the exposure of hydrogen.

The same characterization was repeated on the devices with nitrogen and argon as shown in Figure 5-13 (a) and (b). The results are similar to the characterization with hydrogen. However, the lowering of the current is not as obvious in argon. It is speculated that argon is more difficult to polarize because argon is a single inert atom instead of a diatomic molecule as hydrogen or nitrogen. Therefore, the argon atoms have difficulty sticking to the emitter surface and the emission current is not affected by argon dramatically as with hydrogen and nitrogen. It is noted that the anode currents in three sets of measurements all have delayed responses to the pressure change.

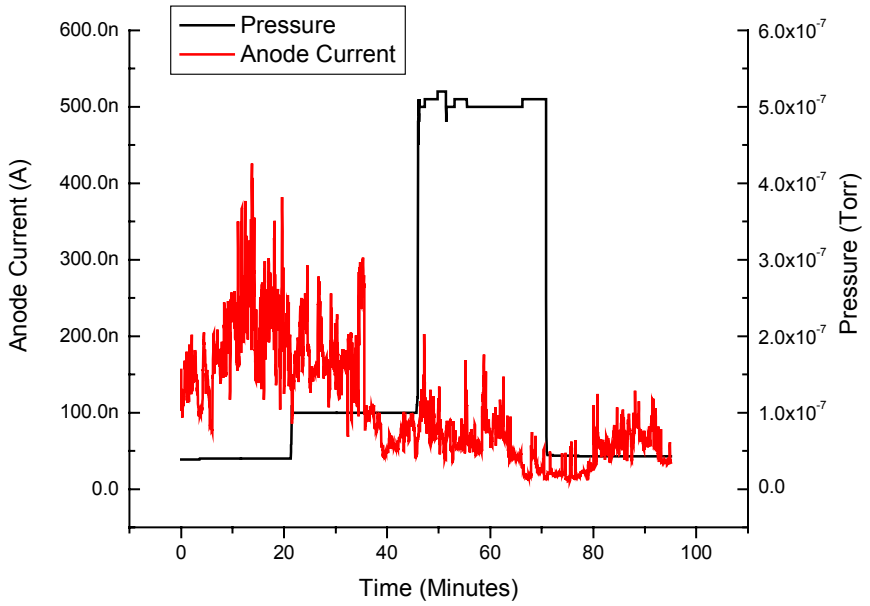


Figure 5-13. (a) Anode current stability of a FEA with the exposure of nitrogen.

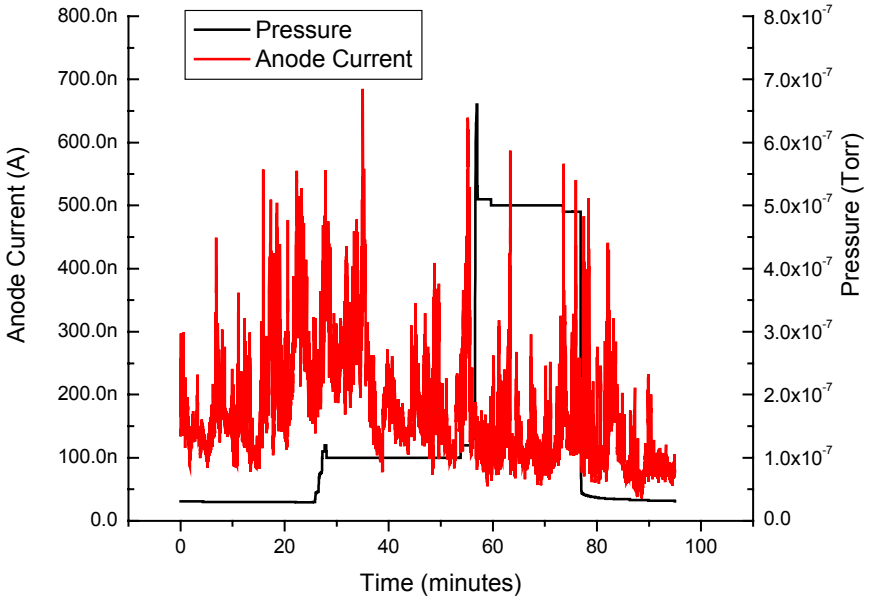


Figure 5-13. (b) Anode current stability of a FEA with the exposure of argon.

The average current and the current fluctuations (ΔI/I) in three different gas conditions are summarized in Table 5-1. As discussed in Chapter 2,

$$\phi(t) = \phi_0 + \Delta\phi(t) \tag{5.10}$$

$$\Delta\phi(t) = 2\pi P_i N_s \theta(t) \tag{5.11}$$

θ (t) will change if there is a pressure change in the system. After the pressure is stabilized and t is long enough, θ (t) will reach an equilibrium value,

$$\theta_{eq} = \frac{k_a P}{k_d + k_a P}. \tag{5.12}$$

The equilibrium θ is usually obtained within several minutes [5.12]. Equilibrium θ increases with pressure, and P_i, N_s and k_a, k_d are unchanged in the same device and gas molecules, and ϕ increases with pressure. Therefore, the average emission current decreases with pressure as shown in Figure 5-14. It is derived in Chapter 2 that the current fluctuation changes with work function changes:

$$\frac{\Delta I}{I} = \left[\frac{-1}{\phi} - \frac{0.72\times10^{-7} B}{\phi^{3/2}} - \frac{1.425\phi^{1/2} B}{\beta V} \right] \times \Delta\phi \tag{5.13}$$

Assuming ϕ = 4.05 eV at 3×10^{-8} Torr as a reference point, β ~ 1/r and r = 6.9 nm for simplicity, ϕ at different gas pressure could be extracted out. The FEA extraction gate voltages are 46 V and 45 V respectively in hydrogen and nitrogen experiments. The extracted ϕ with hydrogen and nitrogen are summarized in Table 5-2. Using the equation (5.13), we can extract the work function difference according to the current fluctuation shown in Table 5-1. The extracted average Δϕ with hydrogen and nitrogen are also summarized in Table 5-2.

Table 5-1. Average current and current fluctuation (ΔI/I) in four pressure conditions with H_2, N_2, and Ar.

Gas (Torr)	$3x10^{-8}$	$1x10^{-7}$	$5x10^{-7}$	$3x10^{-8}$
Average Current with H_2 (A)	$1.41x10^{-7}$	$7.14x10^{-8}$	$4.36x10^{-8}$	$3.02x10^{-8}$
Average Current with N_2 (A)	$1.93x10^{-7}$	$1.27x10^{-7}$	$5.95x10^{-8}$	$5.15x10^{-8}$
Average Current with Ar (A)	$2.08x10^{-7}$	$1.24x10^{-7}$	$2.62x10^{-7}$	$1.64x10^{-7}$
Current Fluctuation with H_2	0.30	0.31	0.26	0.30
Current Fluctuation with N_2	0.32	0.48	0.44	0.46
Current Fluctuation with Ar	0.32	0.37	0.36	0.50

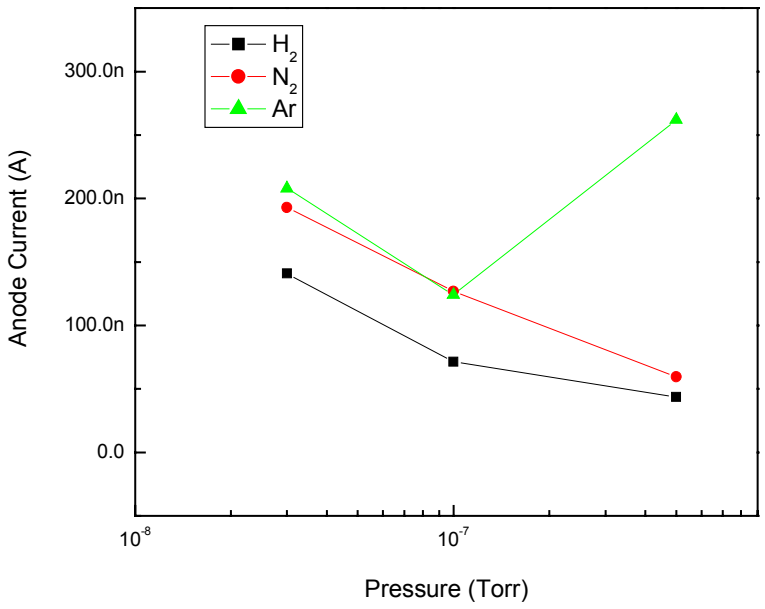


Figure 5-14. Anode current response to the chamber pressure.

Table 5-2. Extracted average work function (ϕ) and work function fluctuation ($\Delta\phi$) in three pressure conditions with H_2 and N_2.

Gas (Torr)	$3x10^{-8}$	$1x10^{-7}$	$5x10^{-7}$
ϕ with H_2 (eV)	4.05	4.18	4.23
ϕ with N_2 (eV)	4.05	4.14	4.23
$\Delta\phi$ with H_2 (eV)	0.08	0.08	0.07
$\Delta\phi$ with N_2 (eV)	0.08	0.12	0.11

Spatial Uniformity

The anode currents of the FEA devices at different wafer locations were monitored while the FEA gate voltage was swept from 0 to 65 V as shown in Figure 5-15. Die 44 (the die is on row 4 and column 4 of the wafer) is at the left side of the wafer, die 54 is at the center, and die 64 is at the right side. The FEA in die 44 is 1 cm apart from the one in die 54. It is concluded that even with every careful fabrication process, the field emission IV characteristics, such as turn-on voltage, are still different in the FEAs from die to die. It is speculated that the variation would be even larger in different FEA devices from wafer to wafer.

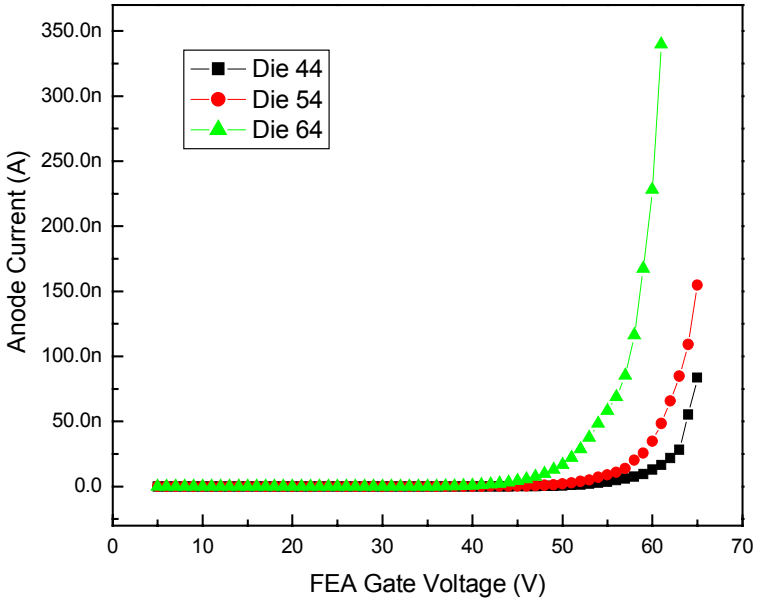


Figure 5-15. Spatial emission current non-uniformity in the FEA devices at different positions on the wafer.

As we discussed in Chapter 2, the current varies with radius of the emitter tip by the following equation:

$$\frac{\Delta I}{I} = \frac{\partial I / \partial r}{I} \times \Delta r = \left[\frac{-2}{r} - \frac{0.95\phi^{3/2} B}{V} \right] \times \Delta r \tag{5.14}$$

Taking V_{GFEA} = 60 V for example, using die 54 as a reference point, and assuming average r = 6.9 nm in the emitters in die 54 for simplicity and ϕ = 4.05 eV, average r of 2.17 nm is extracted in die 64 from the above equation, since Δr = 4.73 nm when ΔI = 200 nA (absolute value of I_{64}-I_{54}). Similarly, the average r of 7.43 nm is extracted in the emitters in die 44. This shows that within a small distance on the wafer, the average tip radius varies within several nanometers but it results in significant non-uniformity of emission current.

Different Array Sizes

There are three field emitter array sizes in our LD-MOSFET/FEA: 1, 10x10 and 20x20. For most of the characterization, 10x10 FEAs were used. In this section, the I-V characteristics of three different array sizes of FEAs are presented. 21 up-down I-V sweeps were performed on the FEAs in which anode currents were monitored while the FEA extraction gate voltage was swept up and down as shown in Figures 5-16 (a), (b) and (c). The method of taking the data was the same as that in the previous section. It is noted that the anode current is low and the current fluctuation is large in the single emitter while the extraction gate voltage was swept between 0 and 87 V. The turn on voltage of the single emitter (~ 65 V) is much larger than the ones in 10x10 and 20x20 FEAs and it requires much higher extraction gate voltage to obtain noticeable anode current. The gate leakage is huge due to high extraction gate voltage. It is concluded that the single emitter is too blunt and too short and below the gate due to over-etching during the isotropic silicon etch process leading to over-oxidation during the sharpening process. For the 10x10 and 20x20 FEAs, the extraction gate was swept between 0 and 60 V. Theoretically, the anode current of the 20x20 FEA should be four times larger than that of the 10x10 FEA assuming every tip emits equally. However, as shown in Figures 5-16 (b) and (c), the peak of the anode current of the 10x10 FEA is a little larger than that of the 20x20 FEA while the turn on voltage is almost the same. Both of the gate leakage currents are small enough to be ignored. As we mentioned in the previous chapter, the sharper emitters dominate the emission process. It is concluded that the number of sharper emitters is larger in the 10x10 FEA than in the 20x20 FEA due to non-uniform emitter fabrication. Figures 5-17 (a), (b), and (c) show the FN analysis of the 11^{th} up-sweep IV curves of three different array sizes. Since b_{FN} is proportional to emitter tip radius, these extracted b_{FN} in Figures 5-17 (a)-(c) confirm that the tip radius of the single emitter is blunt compared with the dominate emitters in the 10x10 and 20x20 FEAs. The tip radius of the emitters that dominate the emission current in the 10x10 FEA is a bit smaller than that of the ones in the 20x20 FEA.

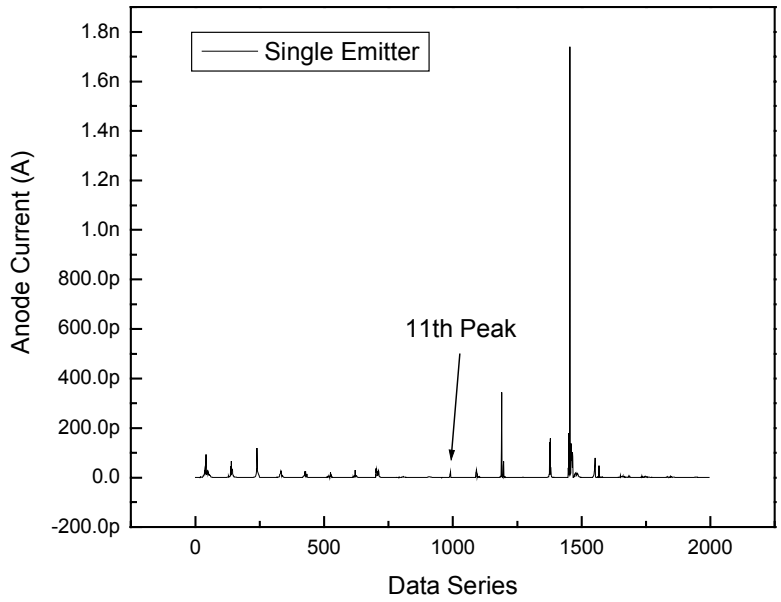


Figure 5-16. (a) Anode current of a single emitter as a function of gate voltage with the extraction gate voltage swept between 0 and 87 V. The lower axis represents 21× repeated up and down voltage sweeps (0 V—87 V—0 V). The peaks (current maximum) correspond to gate voltage of 87 V while the troughs (current minimum) correspond to gate voltage of 0 V. For sweep Nos. 1–10 and 12–21, a single current measurement was taken at each gate voltage while for sweep No. 11, 20 current measurements were taken and averaged at each gate voltage.

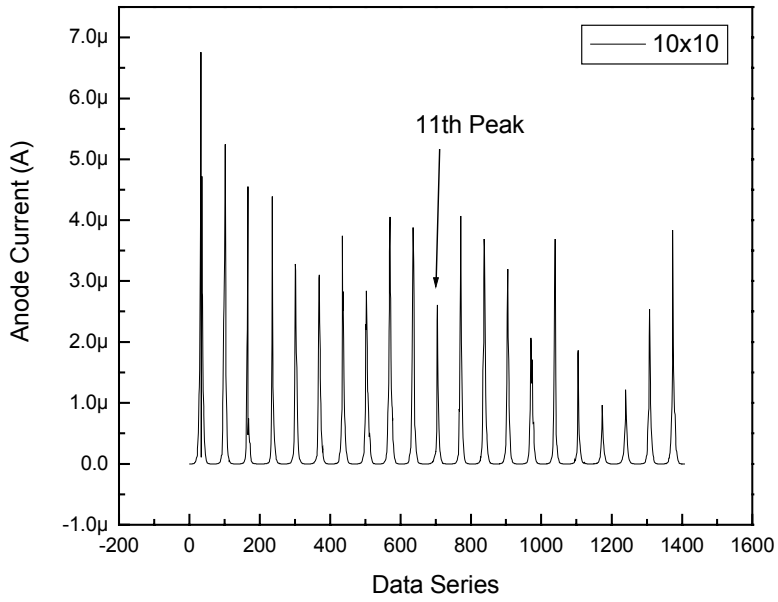


Figure 5-16. (b) Anode current of a 10×10 FEA as a function of gate voltage with the extraction gate voltage swept between 0 and 60 V. The lower axis represents 21× repeated up and down voltage sweeps (0 V—60 V—0 V). The peaks (current maximum) correspond to gate voltage of 60 V while the troughs (current minimum) correspond to gate voltage of 0 V.

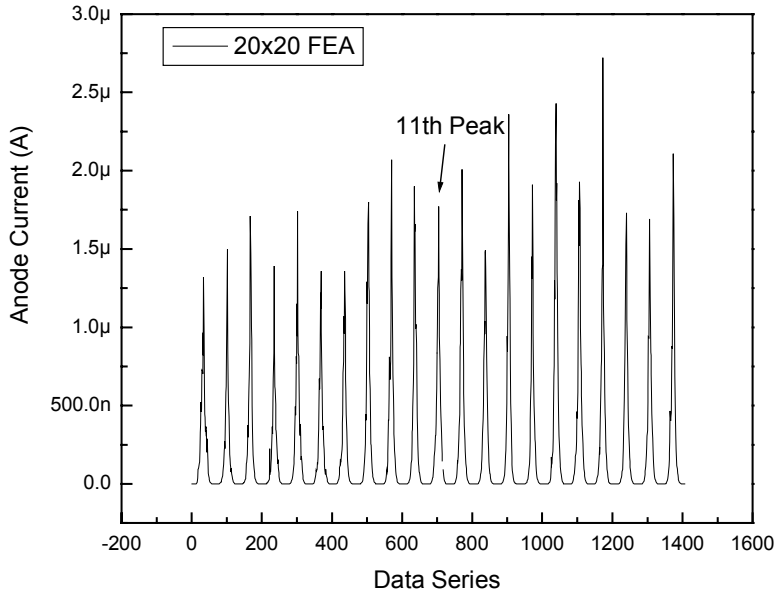


Figure 5-16. (c) Anode current of a 20×20 FEA as a function of gate voltage with the extraction gate voltage swept between 0 and 60 V. The lower axis represents 21× repeated up and down voltage sweeps (0 V—60 V—0 V). The peaks (current maximum) correspond to gate voltage of 60 V while the troughs (current minimum) correspond to gate voltage of 0 V.

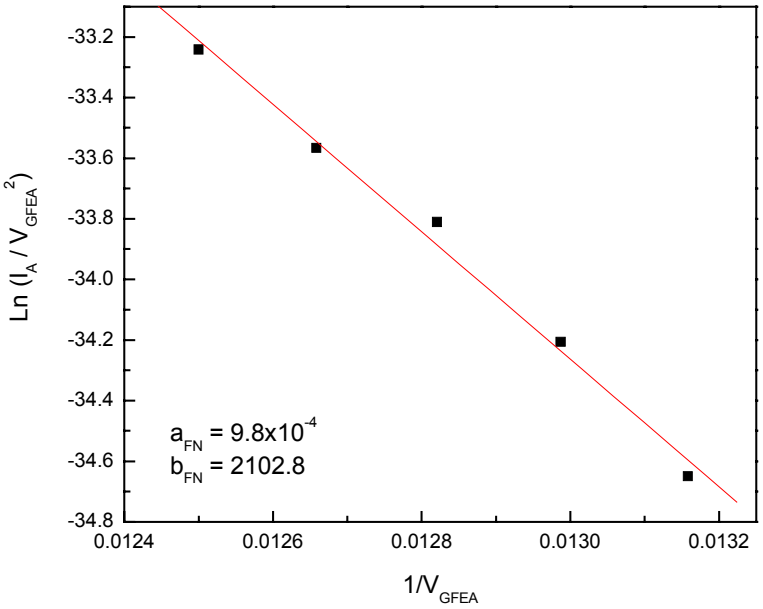


Figure 5-17. (a) FN plot of the 11th peak in Figure 5-16 (a).

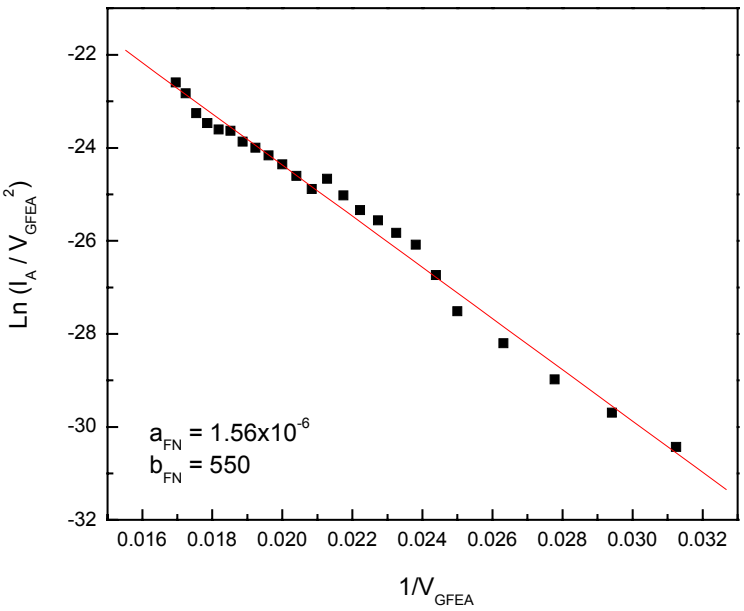


Figure 5-17. (b) FN plot of the 11th peak in Figure 5-16 (b).

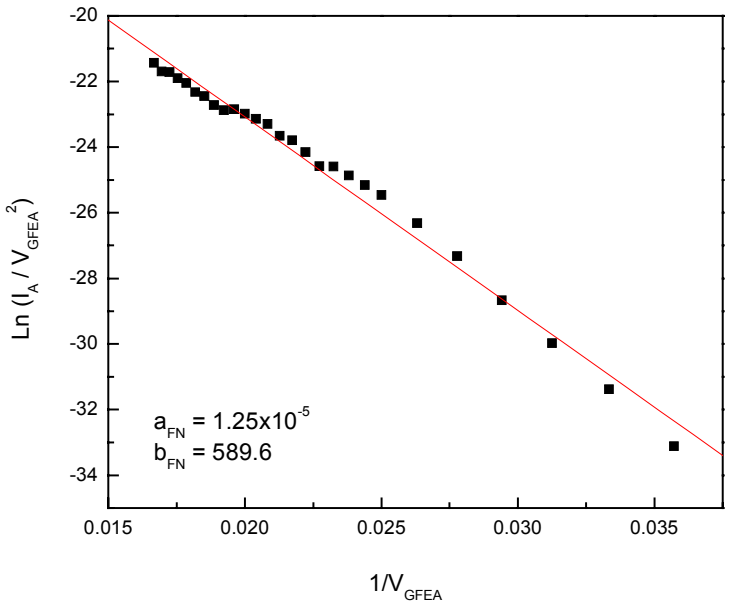


Figure 5-17. (c) FN plot of the 11th peak in Figure 5-16 (c).

Figures 5-18 (a), (b), and (c) show the voltage spreads at constant current levels in the single emitter, 10x10 FEA, and 20x20 FEA. The single emitter has rather large voltage spread of 24 V even at very small current level (0.01 nA). The voltage spreads in the 10x10 FEA and 20x20 FEA are 8 V and 5 V at anode current of 100 nA. The source of the voltage spread at a constant current level is similar to that of the current fluctuation at the constant voltage biased, which is due to the residual gas molecule adsorption/desorption on the emitter surface that leads to work function changes. When there is only one emitter, the work function changes to $\phi_0+\Delta\phi$ as the emitter adsorbs the gas. The work function changes back to ϕ_0 as the emitter desorbs the gas. When the emitter array sizes are larger, the probability of adsorption/desorption on the individual emitters still the same. However, the averaged standard deviation of the probability distribution between $n(\phi_0+\Delta\phi)$ and $n\phi_0$ is smaller when the emitter number (n) is larger. Therefore, statistically the voltage spread is smaller when the array size is larger.

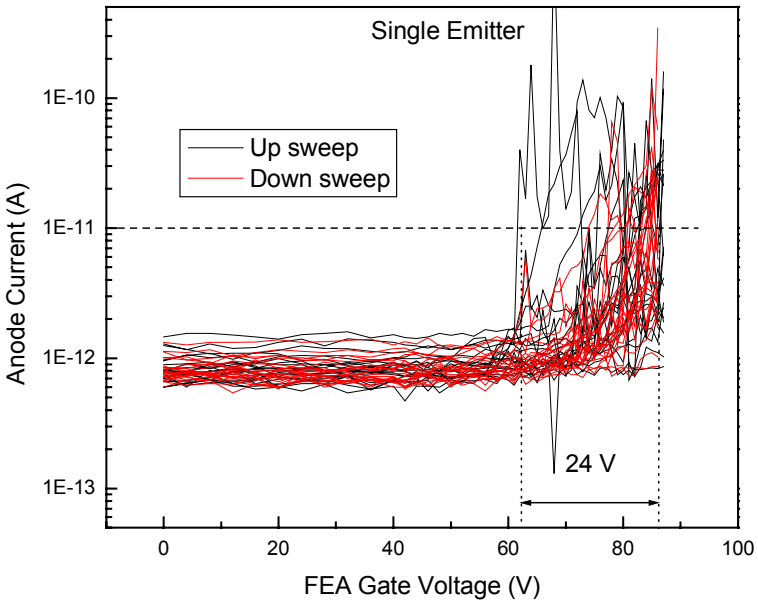


Figure 5-18. (a) Voltage spread of a single emitter at anode current of 0.01 nA.

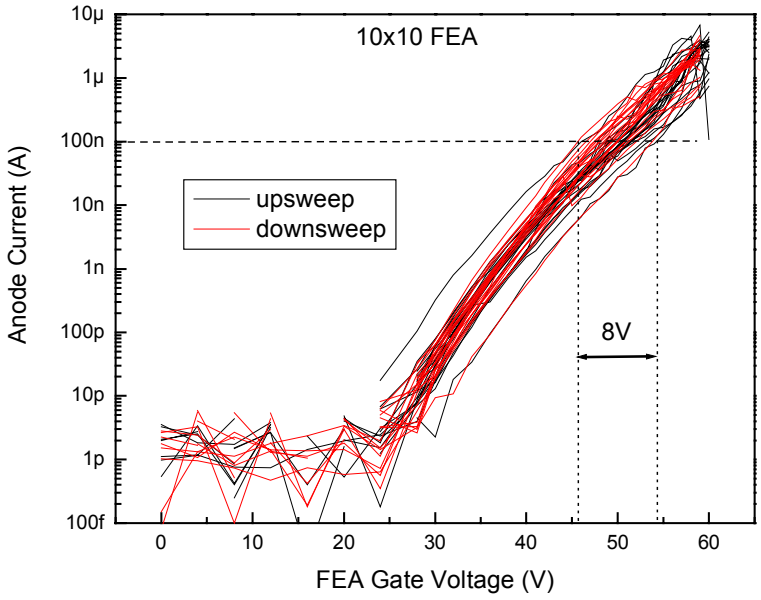


Figure 5-18. (b) Voltage spread of a 10x10 FEA at anode current of 100 nA.

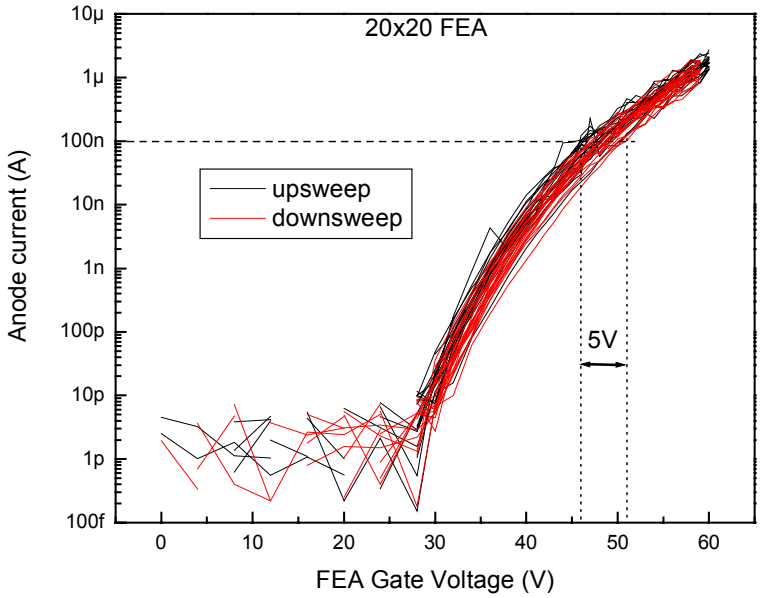


Figure 5-18. (c) Voltage spread of a 20x20 FEA at anode current of 100 nA.

Figure 5-19 compares the emission current of three different array sizes. The IV sweeps of different array sizes are from the 11th peak of Figure 5-16 (a)-(c). The single emitter is quite blunt compared with the emitters in 10x10 array and 20x20 array. More experimental data sets are shown in Appendix G.

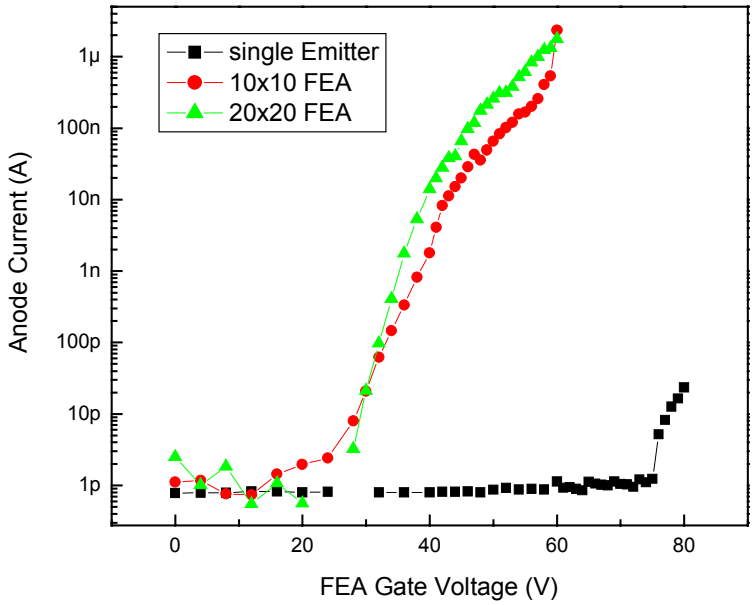


Figure 5-19. Spatial emission current non-uniformity in the FEA devices with different sizes. The IV sweeps of different array sizes are from the 11th peak of Figure 5-16 (a)-(c).

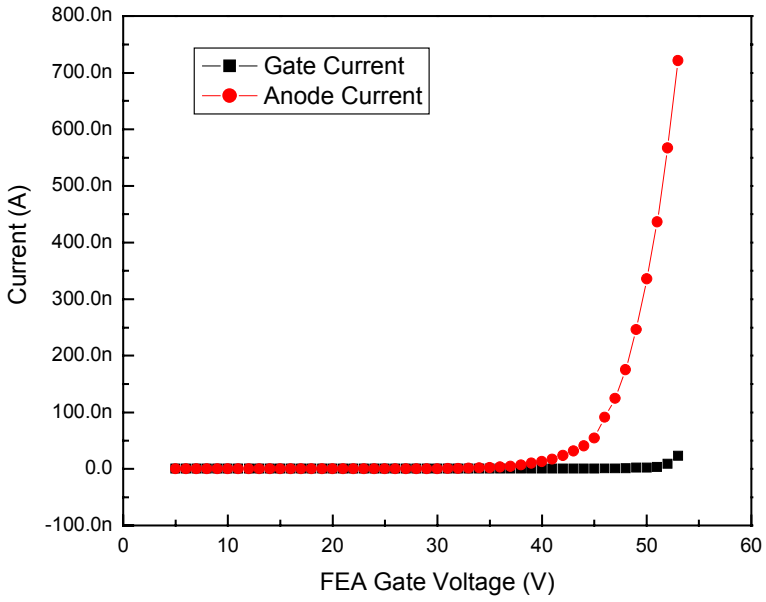
Gate Leakage

The emission current of FEA devices is generally lower than expected. The possible reasons are stated as follows: First, not all of the tips are emitting and only the sharp tips dominate the emission as stated in the previous section. Therefore, the total emission current would be far less than expected. Second, the gate leakage is larger than we expected. The leakage path is possibly through the oxide surface. According to Itoh's work [5.13], a thin nitride layer could be deposited between polysilicon gate and oxide insulator to increase the length of the surface leakage path between the gate and the substrate instead of only the thickness of oxide insulator. Third, if the tip's apexes were below the gate, in other words, the tip of the emitter is not at the same level with the extraction gate, the emission current would be extracted to the gate instead of anode. It depends sensitively on the CMP process used to open the gate aperture. CMP not only

defines the aperture size, the lateral distance between the tip and gate, but also the vertical distance between the tip and the gate.

Low gate leakage current is an important merit of figure to reflect the efficiency of the device and is very important for enhancing the lifetime of the field emitter arrays. Figures 5-20 (a) and (b) show the gate current and anode current in a field emission array. The gate current/anode current ratio is about 2% at higher FEA gate voltage (larger than 50 V). Figure 5-20 (b) shows that the gate leakage gradually increases with gate voltage. The gate current might come from the gate leakage through the oxide insulator, gate leakage along the oxide surface, or the emission current collected by the gate. The detail study of the source of the gate current will be discussed in the following chapter utilizing the integrated MOSFET/FEA device. In some of the devices, the gate leakage is over half of the anode current. We usually considered these devices bad devices and did not characterize them.

(a)



(b)

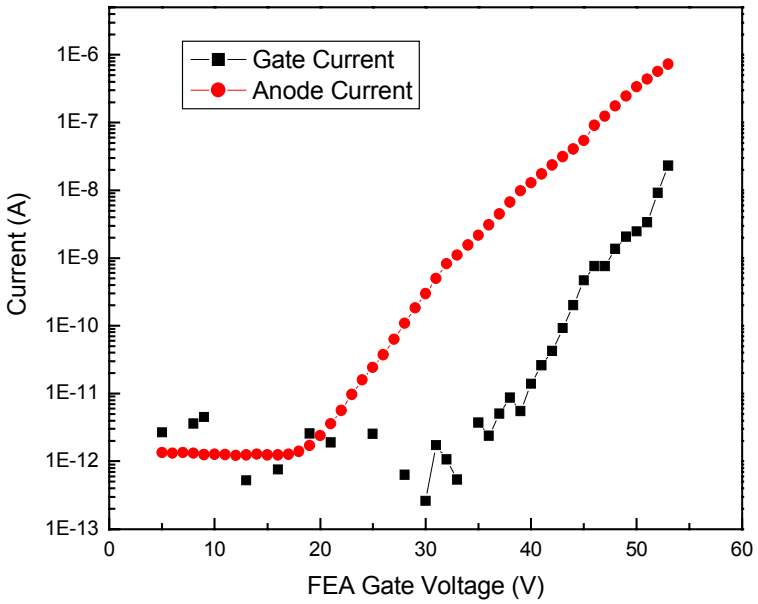


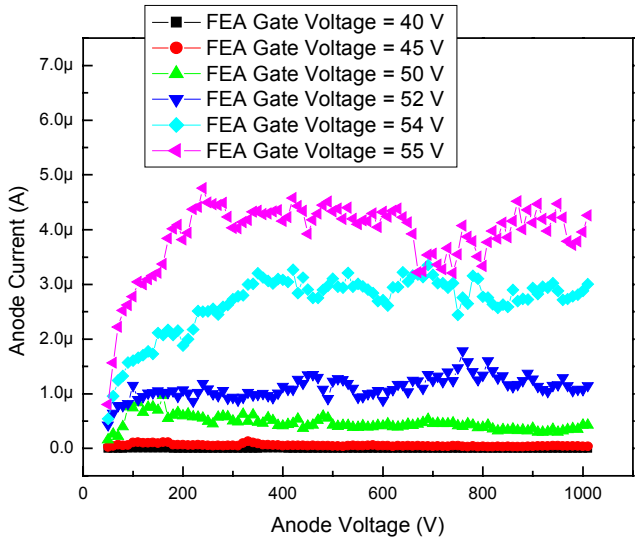
Figure 5-20. Gate leakage current and anode current in a field emission array, (a) linear plot and (b) semi-log plot.

The Effect of Anode Voltage

We also studied how the anode voltage affects the current collection by the anode. The anode and gate currents were monitored while the anode voltage was varied from 0 V to 1000 V and the FEA gate voltage was kept constant. The measurement was repeated at different FEA gate voltages. Figure 5-21 (a) shows that the anode current increases as the anode voltage increases at lower anode voltage. The current saturates after the anode voltage reached 200 V. The anode current fluctuation in the saturation region is due to the inherent current fluctuation of the field emission device. At the lower anode voltages as shown in Figure 5-21 (b), the anode collects electrons only if the anode voltage is larger than 6 V. Theoretically, this value should be the work function of the anode material, which is 5.15 V in nickel [5.14]. The slight deviation may be due to the contact

resistance or slightly oxidized surface of the nickel anode, which has larger work function.

(a)



(b)

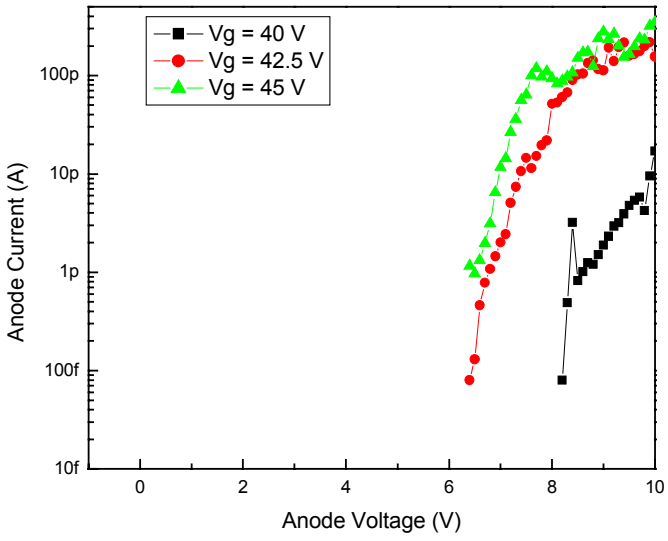


Figure 5-21. (a) Anode current was monitored as the anode voltage was varied from 0 V to 1000 V and the FEA gate voltage was kept constant. (b) Anode current at the lower voltage end. The size of the array is 10x10.

Figures 5-22 (a)-(d) show the energy band diagrams of the field emitter and the anode electrode when the FEA extraction gate and anode are biased at different voltage conditions. In our case, the work function of the anode, nickel, is larger than the work function of the emitter, silicon. Figure 5-22 (a) shows the energy diagram when there is no voltage applied to both the anode and the extraction gate. Since the work functions of the emitter and anode materials are different, the vacuum level is sloped when the Fermi-levels lineup. When the applied FEA extraction gate voltage is high enough, the electrons can tunnel out the bent barrier as shown in Figure 5-22 (b). However, the anode will not collect any electrons emitted if the applied anode voltage is smaller than the work function of the anode. The emitted electrons see an energy barrier in front of the anode, and most of the electrons are collected by the FEA extraction gate. When the applied anode voltage is higher than the work function of the anode material, the energy barrier disappears and the electrons emitted can reach the anode as shown in Figure 5-22 (c). In other words, this voltage is the theoretical initial voltage that anode can collect the emitted electrons. Figure 5-22 (d) shows the typical energy band diagram when operating the field emission device. High enough voltages are applied to both FEA extraction gate and anode so that the electrons can easily tunnel out of the emitter and be easily collected by the anode.

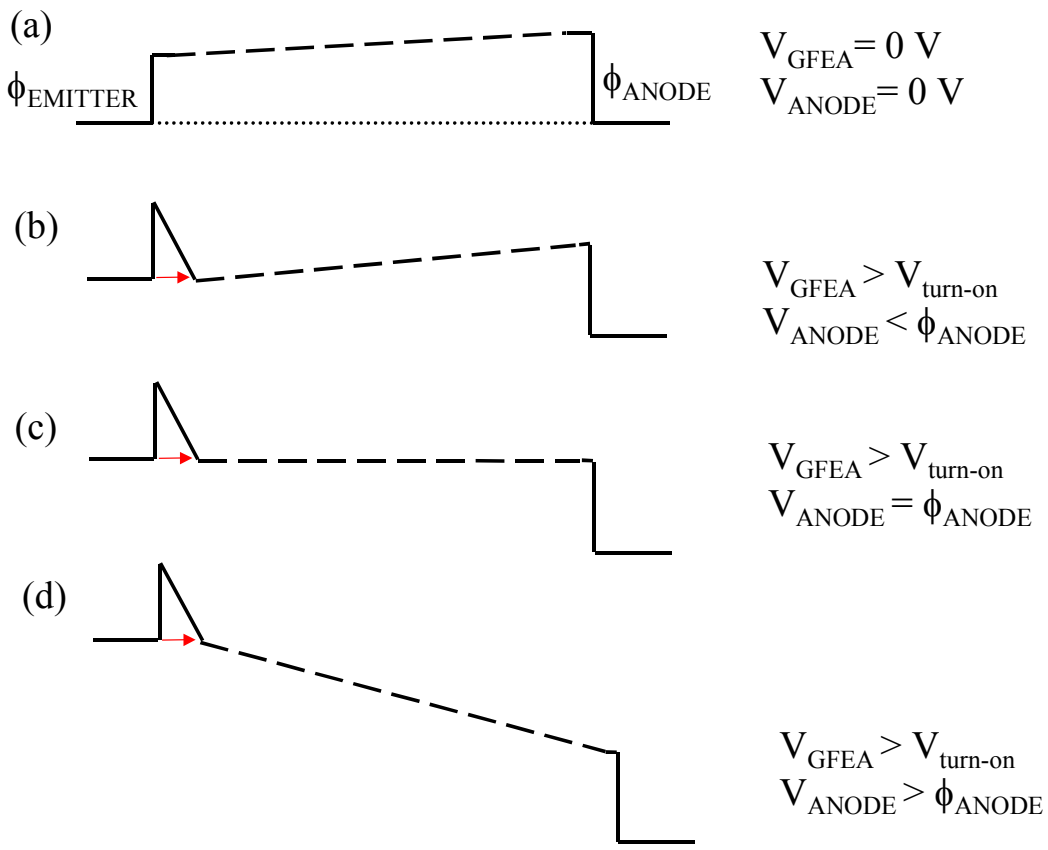
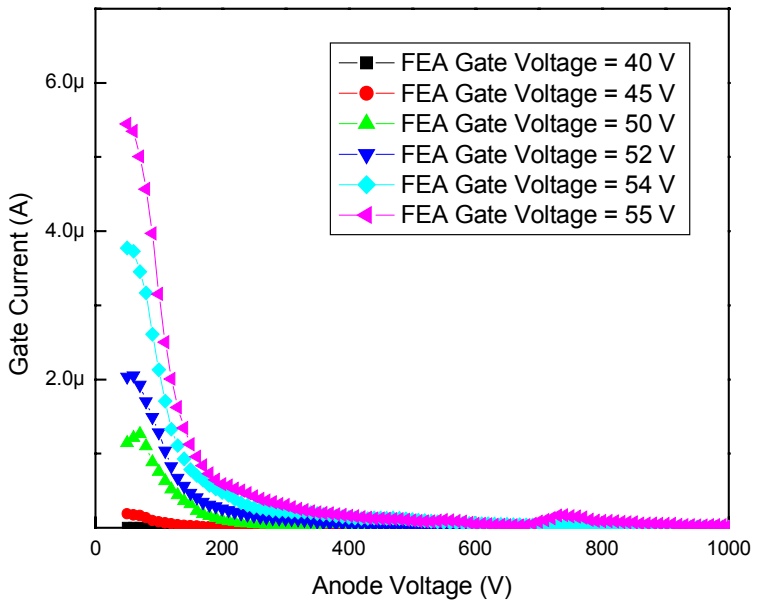


Figure 5-22. Energy band diagram of the field emitter and the anode electrode.

Figures 5-23 (a) and (b) show the gate current vs. anode voltage for this experiment. It clearly shows that when anode voltage is below 200 V, most of the emitted electrons go to the gate. The proportion of emitted electrons collected by the anode increases as the anode voltage increases. In other words, when anode voltage is larger than 200 V, it is large enough to collect all emitted electrons and the anode current is no longer a function of anode voltage [5.15]. In this thesis, the anode current was collected with the anode voltage kept at 1000 V if not specified.

(a)



(b)

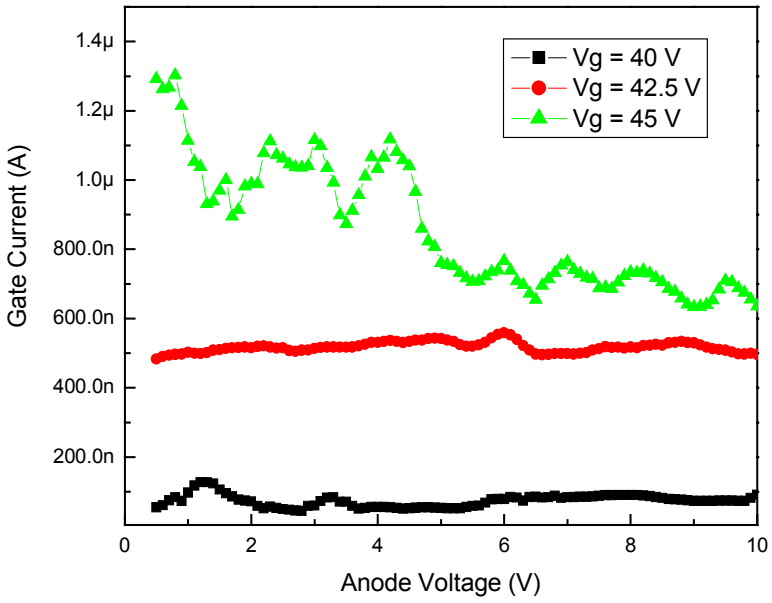


Figure 5-23. (a) Gate current was monitored as the anode voltage was varied from 0 V to 1000 V and the FEA gate voltage was kept constant. (b) Gate current at lower anode voltage end.

Discussion

Ding *et al.* compared the emission characteristics of the silicon field emitters fabricated in literatures [5.16]. Table 5-3 summarizes of the characteristic results including our FEA device. Ding concluded that the turn-on voltage (V_{ON}) could be correlated with b_{FN} in the following equation

$$V_{ON} \approx \frac{b_{FN}}{\ln\left[\frac{k_{FN}}{I_{ON}}\right]} \approx 0.0358\ b_{FN} + 4.6948 \tag{5.15}$$

where I_{ON} is the turn-on current [5.16]. Our data is consistent with Ding's experimental work.

Table 5-3. Literature reports of silicon field emitters [5.16].

Group	Gate aperture	Tip radius of curvature (observed)	Turn-on voltage	b_{FN}	β (cm^{-1})	Radius of curvature ("ball in sphere" model)
Hong	1.3 μm	6.2 nm	24 V	370	$1.45x10^6$	6.9 nm
Ding [5.2]	1 μm	9.2 nm	30 V	830	$6.4x10^5$	15.6 nm
Ding [5.16]	1 μm	1.75 nm	16 V	243	$2.2x10^6$	4.56 nm
Pflug [5.3]	70 nm	4.5 nm	8.5 V	203	$2.6x10^6$	3.85 nm
Uh [5.15]	1.6 μm		38 V	791	$6.68x10^5$	14.8 nm
Trujillo [5.17]	400-500 nm		12 V	131	$4.03x10^6$	2.48 nm
Koga [5.18]	1 μm		8 V	96.1	$5.49x10^6$	1.82 nm
Hisashi [5.19]	90 nm		17 V	270	$1.95x10^6$	5.13 nm

There are several reports on the responses of the emission current to different gas molecules. Temple *et al.* reported the effect of exposure to O_2 and N_2 on silicon field

emitter [5.12]. The gas was admitted into the test chamber through a leak valve until the desired pressure (ex. 10^{-6} Torr) was achieved. The leak valve was then closed. The emission current decreases with time and approaches a plateau value depends on the initial current and total pressure. The current reaches a plateau because the density of adsorbed molecules reaches equilibrium as time increases. In our experiment, the gas molecules were fed through the leak valve continuously and pump out to sustain a constant pressure. The emission current drop with the input of the gas was also observed in our experiment. The emission current is lower when the input gas pressure is higher, which is the same conclusion in both Temple's and our case. However, they found that the emission current would recover when the pressure is pumped down to high vacuum during the operating of the FEA device. This is different from what we observed. We found that the emission current level would only be restored after removing electrostatic bias and restarting in the high vacuum.

Other than Temple *et al.*, Kanemaru *et al.* reported that the emission current from silicon field emitters decreases when the emitters were operating in H_2 and N_2. The current fluctuation increases in both cases [5.20]. Gotoh *et al.* reported the emission characteristics of Spindt-type field emitter arrays (Au, Pt, and Mo emitters) in oxygen ambient [5.11]. The emission current decreases and the noise power increases with an increase in oxygen pressure. Oxygen molecules adsorb at the emitter surface to increase the work function hence decrease the emission current. The current fluctuation is explained by adsorption and desorption of the oxygen molecules on the emitter surface. Chalamala *et al.* reported that hydrogen gas undergoes dissociation and ionization near the emitters. The emitter surface is conditioned through the interaction of the hydrogen atoms and ions with molybdenum emitter, resulting in the formation of volatile molybdenum hydrides. The volatile species are removed by the vacuum system and result in reduced work function and increased electron emission [5.6].

Gilkes *et al.* reported that the emission current from silicon field emitters degrades very fast in CO_2, slower in CH_4, and very slow in ultra high vacuum (UHV) when the emission current was monitored longer than 20 hours [5.7]. In UHV, the degradation was

due to an increase in work function with time. For CO_2 and CH_4, the degradation was primarily due to a blunting of the tips as emission progresses. Matsukawa *et al.* reported the emission current increase when the silicon emitter tips were operating in the C_2H_2 ambient due to work function reduction [5.21]. The C_2H_2 ambient also improves the emission uniformity because the amount of working tips increases in the C_2H_2 ambient.

The summary of our experimental work is that work function changes resulting from exposure to gas molecules dominate the changes in emission current if no chemical reaction occurs on the emitter surface. The work function changes are due to the adsorption and desorption of the gas molecules to the emitter surface. Our findings are consistent with the literature.

5.3 Chapter Summary

In this chapter, we presented the electrical characteristics of the silicon field emission arrays. The emission current fits Fowler-Nordheim equation very well with the following FN parameters: $a_{FN} = (3.14\pm0.3) \times 10^{-7}$ and $b_{FN} = 369\pm4$. We obtained the tip radius of 1.8 nm by fitting the emission current using numerical simulation. It is suggested that the sharp emitters in the field emission devices would dominate the emission current. We also presented the temporal emission fluctuation and calculated the work function distribution that leads to the current fluctuation. The emission behavior depends on the gas atmosphere in the operation system. The emission current decreases and the current fluctuation increases with the existence of the gas molecules. The emission currents from different array locations and array sizes were compared to show the spatial non-uniformity of the field emission. Extraction gate leakage in the field emission device is low compared with the emission current. The gate current might emanate from the leakage though the oxide insulator, the leakage along the oxide surface, or the emission current collected by the gate. The anode current increases with the applied anode voltage at lower anode voltages. The anode current saturates when the anode voltage is greater than 200 V. When anode voltage is larger than 200 V, it collects all the electrons that are

emitted. Finally, the literature reports of the FEA device performance and emission current response to gas molecules are consistent with our device performance.

6. Active Field Emission Device Characterization and Analysis

In previous chapters, a device structure for enhancing the performance of field emission devices was presented. The device structure consists of a voltage controlled current source in series with a field emission device. The current source controls the electron supply to the field emission surface. In this thesis, we chose MOSFET as the voltage controlled current source. In this chapter, we describe and analyze the electrical characteristics of the LD-MOSFET and the electrical characteristics of the integrated LD-MOSFET/FEA device.

6.1 MOSFET Characterization

6.1.1 Measurement Setup

Electrical characterization of MOSFET devices was conducted on a test station equipped with a microscope. Source Measure Units (HP 4145B) were used to simultaneously source the voltage and measure the current. This setup is shown in Figure 6-1. The devices were probed on-wafer and the I-V characteristics of the MOSFET were monitored. The test station was placed in a black box to allow device operation in the dark avoiding any photo-response.

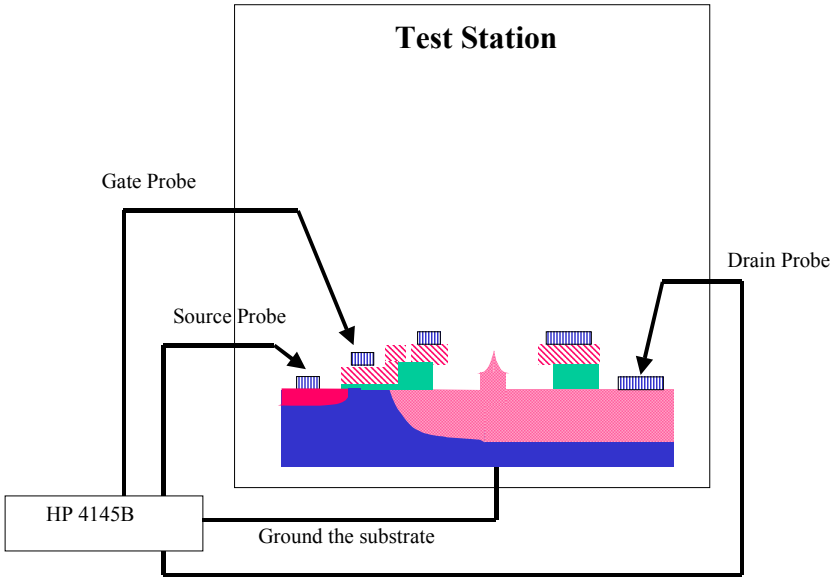


Figure 6-1. The schematic of the test station and the electronics setup.

6.1.2 Device Characterization

In the preliminary experiments shown in Figure 6-2, the measured breakdown voltage of the MOSFET device is much lower than the values obtained from device simulation [6.1]. The measured breakdown voltages of the MOSFET devices and the lightly doped-MOSFET (LD-MOSFET) devices were similar indicating that the lightly doped drain did not work as expected. A measurement of the p-n junction breakdown shown in Figure 6-3, however, confirmed that the breakdown of the MOSFET devices did not occur in the drain region. Instead, the devices broke down at the source/drain leads that connect the source/drain and the metal pads. The leads were heavily doped with phosphorous to reduce their resistance and were surrounded by high concentration boron dopants, which were intended for isolation and reduction of leakage current between devices. Simulation confirmed a breakdown voltage of 8.5 V as shown in Figure 6-4 for heavily doped boron (p+) region and heavily doped phosphorous (n+) region placed adjacent to each other. The breakdown problem could be solved by increasing the separation of the p^+ and n^+

regions. The results of the device simulation shown in Figures 6-5 (a) and (b), suggest that the breakdown voltage of the pn junction between the MOSFET device and the isolation region could be enhanced to about 100 V provided there is a 10 μm separation between the heavily doped phosphorous and boron regions. The leads that connect the MOSFET sources and metal pads are in direct contact with the p- substrate. Therefore, the current voltage characteristics for the p+/p/n+ structure shown in Figure 6-5 (a) suggests a breakdown voltage of 98 V. On the other hands, the leads that connect the MOSFET drains and metal pads are embedded in the n- well on the p substrate. The junction I-V simulation for the p+/n-/n+ structure shown in Figure 6-5 (b) suggests a breakdown voltage of 113 V.

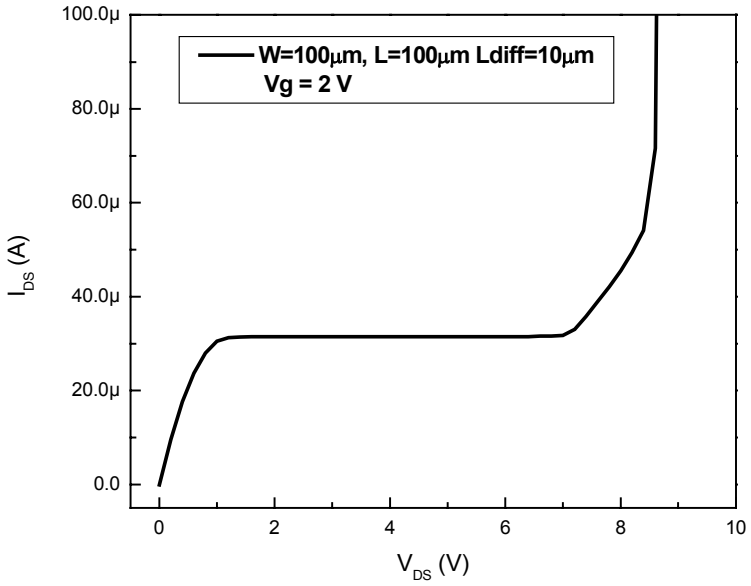


Figure 6-2. Output characteristics of the LD-MOSFET in the preliminary experiments. The MOSFET has the breakdown voltage of 8 V.

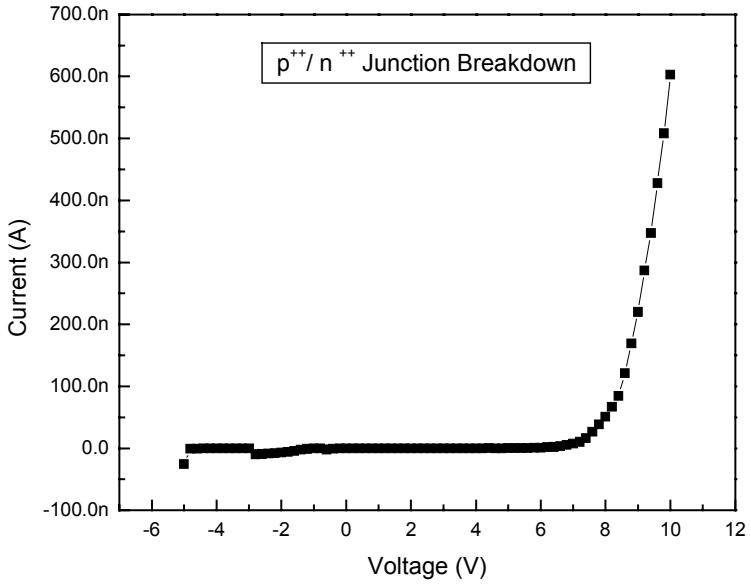


Figure 6-3. Breakdown at the source/drain leads that connect the source/drain and the pads.

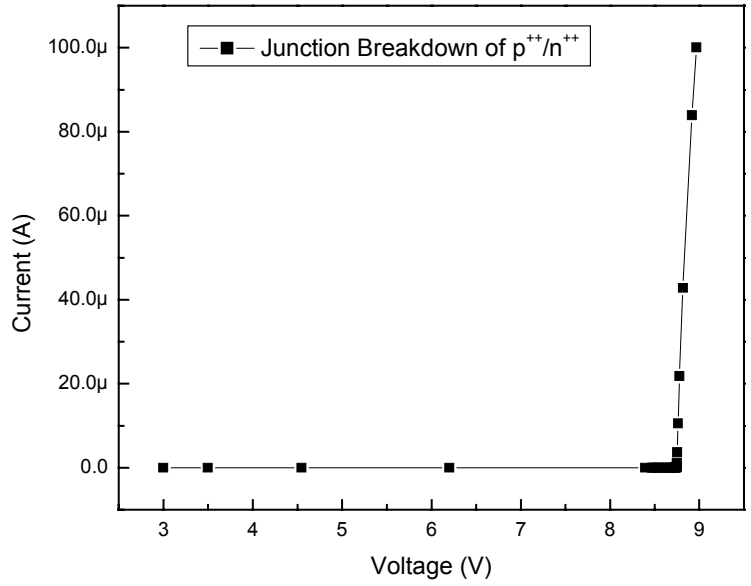
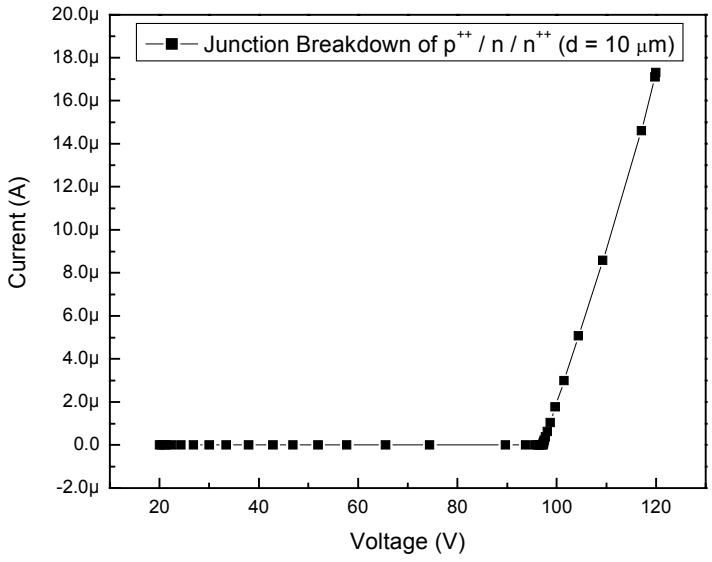


Figure 6-4. Simulation of breakdown voltage at which heavily doped boron region and heavily doped phosphorous region are placed adjacent to each other.

(a)



(b)

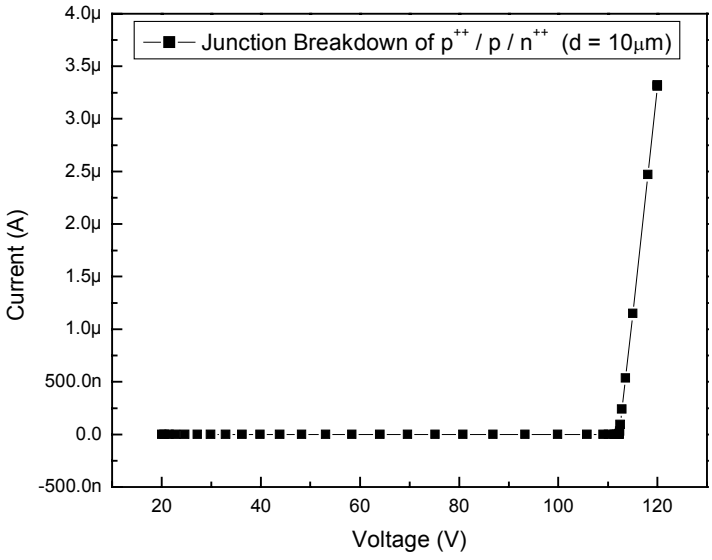


Figure 6-5. Simulation of breakdown voltage at which heavily doped boron region and heavily doped phosphorous region are placed with a 10 μm separation when (a) n- post doping is in between and (b) p substrate is in between.

Figure 6-6 shows the output characteristics of the LD-MOSFET after we revised the mask and a 10 μm separation was placed between the heavily doped phosphorous and boron regions. The device shows the breakdown voltage of ~ 36 V. This 10 μm separation solved the breakdown that occurs at the pn junction between the device area and the isolation implantation. The MOSFET breakdown voltage does not depend on the pn junction between the heavily doped leads and the isolation implantation anymore but on the pn junction between the MOSFET channel and the drain region. In this MOSFET device, the n well implantation dose is $5x10^{12}$ cm^{-2}, which results in $1.5x10^{16}$ cm^{-2} at the drain region after emitter tip formation. The theoretical breakdown voltage is ~ 40 V, which is very close to the actual measured breakdown voltage. Even though the measured breakdown voltage is lower than the design breakdown voltage, 60 V, because the doping concentration is a little higher than expected at the n-well, this breakdown voltage of 36 V is beyond what is required for the integrated LD-MOSFET/FEA devices. As indicated in Chapter 2, in order to accommodate current variation of the field emission device, the current source saturation voltage range has to be larger than the voltage spread of the field emission device at a certain current level. As we also presented in Chapter 5, the voltage spread at a reasonable current level of a 10x10 FEA is smaller than 36 V. From Figure 6-6 we observed that the output resistance of the transistor in the saturation regime is ~ $5x10^{7}$ Ω. Figure 6-7 shows the transfer characteristics of the LD-MOSFET. The threshold voltages of LD-MOSFETs range from 0.4 to 0.6 V, with an average value of 0.5 V. The gate oxide thickness is 45 nm and the electron mobility in the transistor is calculated to be 430 cm^2/V-sec. The subthreshold slope, as shown in Figure 6-8, is 100 mV/decade. Our LD-MOSFET device is a well-behaved MOSFET device.

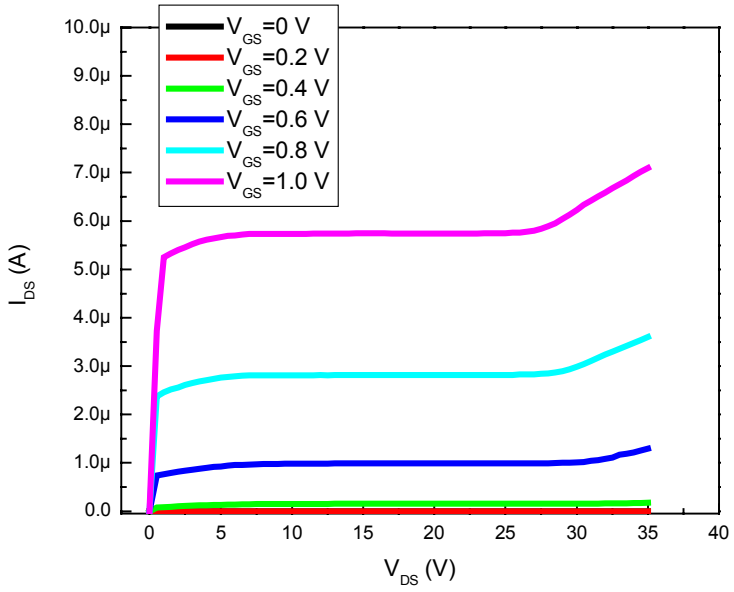


Figure 6-6. Output characteristics of a LD-MOSFET.

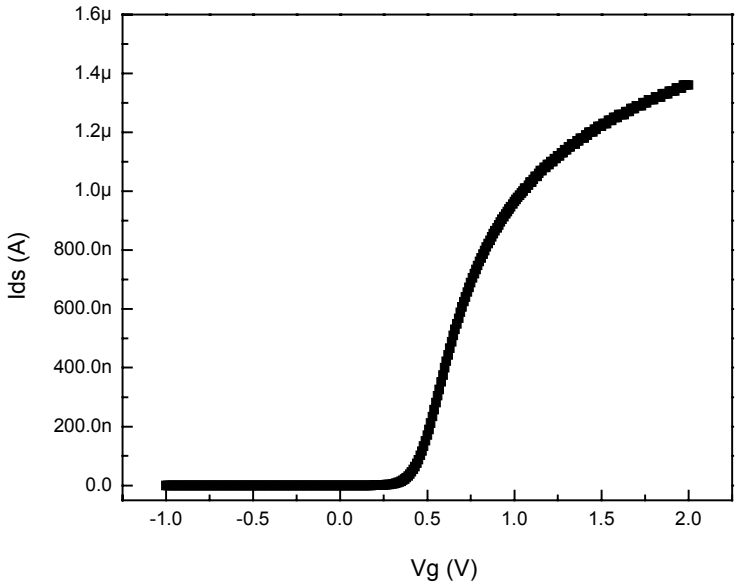


Figure 6-7. Transfer characteristics of a LD-MOSFET.

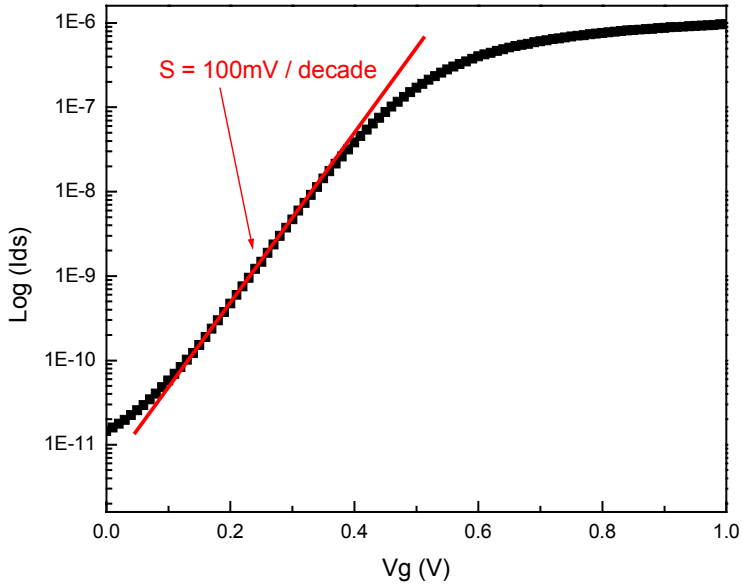
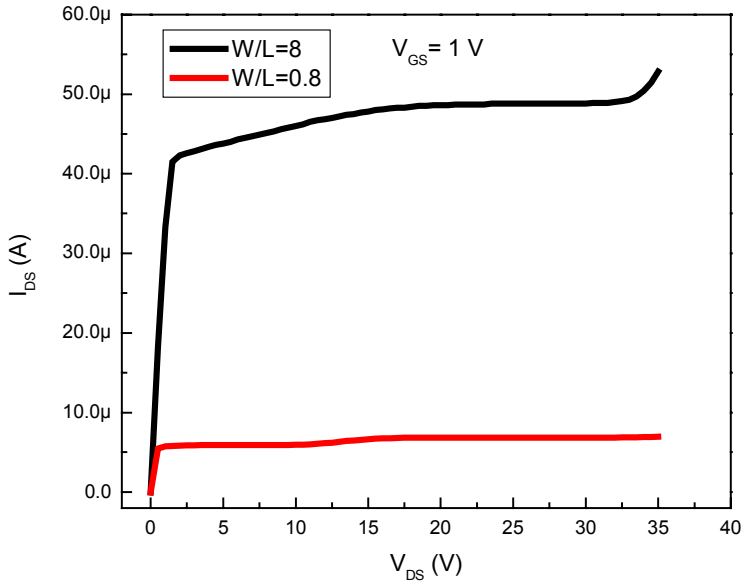


Figure 6-8. Subthreshold slope of a LD-MOSFET.

MOSFETs with different width/length (W/L) ratios were fabricated. The original W/L ratios in our layout were 10 (100 μm/10 μm), 1(100 μm/100 μm), and 0.1(10 μm/100 μm). After the layout revision due to breakdown enhancement, the W/L ratios were 8 (80 μm/10 μm), 0.8 (80 μm/100 μm), and 0.04 (4 μm/100 μm) because only the width of the MOSFET was modified but not the length. The drain currents are approximately proportional to the W/L ratios in the MOSFET devices as shown in Figures 6-9 (a) and (b). We observed some deviation in the drain current due to the drain resistance of the lightly doped drain in the LD-MOSFET devices as shown in Figure 6-10. Resistance is proportional to the length of the resistor. The longer the drift length, the larger the resistance in the lightly doped drain is.

(a)



(b)

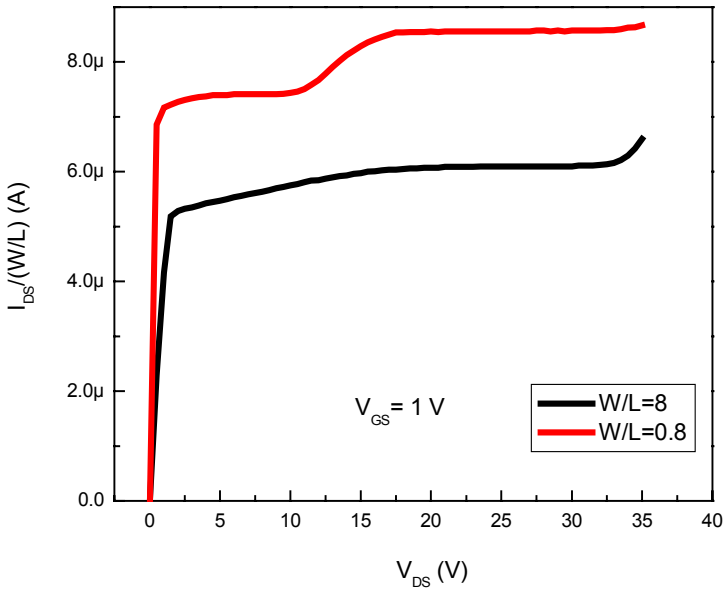


Figure 6-9. (a) Output characteristics of two LD-MOSFET devices. The drift lengths are both 100 µm and the gate voltage is 1 V. (b) Normalized I_{DS} with W/L.

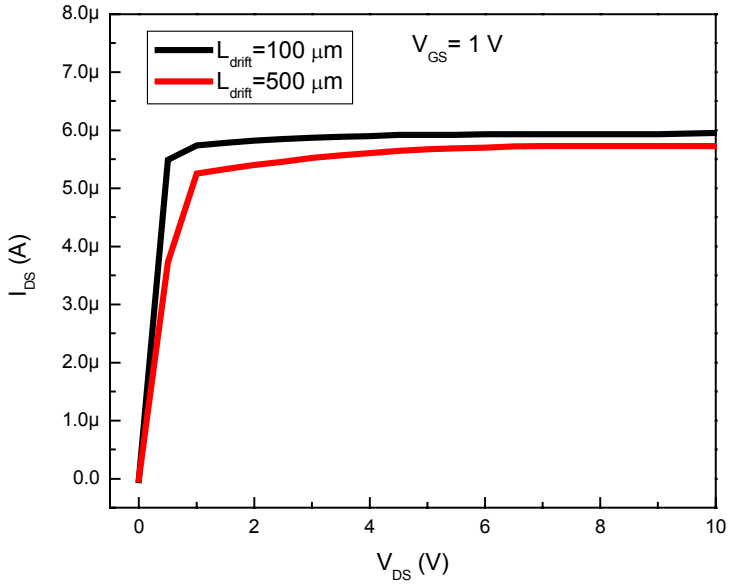


Figure 6-10. Output characteristics of two LD-MOSFET devices. The drift lengths are 100 and 500 μm, respectively, the W/L is 0.8, and the gate voltage is 1 V.

6.2 LD-MOSFET/FEA Characterization

6.2.1 Measurement Setup

The characterization configuration for the integrated LD-MOSFET/FEA device is similar to that for the FEA device: both of the characterizations were conducted in the UHV chamber. The configuration is shown in Figure 6-11. Here, the devices were probed on-wafer and the emitter current, anode current, both FEA and FET gate currents were monitored.

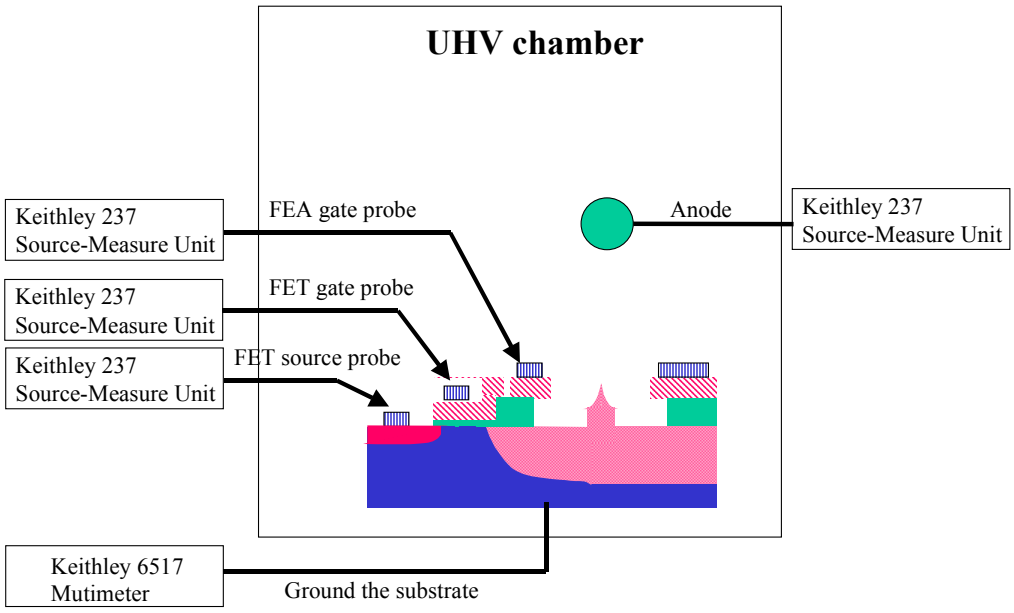


Figure 6-11. The schematic of the UHV testing chamber and the electronics setup.

6.2.2 Device Characterization

Two types of transfer characteristics were taken on the integrated LD-MOSFET/FEA devices. The first transfer characteristic biases the MOSFET gate voltage at a constant voltage higher than the MOSFET threshold voltage while the emission current is varied by changing the FEA extraction gate voltage. The second transfer characteristic biases the FEA extraction gate voltage high enough to obtain electron emission from the FEA while the MOSFET gate voltage is varied to control the emission current.

Transfer Characteristics with MOSFET Gate Voltage Constant:

Figure 6-12 shows the semi-log plot of the anode current as a function of FEA extraction gate voltage in a LD-MOSFET/FEA device. The device has a 20x20 array of emitters

and a MOSFET with channel width of 100 μm, channel length of 10 μm, and drift length of 500 μm. The FEA gate voltage was swept from 0 to 60 V at fixed MOSFET gate voltages above the MOSFET threshold voltage. In this particular integrated LD-MOSFET/FEA device, the threshold voltage of the LD-MOSFET is -0.2 V and the breakdown voltage of the LD-MOSFET is 8 V. When the MOSFET gate is biased below the threshold voltage, the device is always off irrespective of the FEA extraction gate voltage. There are four distinct regimes of operation in Figure 6-12. In the first regime, the device is in the off state at FEA extraction gate voltages below 25 V, which is the turn-on voltage of this FEA device. In the second regime, the device turns on and the anode current increases exponentially as the FEA extraction gate voltage increases. In this regime, the electron transmission is low and the emission current is determined by the transmission probability. The electron transmission increases as the FEA extraction gate voltage is increased. This is the transmission (FEA) controlled regime. In the third regime, the anode current saturates even though the FEA extraction gate voltage is increasing. The transition voltage between the FEA controlled regime and the saturation region is dependent on the relative sizes of the FEA and the MOSFET. The saturation voltage can be predicted numerically. In this particular device,

$a_{FN} = 2.18 \times 10^{-4}$,

$b_{FN} = 725.8$ (from the FN plot of the FEA in this particular device),

$$I_A = 2.18 \times 10^{-4} \times (V_{GE})^2 \exp\left[\frac{-725.8}{(V_{GE})}\right], \tag{6.1}$$

$$I_{D\_sat} = 1 \times 10^{-6} \text{ A}$$

when the LD-MOSFET gate is biased at 0.45 V,

$V_{GE} = 54.5$ V.

$V_{transition} = V_{GFEA} = V_{GE} + V_{DS\_sat} \sim 55.5$ V

because the onset of the MOSFET saturation $V_{DS\_sat} \sim 1$ V as shown in Figure 6-2. This predicted saturation voltage is very close to the actual voltage, 54 V. The small deviation comes from the variation of the anode current in the FEA control regime. The saturation anode current increases as the MOSFET gate voltage increases because higher MOSFET gate voltage results in higher electron density in the inversion layer. This regime is the electron supply (MOSFET) controlled regime. In this regime the electron transmission of

the FEA surface is relatively high compared to the electron supply. It is noted that there is no saturation when the MOSFET gate voltage is biased at 1 V or above. At these MOSFET gate voltages, the electron supply to the emission surface is very high and the anode current is only determined by the electron transmission. Further increase in the FEA gate voltage would result in the saturation of anode current at these MOSFET gate voltages. In the fourth regime, the anode current increases again with the FEA extraction gate voltage. The MOSFET breaks down when the FEA extraction gate voltage is 7 V above the saturation voltages. For example, when the MOSFET gate is biased at 0.45 V, $V_{breakdown} = V_{GFEA\_sat} + 7 \sim 62.5$ V. The device breakdown occurs at lower FEA extraction gate voltages when the MOSFET gate voltages are smaller. The 7 V observed in this figure is consistent with the voltage difference between the MOSFET saturation and breakdown voltages observed during MOSFET characterization shown in Figure 6-2. This breakdown is reversible and it is due to the MOSFET breakdown at the source/drain leads to the metal pads as presented in Section 6.1. If the MOSFET breakdown voltage could be increased to about 10 V, it would provide sufficient margin for the integrated device to operate below the breakdown voltage. This voltage accommodates the voltage spread of the field emission device at reasonable operating FEA extraction gate voltages.

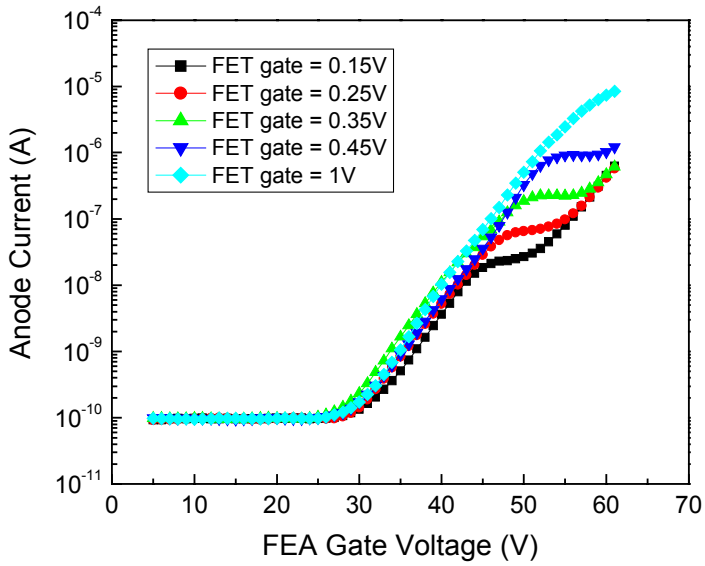


Figure 6-12. Semi-log plot of emission current as a function of FEA extraction gate voltage of an integrated LD-MOSFET/FEA device. The integrated device has a FEA with 20x20 emitters and a MOSFET with channel width of 100 μm, channel length of 10 μm, and drift length of 500 μm.

The data in Figure 6-12 is presented in a FN plot shown in Figure 6-13. The plot confirms that the device is in the transmission control mode in the device breakdown regime. At very low FEA extraction gate voltages, the FN plot is linear with a negative slope indicating that the emission current follows the Fowler-Nordheim characteristics and is controlled by the transmission of electrons through the surface barrier. At intermediate FEA extraction gate voltages, the FN plot becomes non-linear indicating that the emission current is electron supply limited. At very high FEA extraction gate voltages, the MOSFET device is operating in the breakdown regime. In this regime, the FN plot is linear with a negative slope indicating that the emission current is again controlled by the transmission. It should be noted that the slope of the FN plot in the first regime (MOSFET linear region) and the third regime (MOSFET breakdown) are similar. The slight curvature of the plot is due to the varying voltage drop across the MOSFET, V_{DS}.

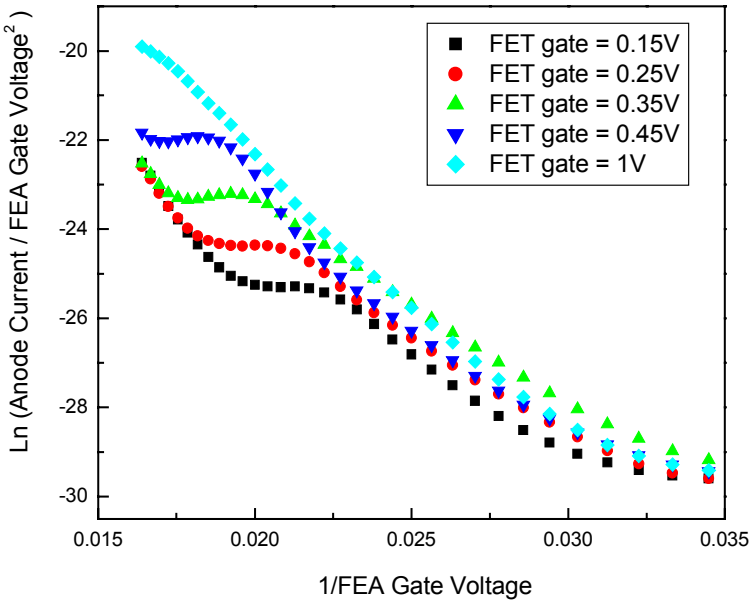


Figure 6-13. FN plot of Figure 6-12.

The LD-MOSFET breakdown voltage was increased by modifying the placement of the heavily boron doped isolation region relative to the heavily arsenic doped source/drain leads to the metal pads as discussed in the previous section. The I-V characterization was repeated on a new integrated LD-MOSFET/FEA device with a higher breakdown voltage as shown in Figure 6-14. The data shown in Figure 6-14 does not have a breakdown region at high extraction gate voltages. The figure shows clearly two distinct regimes: FEA control regime at lower extraction gate voltage and MOSFET control regime at higher extraction gate voltage as indicated in the figure. The threshold voltage of this particular LD-MOSFET device is about 0.05 V. Similarly, the saturation voltage can be predicted numerically. In this particular device, take $V_{GFET} = 0.5$ V for example,

$a_{FN} = 7.05 \times 10^{-7}$,

$b_{FN} = 569$,

$$I_A = 7.05 \times 10^{-7} \times (V_{GE})^2 \exp\left[\frac{-569}{(V_{GE})}\right], \tag{6.2}$$

$$I_{D\_sat} = 0.17 \times 10^{-6} \text{ A}$$

for this particular LD-MOSFET when the MOSFET gate is biased at 0.5 V,

V_{GE} = 59.5 V.

$V_{transition} = V_{GFEA} = V_{GE} + V_{DS\_sat} \sim 60.5V$

because the onset of the MOSFET saturation $V_{DS\_sat} \sim 1$ V as shown in Figure 6-2. This predicted saturation voltage is reasonably close to the actual voltage, 58 V.

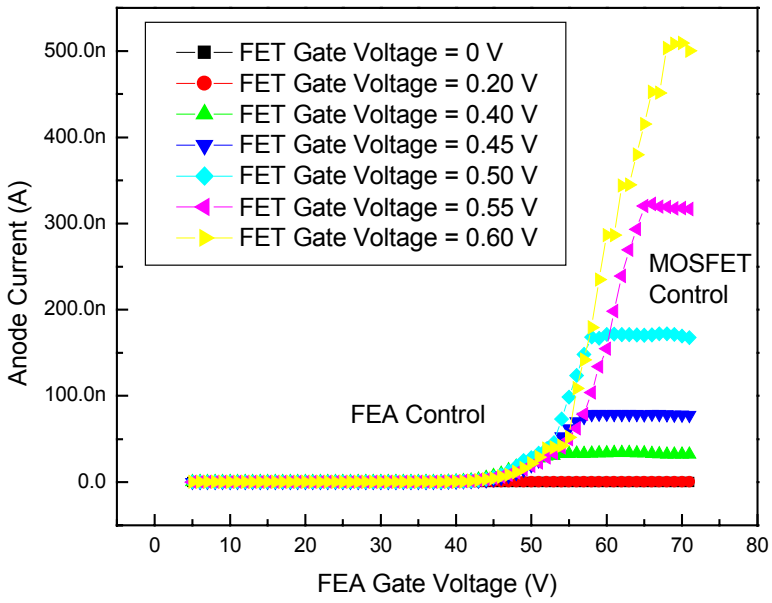


Figure 6-14. Emission current as a function of FEA gate voltage of an integrated LD-MOSFET/FEA device. The integrated device has a FEA with 10x10 emitters and a MOSFET with channel width of 80 μm, channel length of 100 μm, and drift length of 100 μm.

The data in Figure 6-14 is re-presented as a FN plot as shown in Figure 6-15. There are two distinct regimes of the FN plot: the negative slope region is the transmission control regime and the slightly positive region is the electron supply control regime. The FN plot of the integrated device indicates that the slope b_{FN} is ~ 569 in the transmission control regime. Simulation using *Matlab*, which was presented in Section 2.2, also shows a similar trend comparable to the experimental results. It is observed that the device is not fully turned off in the subthreshold regime of the MOSFET ($V_{GFET}<V_T$) due to the high

subthreshold slope in the MOSFET device. More experimental data sets are shown in Appendix G.

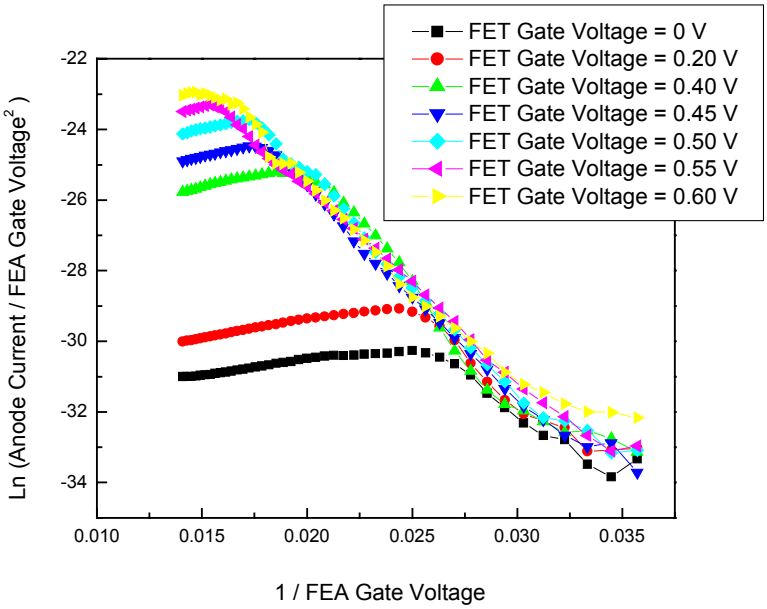


Figure 6-15. FN plot of Figure 6-14.

Transfer Characteristics with FEA Extraction Gate Voltage Constant:

Figure 6-16 shows the anode current as a function of MOSFET gate voltage in an integrated LD-MOSFET/FEA device. The MOSFET gate voltage was swept from -0.4 to 1.3 V at fixed FEA gate voltages above 40 V. Note that this particular FEA device has turn-on voltage of ~ 30 V. The device turns on at the MOSFET threshold voltage of 0.4 V and the device behaves as a regular transistor at the low MOSFET gate voltages. This is the electron supply (MOSFET) controlled regime. The anode current is controlled by the electron supply from the inversion layer. At the high MOSFET gate voltages, the anode current saturates at a level that could be supported by the electron transmission. In this regime, the electron density in the MOSFET channel is high and the electron supply to the emission surface is also high. The saturation anode current is determined by

electron transmission and it increases as the FEA extraction gate voltage increases. This is the transmission (FEA) controlled regime.

The transition voltage from electron supply controlled regime to transmission controlled regime can be predicted numerically. In this particular device, take V_{GFEA} = 50 V for example,

$$I_A \sim 1.25\ \mu A$$

for this particular LD-MOSFET when the FEA extraction gate is biased at 50 V,

$$I_D = \frac{1}{2}\mu_n C_{OX}\frac{W}{L}\left[V_{GS} - V_T\right]^2 \text{ A} \tag{6.3}$$

where μ_n = 480 cm^2/V-sec,

$$C_{ox} = \frac{\varepsilon_{ox}\varepsilon_0}{x_0} = \frac{3.9\times 8.85\times 10^{-14}}{50\times 10^{-7}} = 6.9\times 10^{-8} \text{ farad,} \tag{6.4}$$

$V_T \sim 0.5$ V,

$$I_D = \frac{1}{2}\times 480\times 6.9\times 10^{-8}\times\frac{80}{100}\times\left[V_{GS} - 0.5\right]^2 \tag{6.5}$$

V_{GS} = 0.8 V.

$V_{transition} = V_{GS}$ = 0.8 V

This predicted transition voltage is reasonably close to the actual voltage, 0.65 V.

The I-V characteristics of the integrated LD-MOSFET/FEA device shown in Figure 6-16 indicate that the LD-MOSFET provides excellent control of emission current. The integrated device can be switched from an on-current of 1.15 μA to an off-current of 0.57 nA using a MOSFET gate voltage swing of 0.5 V while the FEA gate voltage is biased at 50 V. This results in an on/off current ratio of 2000:1, far beyond the requirement of most field emission applications. For the FEA device without MOSFET control, an on/off current ratio of 1000:1 requires an extraction voltage swing of ~ 47 V as shown in Figure 6-16. It should be noted that in the FEA control region, the anode current saturates with large current fluctuation. This is due to the temporal instability of the FEA device, which was discussed in previous chapters.

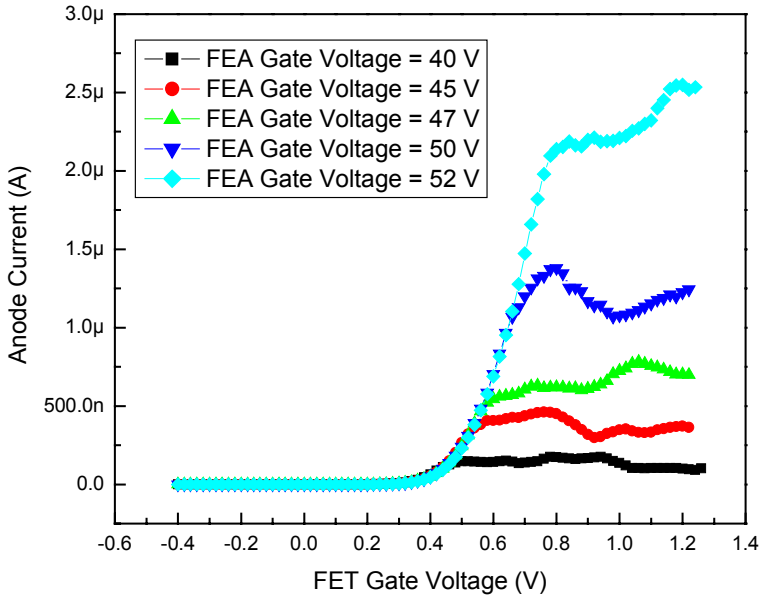


Figure 6-16. Transfer characteristics of an integrated LD-MOSFET/FEA device. The integrated device has a FEA with 10x10 emitters and a MOSFET with channel width of 80 µm, channel length of 100 µm, and drift length of 100 µm.

Gate Leakage

FEA extraction gate leakage was monitored during the field emission device operation. Figure 6-17 shows the comparison of the FEA extraction gate leakage current in the LD-MOSFET/FEA device with and without MOSFET operation. One set of measurements was conducted in the four terminals mode of operation and the other set of measurements was done only on the FEA part of the same integrated device. We denote the one with the MOSFET operation the integrated device and the one without the MOSFET operation the FEA device. The extraction gate current/anode current ratio is about 0.2% in the FEA device and about 1% in the integrated device at the same anode current level. Usually, higher extraction gate voltage would lead to higher extraction gate current. In order to obtain the same anode current level on both devices, the voltage across the emitters (V_{GE}) in both device operations has to be the same. V_{GE} in the FEA device is V_{GFEA}, the

voltage we applied on the extraction gate, while V_{GE} in the integrated device is V_{GFEA}-V_{DS}, where V_{DS} is the voltage across the MOSFET channel. Therefore, V_{GFEA} in the integrated device is higher than V_{GFEA} in the FEA device and it results in higher gate current in the integrated device. More experimental data sets are shown in Appendix G.

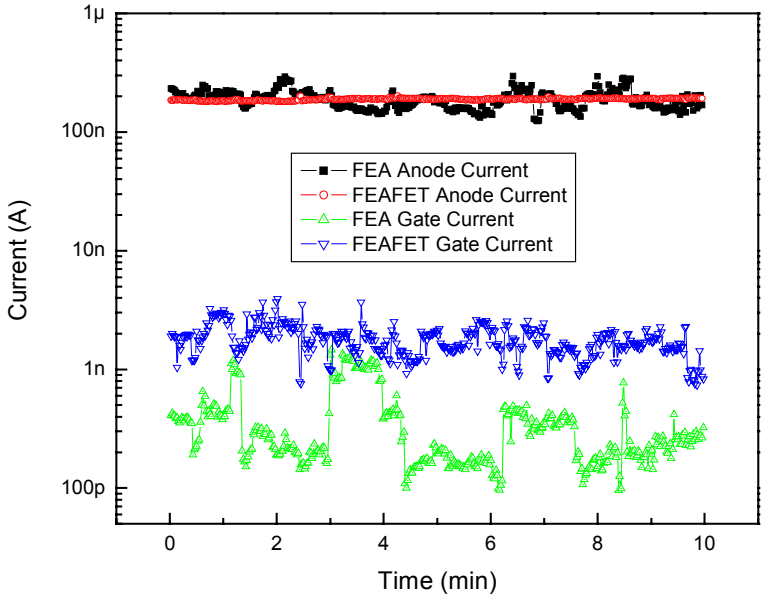


Figure 6-17. FEA extraction gate current and anode current comparison in an integrated LD-MOSFET/FEA device with and without MOSFET operation. V_{GFEA}= 44 V in the FEA device, while V_{GFEA}= 56 V in the integrated device to obtain the same anode current level.

The sources of the FEA extraction gate leakage were explored utilizing the integrated LD-MOSFET/FEA device. Figure 6-18 shows the gate current and anode current when the integrated LD-MOSFET/FEA device is turned on and off by switching the LD-MOSFET gate voltage. The FEA extraction gate current is low when the integrated device is off even at high FEA extraction gate voltages. On the other hand, the FEA extraction gate current is high when the integrated device is on at the same high FEA extraction gate voltages. This suggests that the extraction gate current must be in fact coming from the emission current. Part of the emission current was not collected by the

anode but by the FEA extraction gate. The other gate leakages such as current though the bulk of the insulator layer and along the surface of the insulator are low. These leakages start to increase when the FEA gate voltage exceeds 50 V as shown in the off state in Figure 6-18.

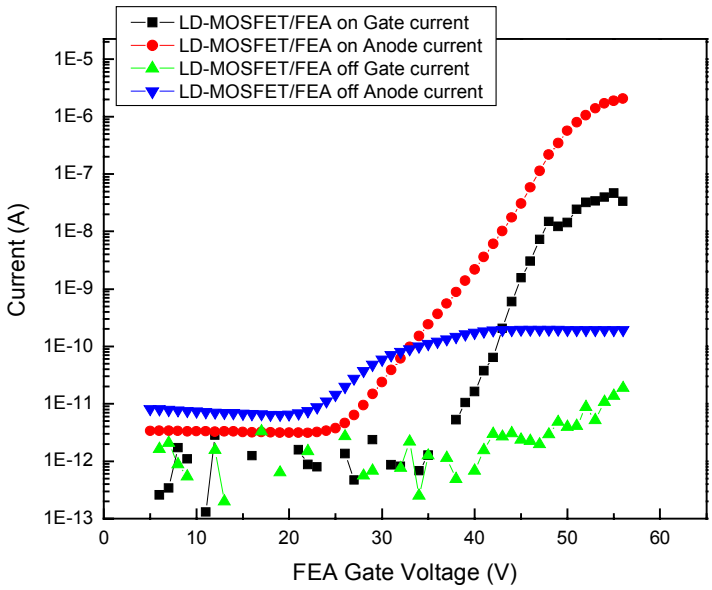


Figure 6-18. Gate leakage and anode current comparison in an integrated LD-MOSFET/FEA device when the device is on and off.

Temporal Stability

When the integrated LD-MOSFET/FEA is in the MOSFET control regime as shown in Figure 6-14, the saturation current is stable. When the integrated LD-MOSFET/FEA is in the FEA control regime as shown in Figure 6-16, the saturation current has large fluctuations. Therefore, the integrated device has to be operated in the MOSFET control regime in order to have stable anode current. In this section, the emission current stability at different current levels, pressures and gasses of both FEA devices and the integrated LD-MOSFET/FEA devices are reported. A comparison of the emission current fluctuations in the FEA, LD-MOSFET and integrated LD-MOSFET/FEA devices

at the current of 1 μA in the vacuum of 10^{-9} Torr is shown in Figure 6-19. The currents were monitored for 10 minutes. The current fluctuation is significantly reduced when the MOSFET is integrated with the FEA and the integrated device is operated in the MOSFET control regime. The anode current fluctuation ΔI/I is reduced from 11.8% to 2.6% when a MOSFET is integrated with the FEA. The current fluctuation is reduced by a factor of 5. It is noted that the anode current of the LD-MOSFET/FEA still has larger fluctuation than the drain current of the MOSFET. Theoretically, the two currents should be the same when the V_{GS} and V_{DS} are the same. The possible reasons of the larger current fluctuation in the LD-MOSFET/FEA are as follows. First, the fluctuations in transmission of the surface barrier could be large enough to move the operating point of the MOSFET out of its saturation region. Second, when the emission current is monitored, only part of the emission current is collected by the anode and part of the current would be collected by the extraction gate, unlike the drain current of the LD-MOSFET which is collected by direct probing on the drain contact. Third, channel length modulation also plays a minor role.

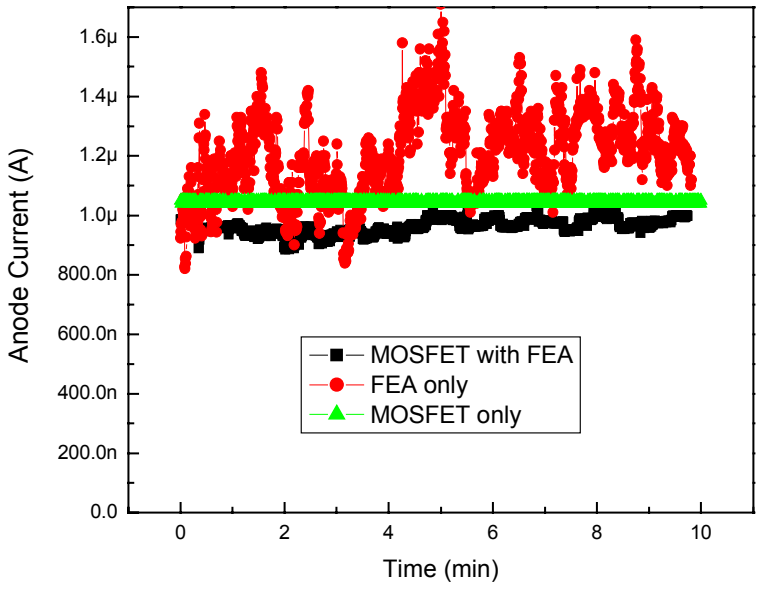


Figure 6-19. Emission current stability in a FEA, LD-MOSFET, and integrated LD-MOSFET/FEA device. V_{GFEA}=56 V and V_{GFET}=0.6 V when operating LD-MOSFET/FEA and V_{GFEA}=53.5 V when operating FEA.

Referring to the sensitivity issue we addressed in Chapter 2, the LD-MOSFET functions as a high dynamic resistance. From Figure 6-6, the output resistance of the transistor in the saturation regime is ~ $5\text{x}10^7$ Ω. Substituting the resistance into the following equation,

$$I_E = \frac{\alpha A \beta^2}{1.1\phi} \exp\left[\frac{B\left(1.44\times10^{-7}\right)}{\phi^{1/2}}\right]\left(V_{GFEA} - (I_E - I_0)R\right)^2 \exp\left[-\frac{0.95B\phi^{3/2}}{\beta\left(V_{GFEA} - (I_E - I_0)R\right)}\right] \tag{6.6}$$

where

$$I_{current\_source} \approx I_0 + I_R \tag{6.7}$$

$$I_{current\_source} = I_E \tag{6.8}$$

$$I_R = I_E - I_0 \tag{6.9}$$

R is the dynamic resistance of the current source, $I_{current\_source}$ is the current from the current source, I_0 is the current provided by the current source, I_R is the current flow through the dynamic resistor in the current source, and I_E is the current flow through the emitter. We will be able to obtain $\frac{\partial I}{\partial \phi}$ by substituting the numbers into the equation we derived in Chapter 2. The average current is 963 nA, and the corresponding ϕ = 4.01 eV by assuming I_0= 900 nA,

$$\frac{\partial I}{\partial \phi} = -3.64\times10^{-7}$$

$$\frac{\Delta I}{I} = \frac{\partial I/\partial \phi}{I}\times\Delta\phi = -0.38\times\Delta\phi \tag{6.10}$$

For the FEA only device, the average current is 1.21 μA, and the corresponding ϕ = 3.96 eV,

$$\frac{\Delta I}{I} = \frac{\partial I/\partial \phi}{I}\times\Delta\phi = \left[\frac{-1}{\phi} - \frac{0.72\times10^{-7}B}{\phi^{3/2}} - \frac{1.425\phi^{1/2}B}{\beta V}\right]\times\Delta\phi\,. \tag{6.11}$$

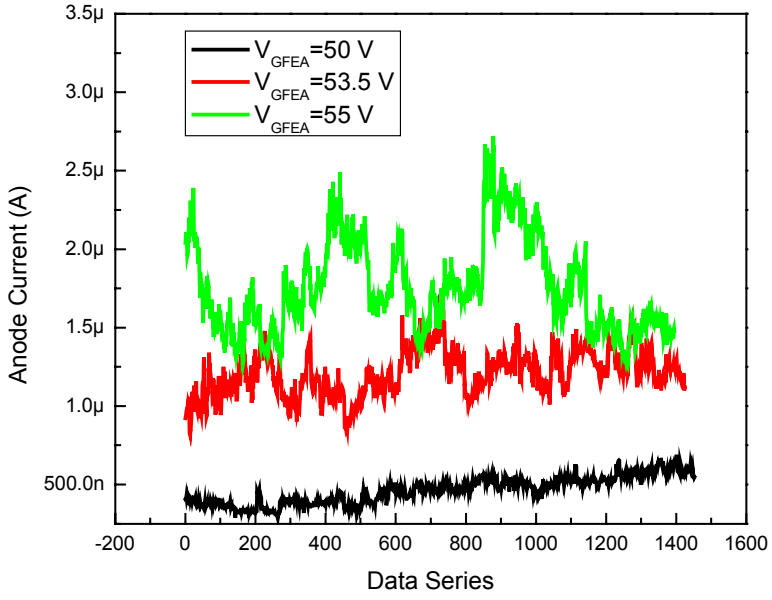
$$\frac{\Delta I}{I} = -3.39\times\Delta\phi \tag{6.12}$$

The corresponding work functions of both FEA and integrated devices were extracted from the FN equations by assuming the tip radius and other parameters are the same in

both devices. The difference of the work function values of the FEA and integrated device might come from the difference of the average emission current. It is obvious that the current fluctuation ΔI/I in FEA is about 10 times larger than LD-MOSFET/FEA if the work function fluctuation (Δϕ) is the same for both FEA and LD-MOSFET/FEA devices. This fits with our experimental data reasonably well.

Current fluctuations of an integrated device with/without MOSFET operation were also monitored at different current levels as shown in Figures 6-20 (a) and (b). We also denote the one with the MOSFET operation the integrated device and the one without the MOSFET operation the FEA device. The current fluctuation (ΔI/I) is summarized in Table 6-1. The integrated device has much smaller current fluctuation than FEA device at every current level. Anode current fluctuation in the FEA device is random and does not depend on the current level; however, ΔI is larger at higher current level. On the other hand, the anode current fluctuation in the integrated device is lower at higher current levels.

(a)



(b)

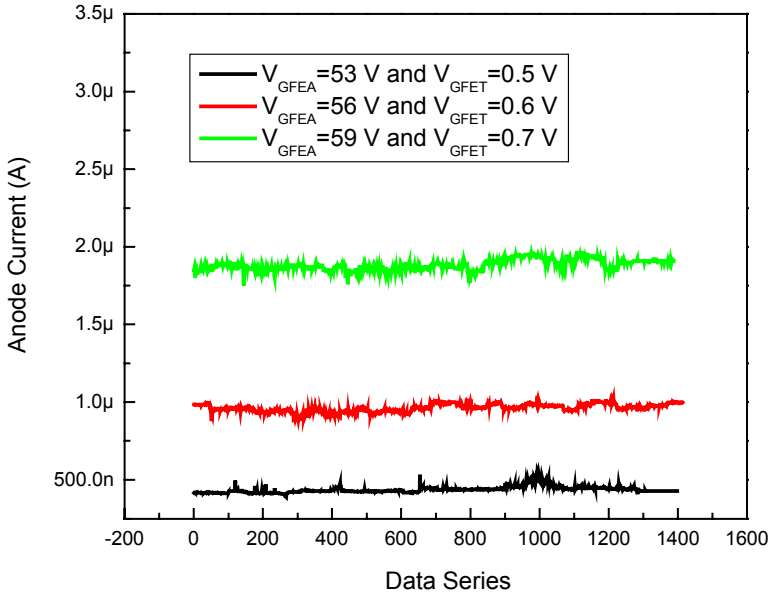


Figure 6-20. Emission current stability in an integrated LD-MOSFET/FEA device (a) without and (b) with MOSFET control in three different current levels.

Table 6-1. Current fluctuation (ΔI/I) in an integrated LD-MOSFET/FEA device with and without MOSFET control in three different current levels.

	I_A = 0.4 μA	I_A = 1.0 μA	I_A = 1.8 μA
FEA only	18.3%	11.8%	16.9%
LD-MOSFET/FEA	4.6%	2.6%	1.8%
Ratio of current fluctuation with and without LD-MOSFET	0.25	0.22	0.11

Sensitivity reduction analysis of the integrated LD-MOSFET/FEA could be done similar to the previous section comparing with the FEA temporal stability analysis presented in Section 5.2. Since

$$\frac{\Delta I}{I} = \frac{\partial I / \partial \phi}{I} \times \Delta \phi , \tag{6.13}$$

$\frac{\partial I / \partial \phi}{I}$ for both devices at three different current levels can be extracted. The output resistance of the transistor in the saturation regime is ~ $5x10^7$ Ω. Table 6-2 summarizes the extracted values. Assuming the work function fluctuation (Δϕ) is the same at the same current level for both FEA and LD-MOSFET/FEA devices, current fluctuation is proportional to $\frac{\partial I / \partial \phi}{I}$. This fits with our experimental data reasonably well. It is proven that integrated LD-MOSFET/FEA has less sensitivity to work function changes and leads to more stable emission current.

Table 6-2. Extracted $\frac{\partial I / \partial \phi}{I}$ in an integrated LD-MOSFET/FEA device with and without MOSFET control in three different current levels.

	I_A = 0.4 μA	I_A = 1.0 μA	I_A = 1.8 μA
FEA only	-3.57	-3.39	-3.32
LD-MOSFET/FEA	-0.7	-0.38	-0.22
Ratio of $\frac{\partial I / \partial \phi}{I}$ with and without LD-MOSFET	0.20	0.11	0.07

The integrated LD-MOSFET/FEA device was then characterized for the response of its emission current to hydrogen gas [6.2-6.3]. The hydrogen input was the same as described in Chapter 5 where the FEA device was characterized for the response of the emission current to hydrogen. The pressures and gas atmospheres were as follows: $5x10^{-8}$ Torr without hydrogen -- $1x10^{-7}$ Torr with hydrogen -- $5x10^{-7}$ Torr with hydrogen -- $5x10^{-8}$ Torr without hydrogen. The anode current response for the FEA device shown in Figure 5-12 was compared with the current response for the integrated device as shown in Figure 6-21. The anode current of the integrated LD-MOSFET/FEA is unchanged regardless the gas and vacuum conditions while the FEA device response to gas input is

very dramatic. The integrated LD-MOSFET/FEA device achieves current stability and reduced noise even in the presence of gas molecules. The same characterization was repeated with nitrogen and argon as shown in Figures 6-22 and 6-23. The anode current responses are similar to that of hydrogen. The responses of the FEA device to different gases are different; but LD-MOSFET definitely stabilized the emission current from the FEA device in all gas ambient tested.

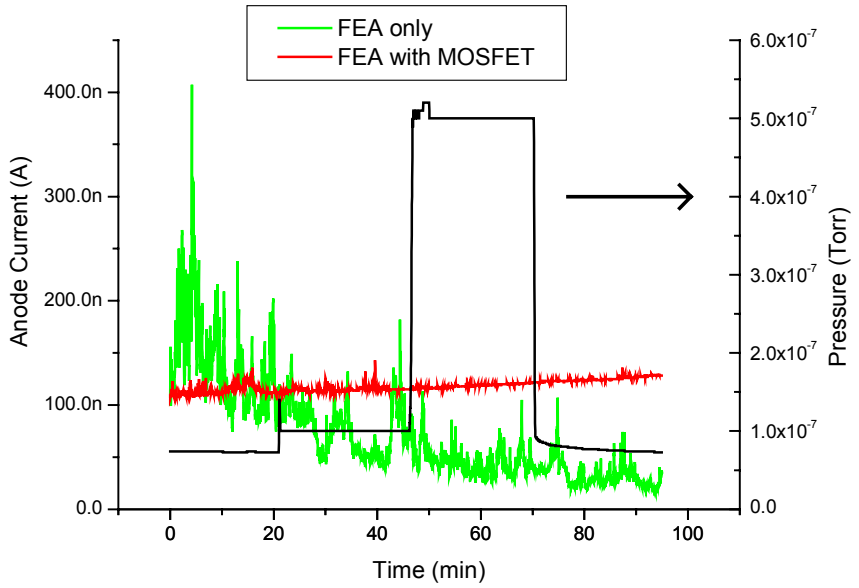


Figure 6-21. Emission current stability in an integrated LD-MOSFET/FEA device with and without MOSFET control in hydrogen.

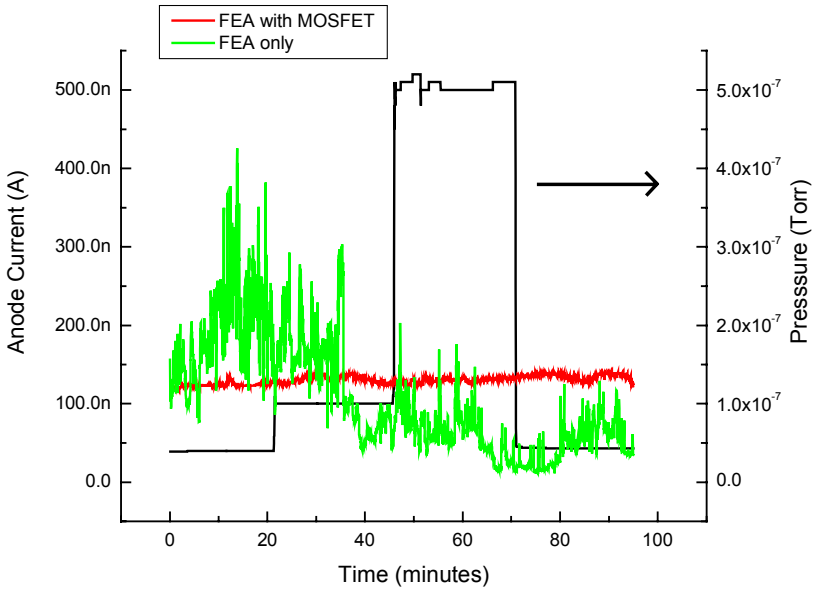


Figure 6-22. Emission current stability in an integrated LD-MOSFET/FEA device with and without MOSFET control in nitrogen.

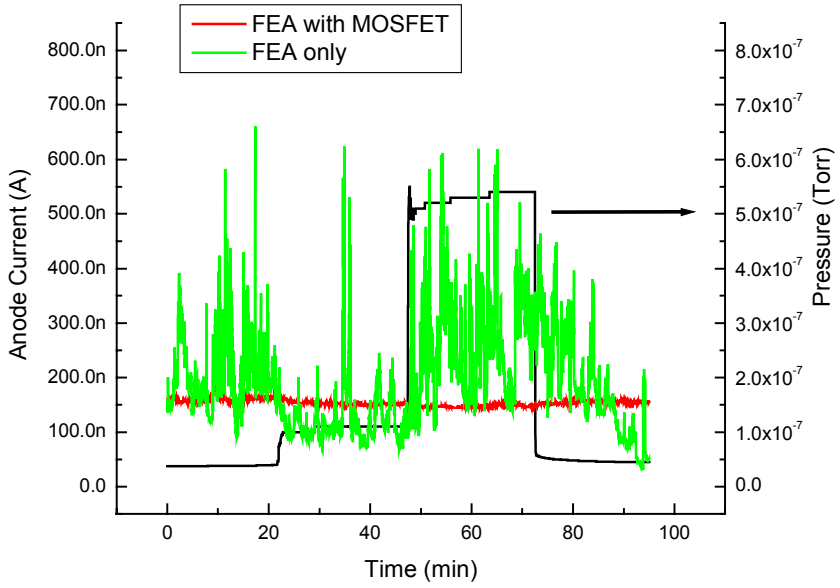


Figure 6-23. Emission current stability in an integrated LD-MOSFET/FEA device with and without MOSFET control in argon.

We attribute the reduction in current fluctuation to the control of emission current by the electron supply, which is not affected by work function changes that may occur due to adsorption-desorption processes or field enhancement changes.

Spatial Current Uniformity

As mentioned in Section 3.2, emitter tip radius has a log-normal distribution and ranges from 1.5 nm to 19 nm. Smaller tip radius emitters dominate the emission process as discussed in Section 5.2. The tip radius ranges and the percentage of the sharper emitters vary slightly across the wafer even with careful fabrication. These slight variations in tip radius would result in large variation in emission current due to the exponential dependency. Spatial current uniformity was next examined on the integrated devices with the same device dimensions but at different positions on the wafer. Die 45 (the die is on row 4 and column 5 of the wafer) is at the left side of the wafer, die 65 is at the right side, and die 54 is at the upper side. Die 45 and die 65 are about 2 cm apart; die 45 and die 54 are 1.5 cm apart. The anode currents of different integrated devices were monitored while the FEA gate voltage was swept from 0 to 70 V as shown in Figure 6-24. The LD-MOSFET was biased so that the difference between the MOSFET gate voltage and the threshold voltage (ΔV_{GS}) is 0.5 V. ΔV controls the amount of electrons that can pass through the MOSFET channel and therefore the electron supply to the emitter surface. Three different devices show different turn-on voltages and saturation voltages in the FEA controlled regime. However, the saturation current level, which is determined by the MOSFET, is the same regardless the FEA's position on the wafer. The LD-MOSFET was also biased at ΔV_{GS} of 0.4 V, lower saturated current was obtained and similar results were observed. Similar to previous sections, the saturation voltage can be predicted numerically. In this particular device, take die 54 for example,

$a_{FN} = 7.83 \times 10^{-7}$,

$b_{FN} = 585.48$ (extracted from FEA of this integrated device),

$$I_A = 7.83 \times 10^{-7} \times (V_{GE})^2 \exp\left[\frac{-585.48}{(V_{GE})}\right], \tag{6.14}$$

$$I_{D\_sat} = 0.17 \times 10^{-6} \text{ A}$$

when ΔV is 0.5 V,

$V_{GE} = 60.5$ V.

$V_{transition} = V_{GFEA} = V_{GE} + V_{DS_sat} \sim 61.5$V

because the onset of the MOSFET saturation $V_{DS\_sat} \sim 1$ V as shown in Figure 6-2. This predicted saturation voltage is reasonably close to the actual voltage, 58 V.

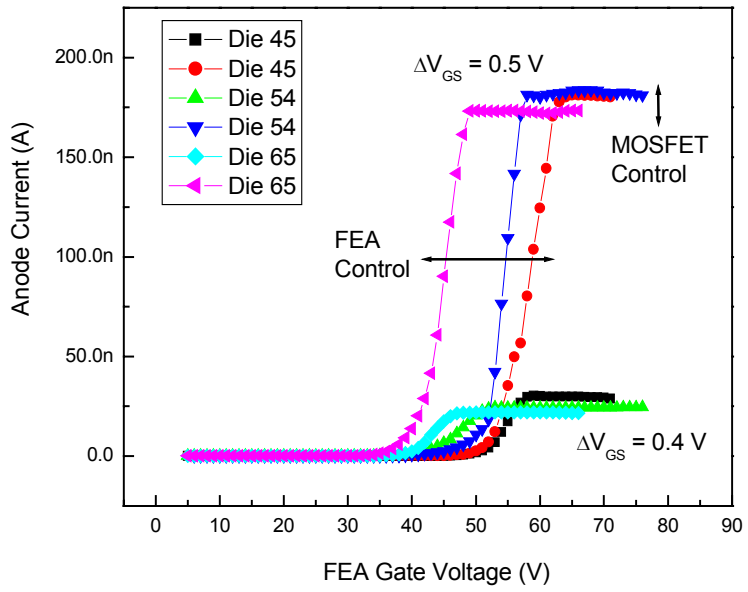


Figure 6-24. Spatial emission current uniformity in the integrated LD-MOSFET/FEA devices at different positions on the wafer. ΔV_{GS} is 0.5 V (anode current is 170 nA) and 0.4 V (anode current is 25 nA).

The same characterization was repeated on two integrated devices with the same LD-MOSFET dimensions but different array sizes: 10x10 emitters and 20x20 emitters. It is obvious that the turn-on voltages and saturation voltages of the two devices are different as shown in Figure 6-25 due to different number of emitters. When the emission current is controlled by electron supply, the LD-MOSFET dimension controls the current magnitude, and the saturation current level is the same regardless of the array size.

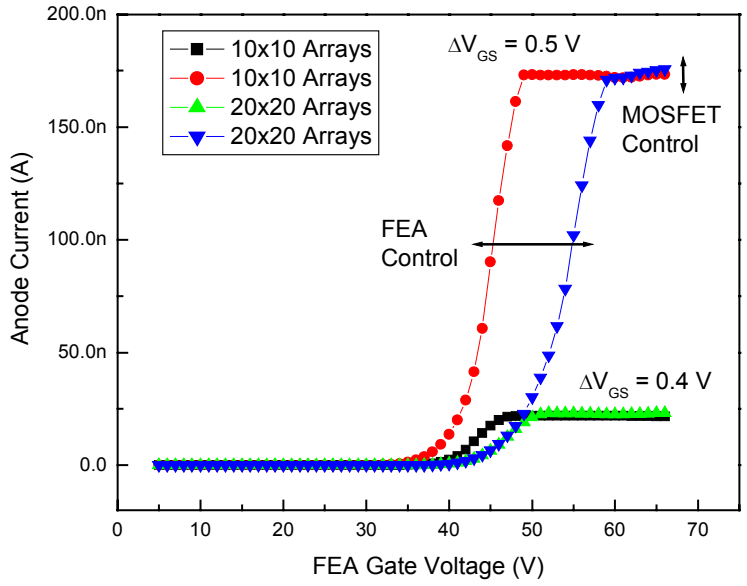


Figure 6-25. Spatial emission current uniformity in two integrated LD-MOSFET/FEA devices with different array sizes. ΔV_{GS} is 0.5 V (anode current is 170 nA) and 0.4 V (anode current is 25 nA).

Saturation voltage can be predicted as follows. In this particular device and take 10x10 FEA for example,

$a_{FN} = 3.93 \times 10^{-5}$,

$b_{FN} = 614.08$,

$$I_A = 3.93 \times 10^{-5} \times (V_{GE})^2 \exp\left[\frac{-614.08}{(V_{GE})}\right], \qquad (6.15)$$

$$I_{D\_sat} = 0.17 \times 10^{-6} \text{ A}$$

when ΔV is 0.5 V,

$V_{GE} = 47$ V.

$V_{transition} = V_{GFEA} = V_{GE} + V_{DS\_sat} \sim 47$ V

because the onset of the MOSFET saturation $V_{DS\_sat} \sim 1$ V as shown in Figure 6-2. This predicted saturation voltage is very close to the actual voltage, 48.5 V.

Low Voltage Switching of the LD-MOSFET/FEA

Next, the switching frequency of the integrated LD-MOSFET/FEA device was examined. In this thesis, ultra-high switching frequency of the device is not the main objective; however, we would like to know how well the low voltage control LD-MOSFET can switch the integrated device and obtain stable emission current. The particular integrated device we monitored has a FEA of 10x10 emitters and a LD-MOSFET with channel width of 4 μm, channel length of 100 μm, and drift length of 10 μm. The MOSFET gate was controlled by a step function that switched between of 0 and 1.4 V to toggle integrated device off and on respectively while the FEA extraction gate voltage was kept constant at 65 V. The emission current was converted into voltage (1 μA to 1 V) by current-voltage converter and monitored by oscilloscope. In this setup, the oscilloscope can only monitor the electrode that is grounded because it does not supply voltage. The anode needs to be grounded while other electrodes need to be offset by -1000 V. However, the extraction FEA gate leakage is less than 0.1% of the anode current and the MOSFET gate leakage is less than 1 pA in this integrated device at the operating FEA extraction voltage. We can assume that the anode current is the emitter current. The current from the emitter electrode was monitored by the oscilloscope instead of the current from the anode electrode. The step signal had 50 % duty without offset and the frequency of switch was increased from 1 Hz to 100 KHz in different sets of measurements. The results are shown in Figure 6-26. The emission current can be switched between 0 and 0.35 μA up to 10 KHz. The current fluctuations of the on currents are 1%, 1.2% and 1.8% when the frequencies are 1 Hz, 10 Hz and 10 KHz. The device seems to pick up some undesired noise at frequency of 10 Hz. It is believed that the noise is not from the device itself but from the surrounding equipment. When the frequency went up to 1 KHz, the current had an overshoot. When the frequency went up to 100 KHz, the device was unable to respond to the applied voltage. Usually, the switching frequency higher than 80 Hz in the display would not be apparent to the human eye. The switching frequency shown in this device is adequate for most of the field emission applications. In conclusion, we can switch the device using a small voltage swing and obtain stable emission current in the integrated LD-MOSFET/FEA device.

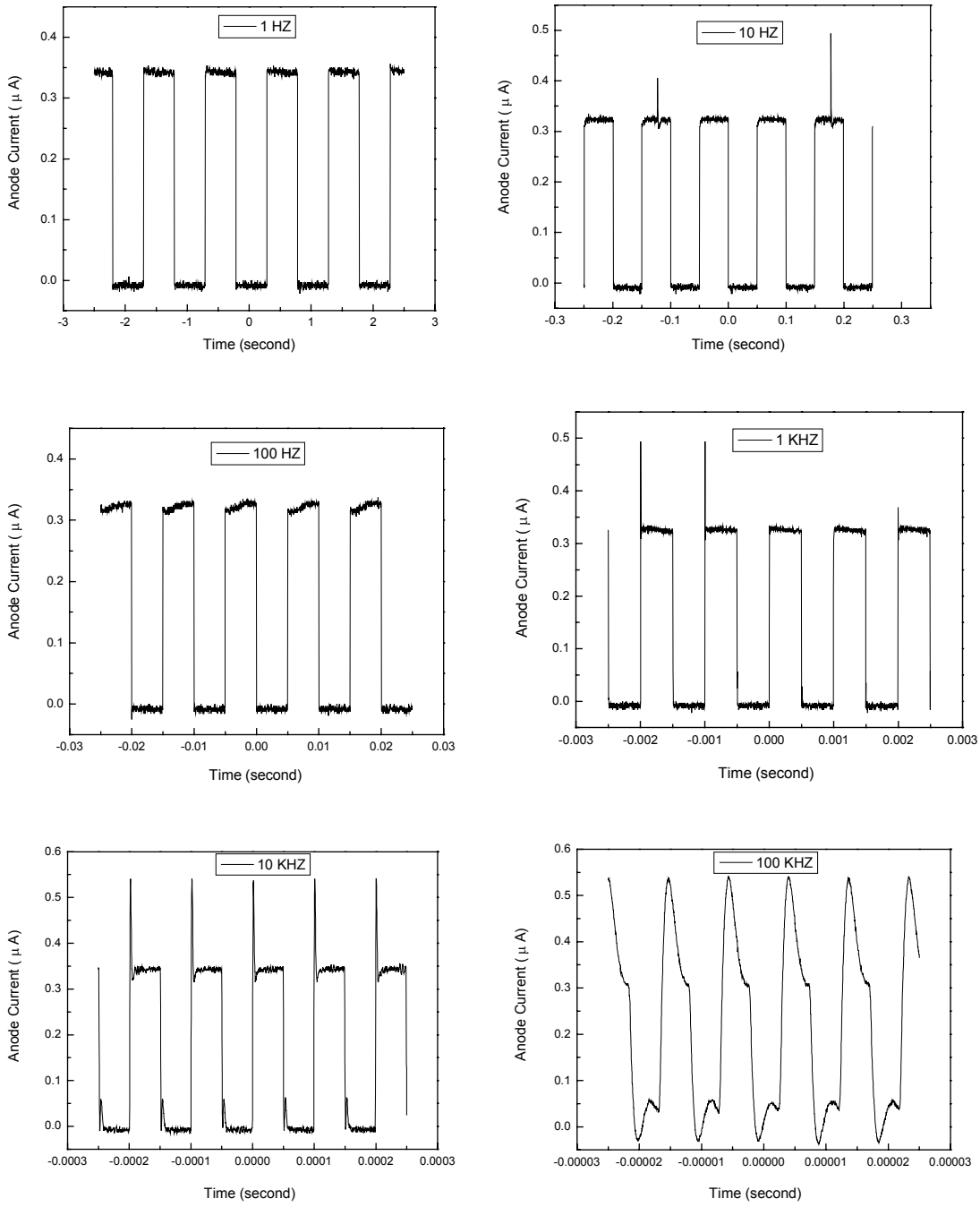


Figure 6-26. The switch of an integrated LD-MOSFET/FEA device in different step function frequencies.

A simple model is constructed to show the switch frequency of the integrated MOSFET/FEA device. Figure 6-27 shows the equivalent circuit of the integrated device

with capacitors. The current summation at any node in the circuit equals zero (Kirchhoff's Current Law). In other words, the sum of current into a node equals the sum of current going out of a node.

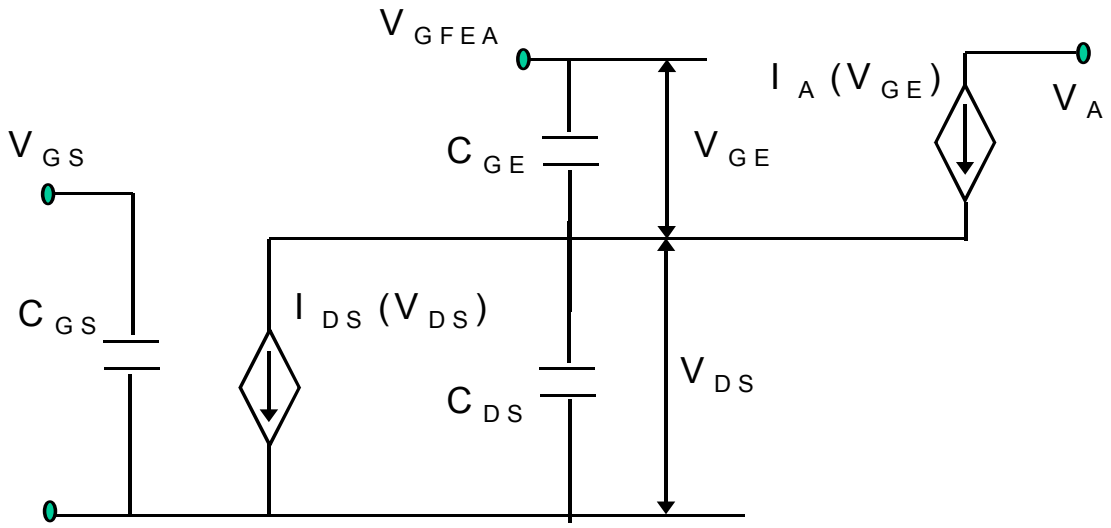


Figure 6-27. Equivalent circuit of an integrated device with capacitors for switch model.

We can write a differential equation for the node between the MOSFET drain and the emitter of the FEA.

$$I_D(V_{GS}) - I_A(V_{GE}) - C_{GE}\frac{d}{dt}[V_{GFEA} - V_{DS}] + C_{DS}\frac{dV_{DS}}{dt} = 0\,, \qquad (6.16)$$

where I_D is the drain current of the MOSFET, V_{GS} is the MOSFET gate voltage, C_{GE} is the emitter capacitance, and C_{DS} is the MOSFET channel capacitance. Assuming the integrated device is working in the MOSFET control regime and the drain current is the MOSFET saturation current.

$$I_D = I_{D\_sat} = \frac{\mu C_{GS} W}{2L}(V_{GS} - V_T)^2(1 + \lambda V_{DS})\,, \qquad (6.17)$$

where μ is electron mobility, C_{GS} is the MOSFET gate capacitance, W is the MOSFET channel width, L is the MOSFET channel length, V_T is the MOSFET threshold voltage, and λ is the channel length modulation parameter in MOSFET saturation current. Anode current is assumed the same as emission current.

$$I_A = a_{FN} V_{GE}{}^2 \exp\left[\frac{-b_{FN}}{V_{GE}}\right], \tag{6.18}$$

and

$$V_{GFEA} = V_{GE} + V_{DS}\,. \tag{6.19}$$

Therefore,

$$I_A = a_{FN}\left(V_{GFEA} - V_{DS}\right)^2 \exp\left[\frac{-b_{FN}}{\left(V_{GFEA} - V_{DS}\right)}\right]. \tag{6.20}$$

Since V_{GFEA} is kept constant and the integrated device is solely switched by the MOSFET gate voltage,

$$C_{GE}\frac{d}{dt}\left[V_{GFEA} - V_{DS}\right] + C_{DS}\frac{dV_{DS}}{dt} = \left[C_{GE} + C_{DS}\right]\frac{dV_{DS}}{dt} = I_A - I_D\,. \tag{6.21}$$

This equation is solved by *Matlab* numerically. For simplicity, the depletion semiconductor capacitance is used for $C_{DS.}$ Emitter capacitance (C_{GE}) can be approximated by the parallel plate capacitance between the gate electrode and the base of the emitters, which is given by

$$C_{GE} = \varepsilon\varepsilon_0\left(\frac{A}{d}\right), \tag{6.22}$$

where ε is the permittivity of the gate-to-base insulator, A is the area of the gate electrode that overlaps the base area, and d is the thickness of the insulator. More exact calculations of the capacitance take into account the effect of gate apertures, undercut in the gate-to-base insulator, and fringing capacitance between the emitter and the gate electrode. This particular device has a MOSFET with channel length of 100 μm, channel width of 4 μm, and a FEA with 10x10 emitters,

$a_{FN} = 3.14 \times 10^{-7}$,

$b_{FN} = 370$ (from section 5-2),

$V_{GFEA} = 50$ V,

$$I_A = 3.14\times10^{-7}\times\left(50 - V_{DS}\right)^2 \exp\left[\frac{-370}{\left(50 - V_{DS}\right)}\right], \tag{6.23}$$

$$I_D = 3.5\times10^{-7}\times\left(1 + 0.01\times V_{DS}\right), \tag{6.24}$$

$$C_{GE} = \varepsilon\varepsilon_0\left(\frac{A}{d}\right), \tag{6.25}$$

$$C_{GE} = 3.9\times 8.85\times 10^{-14}\times\left(\frac{200\times 10^{-4}\times 200\times 10^{-4}}{700\times 10^{-7}}\right) = 1.97\times 10^{-12} \text{ (farad)},$$

$$C_{DS} = \frac{\varepsilon_{silicon}\varepsilon_0 A}{w}\times 2, \tag{6.26}$$

where $\varepsilon_{silicon}$ is the permittivity of the silicon, w is the depletion width (the maximum equilibrium depletion width is ~ 0.1 μm when the channel doping N_A is 10^{17} cm^{-3}). The reason for the factor of 2 term in C_{DS} is because there is another 100-μm drift length under the MOSFET gate to have another capacitor parallel to the capacitor from the original channel.

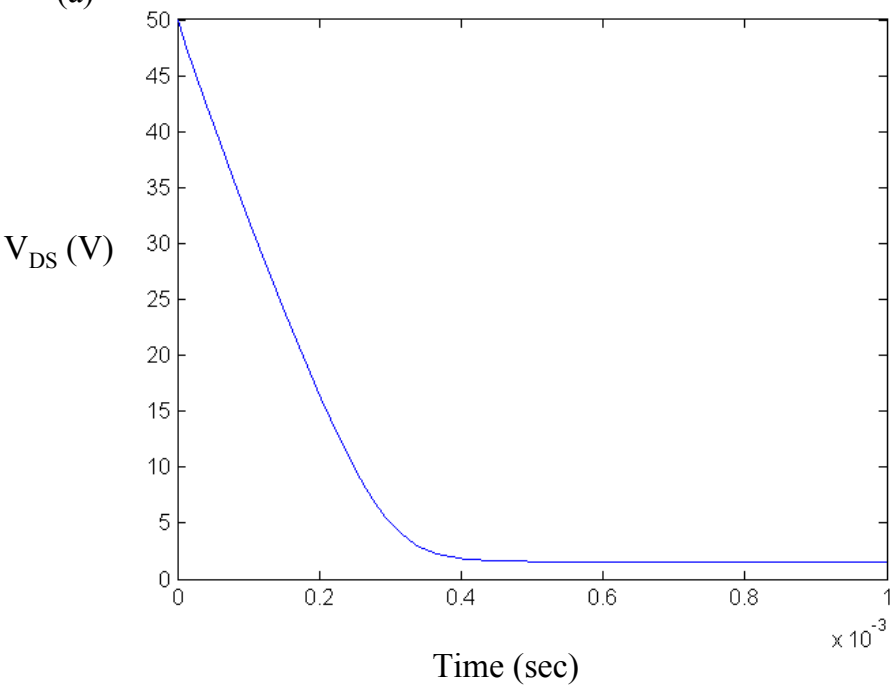
$$C_{DS} \approx \frac{11.8\times 8.85\times 10^{-14}\times 4\times 10^{-4}\times 100\times 10^{-4}}{0.1\times 10^{-4}}\times 2 = 8.36\times 10^{-13} \text{ (farad)}.$$

Therefore,

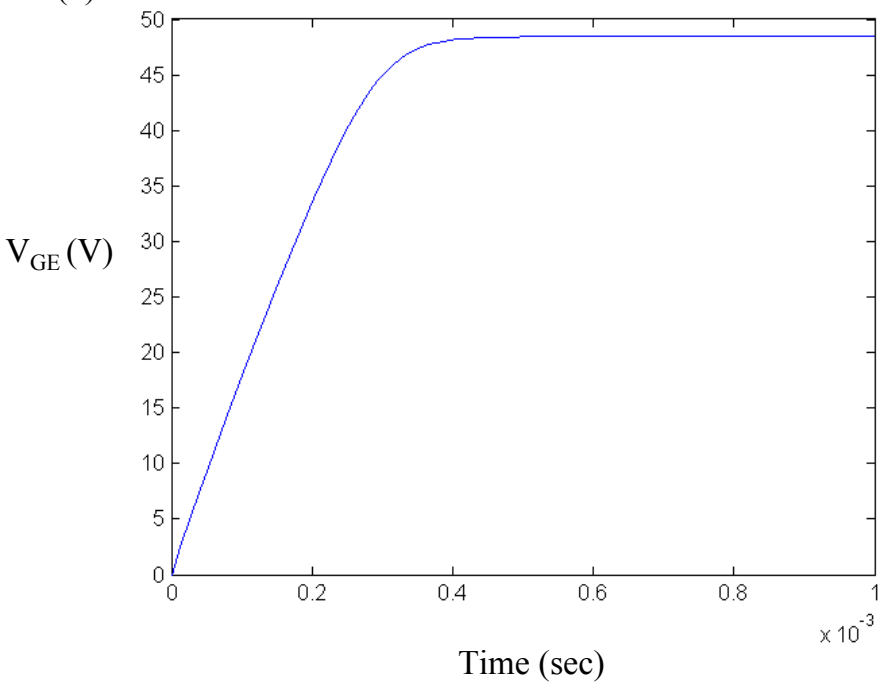
$$\frac{dV_{DS}}{dt} = \frac{I_A - I_D}{C_{GE} + C_{DS}}. \tag{6.27}$$

By substituting all the numbers, Figures 6-28 (a)-(c) show V_{DS}, V_{GE}, and I_A changes with time. The time constant is 0.4 ms. In other words, the limiting frequency of this particular device should be 2.5 KHz. The simulation is a reasonable fit to our experimental data. The smaller the sum of C_{GE} and C_{DS}, the faster the MOSFET can switch the integrated device. The thickness of the insulator can be increased or the dielectric constant can be lower by using insulating materials other than silicon dioxide to increase C_{GE}.

(a)


V_{DS} (V)
50
45
40
35
30
25
20
15
10
5
0
0
0.2
0.4
0.6
0.8
1
x 10^-3
Time (sec)

(b)


V_{GE} (V)
50
45
40
35
30
25
20
15
10
5
0
0
0.2
0.4
0.6
0.8
1
x 10^-3
Time (sec)

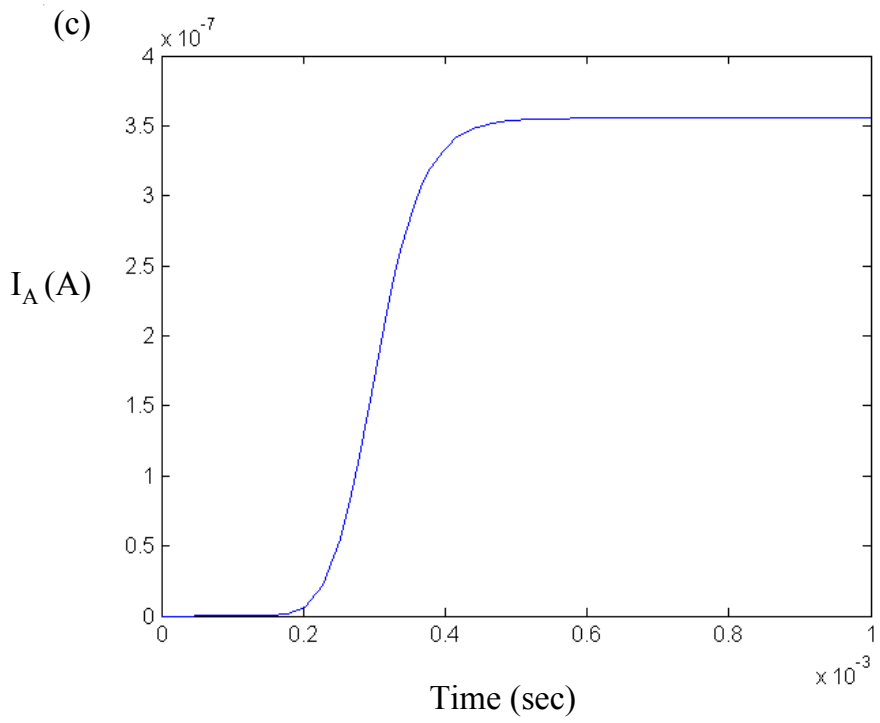


Figure 6-28. (a) Drop of V_{DS}, (b) increase of V_{GE}, and (c) increase of I_A with time.

Power Dissipation in the FEA and Integrated LD-MOSFET/FEA Devices

The sources of the power dissipation for the field emission devices are mostly from the electron acceleration (electron collection at the anode), gate leakage (or electron recollection), and addressing power. For a field emission application that consists of a large amount of FEAs, the addressing power is the main power dissipation source. In order to compare the power dissipation in the FEA and the integrated LD-MOSFET/FEA devices, we take the devices from Figure 6-19 for example. For the same on-current, in the FEA device, the energy for addressing the devices

$$E_{FEA} \approx \frac{1}{2} C_{FEA} V_{GFEA}{}^2 = \frac{1}{2} \times (2 \times 10^{-12}) \times 53.5^2 = 2.9 \times 10^{-9} \text{ (J)} \qquad (6.28)$$

In the integrated device, even though V_{GFEA} is larger, the addressing voltage is V_{GFET},

$$E_{integratedFEA} \approx \frac{1}{2} C_{MOSFET\_gate} V_{GFET}{}^2 = \frac{1}{2} \times (6.9 \times 10^{-12}) \times 0.6^2 = 1.2 \times 10^{-12} \text{ (J)} \qquad (6.29)$$

If we switch the devices at the same frequency, power dissipation ∝ energy. Therefore the power dissipation in the integrated device is less than the one in the FEA device.

Comparison of the Integrated Transistor/FEA Results with the Literature

Excellent I-V characterization results have been obtained from the integrated MOSFET/FEA devices reported by Itoh *et al.* [6.2-6.8]. The gate voltage required to obtain a field emission current of 0.1 μA is about 48 V. For the devices they reported most recently, the emission current is effectively controlled by the MOSFET at a gate voltage of less than 5 V. They demonstrate the switch frequency of 1 Hz with less than 1 % on current fluctuation. We do have similar device structure with Itoh's group. However, the fabrication process is somewhat different, and some of the materials selections and the device dimensions for both MOSFET and FEA are also different as discussed in Chapter 4. The main drawback of Itoh's device is low on/off current ratio, and the limited switch frequency might not be suitable for most of the field emission application. The MOSFET controlled regime can be achieved at much lower FEA extraction gate voltage in our devices than Itoh's. The comparison of our devices with Itoh's devices is summarized in Table 6-3.

Table 6-3. Comparison of our devices with Itoh's devices.

	Itoh *et al.*	Hong *et al.*
MOSFET gate voltage sweep	< 5 V	< 2 V
Switching frequency cut-off	1 Hz	10 K Hz
On current fluctuation at 1 Hz switch	< 1 %	1-2 %
ON/OFF current ratio	~ 32:1	>1000:1
FEA gate voltage at which MOSFET control starts	~ 65 V	~ 50 V

Other than Itoh's group, Yokoo *et al.* [6.9] also demonstrated the stabilization of the emission current in a field emitter arrays by adding a commercially available MOSFET. However, their results are rather preliminary and without quantitative information.

Recently, Itoh's group [6.10] and J. H. Lee *et al.* [6.11] integrated amorphous silicon thin film transistor (a-Si TFT) with the field emitter arrays and Hashiguchi *et al.* [6.12] reported the integration of polycrystalline silicon thin film transistor (poly-Si TFT) with polycrystalline silicon field emitters. The emitter materials are a-Si in Itoh's device and Mo in Lee's device. Itoh reported the switching of the FEA with transistor gate voltage swing of less than 15 V with the FEA extraction gate is biased at 150 V. The a-Si TFT device has a channel width of 100 μm and a gate length of 10 μm, and the FEAs has 1000 a-Si tips. Lee reported an ON/OFF ratio of greater than 1000:1 for field emission current with transistor gate voltage swing of more than 30 V with the FEA extraction gate is biased at > 55 V. The a-Si TFT device has a channel width of 150 μm and a gate length of 30 μm, and the FEAs has 400 Mo tips. Lee also reported the stabilization of the field emission current by the a-Si TFT. Hashiguchi reported well-controlled emission current by poly-Si TFT in their preliminary results; however, the TFT devices are not optimized yet.

Shimawaki *et al.* [6.13] reported a monolithic FEA integrated with a junction field effect transistor (JFET). The process is simple and the emission current shows well-controlled characteristics by the JFET. The 5-tip FEA can be switched by JFET with the gate voltage swing of 0.1 V in the switching frequency of 0.5 Hz to get the ON/OFF current ratio of 4 (0.4 nA/0.1 nA) when the FEA gate voltage is biased at 38 V and anode voltage is biased at 200 V. The field emission current is stabilized by the JFET.

Finally, Binh *et al.* reported a similar concept of using electron supply to modulate the field emission [6.14]. They adapted a solid-state Schottky metal-semiconductor barrier to inject electrons into a field-controlled negative electron affinity surface, which is an ultra-thin semiconductor layer. They successfully confirmed the two serial emission processes mechanism: electron injection followed by electron emission. At low anode voltage (but

above threshold), the emission is controlled by electron tunneling through surface barrier; at high anode voltage, the emission is controlled by Schottky barrier. When the emission is controlled by Schottky barrier, the stability of the current is not affected by the pressure of the environment. On the other hand, the emission current varies with temperature in the electron injection controlled regime because electrons jump over the Schottky barrier by thermionic-like mechanism.

6.3 Chapter Summary

In this chapter, we introduced the LD-MOSFET device and presented the output/transfer characteristics of the LD-MOSFET devices. We obtained a well-behaved LD-MOSFET with the an average threshold voltage of 0.5 V, breakdown voltage of 36 V, and subthreshold slope of 100 mV/decade after modifying the device layout to increase the breakdown voltage. Next, we characterized the integrated MOSFET/FEA device. We demonstrated very good control of the emission current by the gate voltage of the LD-MOSFET, and larger than 1000:1 ON/OFF current ratio was obtained with the MOSFET gate voltage swing of 0.5 V while the FEA extraction gate voltage was kept at 60 V. The source of the gate leakage current might be the emitted electrons collected by the extraction gate electrode instead of the anode electrode. The gate leakage current was about 1% of the anode current and was considered very low. The emission current fluctuation was reduced immensely in the integrated device compared to the FEA device. This current fluctuation reduction was also maintained in the presence of the gas molecules. We also presented the spatial current uniformity in the integrated LD-MOSFET/FEA devices at different wafer positions and array sizes. In one particular integrated device, the limitation of switching frequency was between 10 KHz and 100 KHz. It is beyond what we need for most of the field emission applications. A switch frequency model was demonstrated for the integrated MOSFET/FEA device. This switching frequency is in agreement with the model. Finally, the literature reports of the

integrated transistor/FEA device performance were presented and compared with our device performance.

7. Thesis Summary and Suggestions for Future Work

7.1 Thesis Summary

Silicon field emission arrays attracted a lot of attention recently because of their potential for wide applications in vacuum microelectronics. However, the non-uniformity, instability of emission current and high voltage control of the devices have been concerns for the silicon emitter arrays. This thesis used electron supply to modulate the emission process instead of electron transmission through the energy barrier by adopting MOSFET as a current source for the silicon field emission devices.

A novel process for integrating a LD-MOSFET as a current source with a FEA device using CMP technology was presented. The silicon field emitter arrays with self-aligned gate aperture of ~ 1.3 μm were successfully achieved. The average turn on voltage of the FEA is ~ 24 V. Gate current was less than 10 %, and in most cases less than 2 %, of the anode current. An analysis using TEM shows the tip radius has a log-normal distribution with the peak of 6.2 nm and the distribution width of 0.37 nm. The emission current fits Fowler-Nordheim equation very well with the following FN parameters: a_{FN} = (3.14±0.3) x 10^{-7} and b_{FN} = 369±4. We obtained the tip radius of 1.8 nm by fitting the emission current using numerical simulation. It is suggested that the sharp emitters in the field emission devices would dominate the emission current. Optimization of the silicon isotropic etching and oxidation sharpening process should further reduce the tip radius and distribution width. Furthermore, optimization of the CMP should reduce the operating voltage increase the emission uniformity.

A comprehensive oxidation sharpening study was conducted in this thesis. A new sharp emitter tip formation mechanism is proposed rather than a continuous oxidation process. Neck breaking occurs before the sharp emitter tip is formed. Stress from volume

difference of silicon and silicon dioxide is the main cause for the emitter neck breaking. Initial formation of microcracks at the neck surface occurs at high temperature due to volume difference stress and oxide grows into the cracks right after the crack formation. It is suspected that if the neck region is too thick for the volume difference stress to break the silicon bond, the combination of both volume difference stress and cool-down stress might be able to break the silicon neck at lower temperature. In the sharp emitter formation process, the microcracks formed by volume difference is more important because the neck needs to be further consumed by oxidation at high temperature. The stress-induced oxide growth reduction for three-dimension features was also presented in this thesis.

The LD-MOSFET has an average threshold voltage of 0.5 V and the subthreshold slope is about 100 mV/decade. The MOSFET has the breakdown of ~ 40 V, which is sufficient to compensate the field emission voltage spread at a desired current level. The LD-MOSFET/FEA transfer characteristics were obtained in two ways: the extraction gate voltage was varied while the MOSFET gate voltage was kept constant or the MOSFET gate voltage was varied while the extraction gate voltage was kept constant. The experimental results have good agreement with the device simulation by *MATLAB*. Both show the negative slope of a FN plot at the low extraction gate voltage where electron transmission dominates the emission process and slightly positive slope at the high extraction gate voltage where the electron supply dominates the emission. The operating mechanism of the MOSFET/FEA was presented in this thesis.

The most significant result of this work is that the LD-MOSFET shows good control on the FEA and greatly reduced the current fluctuation temporally and spatially. Whereas earlier literature reports provided only the reduction of current fluctuation temporally, we also showed the spatially uniform emission current by the same idea to modulating the emission current by electron supply. The MOSFET can stabilize the emission current even in the presence of the gas molecules. An additional benefit is the modulation of the emission current by a much lower voltage – the MOSFET threshold voltage that now controls electron emission is much lower than the FEA turn-on voltage. A MOSFET

voltage swing of less than 1 V can achieve an on/off current ration of more than 1000:1, which is excellent for most of the field emission device applications whereas the conventional FEA device required extraction gate voltage swing of about 45 V to obtain the required on/off current ratio. This results in much lower switching power consumption, which is an important characteristic for some field emission devices. The maximum switching frequency of the integrated device was up to 10KHz. It is also beyond what we need for most of the field emission applications. A switching frequency model for the integrated MOSFET/FEA device is consistent with measured data.

7.2 Main Contributions

The main contributions of this work are summarized as follows:

1. An original process for fabricating the LD-MOSFET/FEA devices was demonstrated. This process combined silicon isotropic/anisotropic etching and oxidation sharpening for silicon emitter formation, CMP for extraction gate aperture opening, and modification of the traditional MOSFET fabrication process.

2. We demonstrated the oxidation mechanism of the silicon emitter sharpening process. The neck breaking mechanism was first revealed and the three-dimensional oxidation behavior was first studied.

3. Spatial uniform and temporal stable emission current were obtained by integrating a LD-MOSFET with a FEA. The device design also resulted in low voltage control of the FEA.

4. A detailed theoretical framework of the operation of the integrated LD-MOSFET/FEA was provided.

7.3 Suggestions for Further Work

The single emitter is potentially an electron source for some sensors or e-beam lithography. A much better control of the electron emission is needed. Therefore, a MOSFET controlled single field emitter attracts great interested. However, in our fabrication process, the emission sharpness is a strong function of array density due to the etching process. The single emitter was more blunt than the emitters in the 10x10 or 20x20 FEAs due to over-etched and over-oxidized. The first suggestion for future work is to use the same mask-set, optimize the etching process, and make several perfect single emitters. Repeat the work done in this thesis and provide a better study on the single emitter.

The second recommendation is to assemble a vacuum chamber with more electrical probing arms by modifying the current vacuum chamber. We have several designs on the mask layout such as 1x8, 1x4, 1x2, and 2x2 integrated LD-MOSFET/FEA sets that could not be tested due to the limitation of the probe numbers. The study could be more completed with these results.

Another extension of this work is to further study the short term/long term noise of the gas effect on the silicon emitters. Emission is a very sensitive process due to surface properties, and our current study could not provide a conclusive result for the short-term emission current fluctuation in different gases.

Regarding the process, more precise control of CMP is needed. The CMP is the most difficult part of the fabrication process in this work. In order to increase the yield and improve the uniformity, CMP should definitely be optimized. Better characterization equipment is needed to determine the end point of polishing. At present, it requires each wafer to be examined under SEM multiple times before it is done. In addition, the uniformity of the MOSFET devices and yield of the integrated devices should be improved by more precise processing control.

Appendix

A. Microsystems Technology Laboratories' Fabrication Facilities

The Integrated Circuits Laboratory (ICL): to be used for CMOS and CMOS-compatible processes. The ICL is a Class 10 lab.

The Technology Research Laboratory (TRL): to be used for CMOS-compatible and other semiconductor devices, including opto-electronics, and MEMS. The TRL is a Class 100 Lab.

The Exploratory Materials Laboratory (EML): to be used for basic thin film deposition and photolithography. Tools are available for use with a great variety of materials. The EML is a Class 1000 Lab [A.1].

B. Mask Sets for Silicon LD-MOSFET/FEA Devices

The original mask set consists of 7 levels. The masks are summarized in Table B-1.

Table B-1. Mask set description.

Mask #	Objective	Tone*	Minimum Feature Size**
1	Post doping	DF	5
2	Tip definition	CF	1
3 (the optional mask)	Oxide thinning	DF	160
4	Gate definition	CF	5
5	Contact via definition	DF	5
6	Metal pad definition	CF	5
7	Tip Exposure	DF	5

* Tone: Clear field (CF) or Dark field (DF)

** Unit: μm

After the preliminary experiment, several masks were revised and more masks were added to the mask set. The revised masks are summarized in Table B-2 and the complete mask layout is shown in Figure B-1.

Table B-2. Revised mask set description.

Mask #	Mask Name	Objective	Tone	Minimum Feature Size	Comment
1	Array Mask	Post doping	DF	5	unchanged
2	Dot Mask	Tip definition	CF	1.7	Revised to have larger PR disks
9	Isolation Mask	Isolation doping	CF	5	Added for boron implantation
3	MOSFET Channel Mask	Oxide thinning & threshold voltage adjustment	DF	5	Revised to open channel region only & added for boron implantation
4	MOSFET Gate Mask	Gate definition	CF	5	Unchanged
5	MOSFET Source Mask	MOSFET source definition	DF	5	Revised to un-reveal the FEA area & reduce the MOSFET width
8	Contact Mask	Contact hole definition	DF	5	Added because of passivation layer
6	Metal Mask	Metal pad definition	CF	5	unchanged
7	Tip Exposure Mask	Tip Exposure	DF	5	Fix the mask error

* Our design rule is 2-5 μm depends on the tolerance of the device.

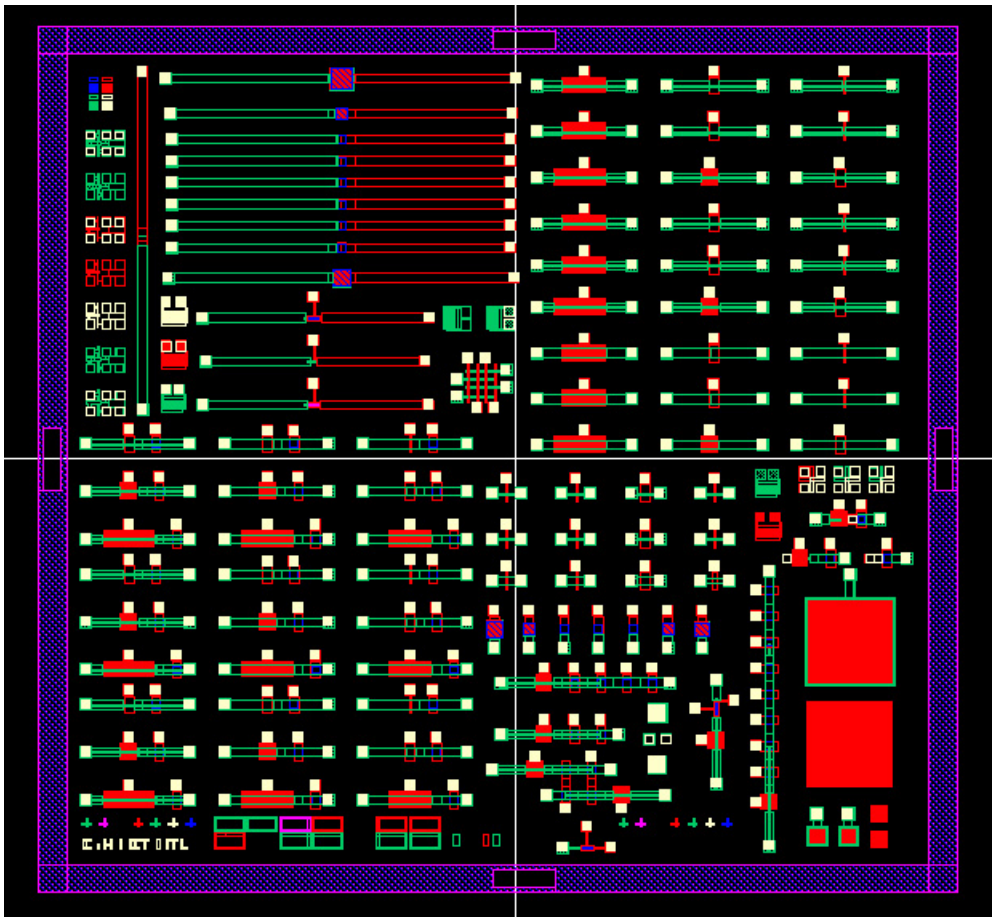


Figure B-1. The mask layout.

Several device structures were included in the layout: FEA, MOSFET, LD-MOSFET, and the integrated LD-MOSFET/FEA. Other device structures included are ridge-type emitters and the integrated LD-MOSFET/ridge emitters. The devices on the layout are summarized in Table B-3.

Table B-3. Device summary.

Device	parameter	description
FEA	1x1, 20x20, 30x30 and 60x60 3 and 4 μm separated between tips	7 sets of devices
MOSFET	* W = 5, 10, 100 μm x L = 5, 10, 100 μm and W = L = 1, 20, 50 μm	12 sets of devices
LD-MOSFET	W = 5, 10, 100 μm x L = 5, 10, 100 μm x L_{drift} = 10, 100 500 μm	27 combination devices
LD-MOSFET/FEA	1x1, 10x10 and 20x20 arrays, 4μm separation and W/L = 0.1, 1 and 10, L_{drift} = 10, 100 500 μm	27 combination devices
FEA set	4 polysilicon line x 4 n+ line FEA device with single tip	single tip at the intersection of polysilicon line and n+ line
Field emitter ridge	20, 100 μm and 5x20 μm with 3 μm separation and W = 10, L = 100 and L_{drift} = 100 μm	extracted gate and focus gate are in the devices
LD-MOSFET/Ridge	5x20 μm with 3 μm separation W = 10, L = 100 and L_{drift} = 100 μm	

*W is width, L is length and L_{drift} is the drift length of the transistor.

C. Process Flow of the Fabrication of Silicon FEA/MOSFET Devices

LOT name: FEAFET1

Start with 20, p-type (100) 4 in Si wafer, resistivity = 10-20 ohm-cm

The process is not gold contaminated. Almost all processing was done in ICL.

1. Post Doping

#	Step	Cafe Name	Parameters	Notes
1.01	Wafer Clean	RCA	5:1:1 H_2O: H_2O_2: NH_4OH(10m) 80°C 50:1 H_2O:HF (15 s) 6:1:1 H_2O: H_2O_2: HCl (15m) 80°C	ICL
1.02	Oxide Growth	tubeA3	500 Å, 950 °C, wet oxide	ICL recipe#123
1.03	Measurement	UV1280	SiO_2 thickness	ICL
1.04	HMDS Prime	HMDS	125 °C, 25 m	ICL
1.05	PR Coat/Pre-bake	coater6	KTI pos. PR 820 35cs, 5500 rpm, 1150nm Pre-bake: 115°C, 60 s	ICL
1.06	Exposure	stepper2	Mask#1 DF only on dies (6,1) and (6,8)	ICL
1.07	PR Develop	developer	Post exposure-bake: 115°C, 60 s Develop: OCG 934 1:1 pos. PR developer Post bake: 130 °C, 60 s	ICL
1.08	Oxide Etch	oxide	7:1 BOE	ICL
1.09	Silicon Etch	AME5000	Cl_2 20 sccm, HBr 20 sccm, NF_3 10sccm, 200mT for 5000A (Undoped-polysilicon)	ICL

1.10	Resist Strip	asher		ICL
1.11	Measurement	UV1280	PR thickness	ICL
1.12	Wafer Clean	pre-metal	1:3 H_2O_2:H_2SO_4 (10 m) 50:1 H_2O:HF (15 s)	ICL (can skip if no PR left after 1.11)
1.13	HMDS Prime	HMDS	125 °C, 25 m	ICL
1.14	PR Coat/Pre-bake	coater6	KTI pos. PR 820 35cs, 5500 rpm, 1150 nm Pre-bake: 115°C, 60 s	ICL
1.15	Exposure	stepper2	Mask#1 DF	ICL
1.16	PR Develop	developer	Post exposure-bake: 115°C, 60 s Develop: OCG 934 1:1 pos. PR developer Post bake: 130 °C, 60 s	ICL
1.17	Implant	Implanter	P, 180 KeV, (i)2 x 10^{12} cm^{-2}, (ii)5 x 10^{12} cm^{-2}	Send out
1.18	Resist Strip	asher		ICL
1.19	Wafer Clean	pre-metal	Rinse in piranha-strip dump rinser first Piranha in piranha-strip tank (10 m) Piranha in piranha-clean tank (10 m) HF dip in HF tank (30 s)	ICL
1.20	Wafer Clean	RCA	5:1:1 H_2O: H_2O_2: NH_4OH (10m) 80°C 50:1 H_2O:HF (15 s) 6:1:1 H_2O: H_2O_2: HCl (15m) 80°C	ICL
1.21	Implant Drive-In + Oxide Growth	tubeA2 tubeA3	1000°C wet oxide, 25 min 1150°C N_2,, 130 min	ICL recipe #122 and #345

1.22	Measurement	UV1280	SiO_2 thickness	ICL
1.23	Measurement	SIMS	Thickness of doped Si	Sent out (monitor)
1.24	Measurement	four point probe	Resistivity of doped Si	ICL (monitor)

2. Tip Definition

#	**Step**	**Cafe Name**	**Parameters**	**Notes**
2.01	HMDS Prime	HMDS	125 °C, 25 m	ICL
2.02	PR Coat/Pre-bake	coater6	KTI pos. PR 820 35cs, 8500 rpm, 920 nm Pre-bake: 115°C, 60 s	ICL
2.03	Exposure	stepper2	Mask#2LF	ICL
2.04	PR Develop	developer	Post exposure-bake: 115°C, 60 s Develop: OCG 934 1:1 pos. PR developer Post bake: 130 °C, 60 s	ICL
2.05	Measurement	SEM	Diameter of PR dot	DMSE (monitor)
2.06	Oxide Etch	AME5000	CF_4 15 sccm/CHF_3 10sccm, 12 mT, 250W (FEA OX)	ICL anisotropic
2.07	Measurement	UV1280	SiO_2 thickness	ICL (make sure oxide is clean)
2.08	Resist Strip	asher		ICL
2.09	Wafer Clean	pre-metal	1:3 H_2O_2:H_2SO_4 (10 m) 50:1 H_2O:HF (15 s)	ICL
2.10	Measurement	SEM	Diameter of oxide dot	DMSE (monitor)
2.11	Si Etch	AME5000	SF_6 75 sccm, 175 mT, 100 W	ICL isotropic

			& Cl_2 56sccm/HBr 7 sccm, 30mT, 300W (DING SI ETCH & Z PRH ANISO SI)	& anisotropic
2.12	Observation	SEM	Structure of tip neck region	DMSE (monitor)
2.13	Cap Strip	Oxide	7:1 BOE, 1 m	ICL
2.14	Wafer Clean	pre-metal	1:3 H_2O_2:H_2SO_4 (10 m) 50:1 H_2O:HF (15 s)	ICL
2.15	Wafer Clean	RCA	5:1:1 H_2O: H_2O_2: NH_4OH (10m) 80°C 50:1 H_2O:HF (15 s) 6:1:1 H_2O: H_2O_2: HCl (15m) 80°C	ICL
2.16	Sharpening Oxidation	tubeA3	950 °C, 15 h, 100 % dry O_2	ICL Recipe #160
2.17	Observation	SEM	Structure	DMSE (monitor)

3. Boron Implantation

#	**Step**	**Cafe Name**	**Parameters**	**Notes**
3.01	HMDS Prime	HMDS	125 °C, 25 m	ICL
3.02	PR Coat/Pre-bake	coater6	KTI pos. PR 820 35cs, 8500 rpm, 920nm Pre-bake: 115°C, 60 s	ICL
3.03	Exposure	stepper2	Mask#9LF	ICL
3.04	PR Develop	developer	Post exposure-bake: 115°C, 60 s Develop: OCG 934 1:1 pos. PR developer Post bake: 130 °C, 60 s	ICL
3.05	Implant	Implanter	B, 80 KeV, $3.5x10^{13}$ cm^{-2} 7 °tilt	Send out
3.06	Measurement	SIMS	Thickness of doped Si	Sent out

				(monitor)
3.07	Wafer Clean	pre-metal	Rinse in piranha-strip dump rinser first Piranha in piranha-strip tank (10 m) Piranha in piranha-clean tank (10 m) HF dip in HF tank (30 s)	ICL

4. Insulator and Gate Deposition

#	**Step**	**Cafe Name**	**Parameters**	**Notes**
4.01	Wafer Clean	RCA	5:1:1 H_2O: H_2O_2: NH_4OH (10m) 80°C 50:1 H_2O:HF (15 s) 6:1:1 H_2O: H_2O_2: HCl (15m) 80°C	ICL
4.02	LPCVD Oxide	tubeA7	400 °C, SiH_4 50 sccm, O_2 150 sccm, 350 mT, 700 nm	ICL Recipe:#462 (103A/min)
4.03	Measurement	UV1280	SiO_2 thickness	ICL (monitor)
4.04	LTO Densification	tubeA2	1000 °C, N_2, 2hr	ICL Same day as 3.02
4.05	HMDS Prime	HMDS	125 °C, 25 m	ICL
4.06	PR Coat/Pre-bake	coater6	KTI pos. PR820 35cs, 5500 rpm, 1150 nm Pre-bake: 115°C, 60 s	ICL
4.07	Exposure	stepper2	Mask#3DF	ICL
4.08	PR Develop	developer	Develop: OCG 934 1:1 pos. PR developer Post bake: 130 °C, 60 s	ICL
4.09	Oxide Etch	oxide	7:1 BOE	ICL

4.10	Resist Strip	asher		ICL
4.11	Wafer Clean	pre-metal	1:3 H_2O_2:H_2SO_4 (10 m) 50:1 H_2O:HF (15 s)	ICL
4.12	Wafer Clean	RCA	5:1:1 H_2O: H_2O_2: NH_4OH (10m) 80°C 50:1 H_2O:HF (15 s) 6:1:1 H_2O: H_2O_2: HCl (15m) 80°C	ICL
4.13	Oxide Growth	tubeA3	500 Å, 1000 °C, dry oxide	ICL #121
4.14	Measurement	UV1280	Oxide thickness	ICL (monitor)
4.15	Implant	Implanter	B, 10 KeV, $5x10^{12}$ cm^{-2} 7 °tilt	Send out
4.16	Wafer Clean	pre-metal	Rinse in piranha-strip dump rinser first Piranha in piranha-strip tank (10 m) Piranha in piranha-clean tank (10 m) HF dip in HF tank (30 s)	ICL
4.17	Wafer Clean	RCA	5:1:1 H_2O: H_2O_2: NH_4OH (10m) 80°C 50:1 H_2O:HF (15 s) 6:1:1 H_2O: H_2O_2: HCl (15m) 80°C	ICL
4.18	Implant Anneal	rta2	1000 °C, 20 sec	ICL
4.19	Measurement	SIMS	Thickness of doped Si	Sent out (monitor)
4.20	Oxide Etch	oxide	7:1 BOE (~500 Å)	ICL
4.21	Wafer Clean	RCA	5:1:1 H_2O: H_2O_2: NH_4OH (10m) 80°C 50:1 H_2O:HF (15 s) 6:1:1 H_2O: H_2O_2: HCl (15m) 80°C	ICL
4.22	Oxide Growth	tubeA3	500 Å, 1000 °C, dry oxide	ICL #121
4.23	Measurement	UV1280	Oxide thickness	ICL (monitor)

4.24	LPCVD Poly-Si	tubeA6	4000 Å 625 °C, SiH_4 150 sccm, 250 mT	ICL Recipe:#461 (65A/min) Same day as 3.13
4.25	Doping	tubeA4	$POCl_3$, 925°C, 1 hr 39min	ICL Recipe:#310
4.26	Doping Oxide Removal	oxide	7:1 BOE	ICL
4.27	Measurement	UV1280	Poly-Si thickness	ICL
4.28	Observation	SEM	Structure	DMSE (monitor)
4.29	Measurement	four point probe	Resistivity of doped Si	ICL (monitor)

5. Gate Aperture Definition

#	**Step**	**Cafe Name**	**Parameters**	**Notes**
5.01	CMP of Poly CMP of Oxide	CMP	Table speed 10 rpm, quill speed 5 rmp, down force 2.5 psi, slurry 150 ml/min, back pressure 1 psi polishing time 155 sec	ICL
5.02	CMP Clean			ICL
5.03	Wafer Clean	pre-metal	Rinse in piranha-strip dump rinser first Piranha in piranha-strip tank (10 m) Piranha in piranha-clean tank (10 m) HF dip in HF tank (30 s)	ICL
5.04	Observation	SEM	Structure	ICL
5.05	Measurement	UV1280	Poly-Si thickness	ICL

6. Gate Definition

#	Step	Cafe Name	Parameters	Notes
6.01	HMDS Prime	HMDS	125 °C, 25 m	ICL
6.02	PR Coat/Pre-bake	coater6	KTI pos. PR820 35cs, 5500 rpm, 1150 nm Pre-bake: 115°C, 60 s	ICL
6.03	Exposure	stepper2	Mask#4LF	ICL
6.04	PR Develop	developer	Post exposure-bake: 115°C, 60 s Develop: OCG 934 1:1 pos. PR developer Post bake: 130 °C, 60 s	ICL
6.05	Poly Etch	AME5000	Cl_2 56sccm/HBr 7 sccm, 30mT, 300W (Z PRH ANISO SI)	ICL etch rate ~ 95A/sec
6.06	Resist Strip	asher		ICL
6.07	Measurement	UV1280	Poly-Si thickness	ICL
6.08	Observation	SEM	Structure	ICL
6.09	HMDS Prime	HMDS	125 °C, 25 m	ICL
6.10	PR Coat	coater6	KTI pos. PR 820 35cs, 5500 rpm, 1150 nm	ICL
6.11	PR Bake	developer	Post bake: 130 °C, 60 s	ICL
6.12	Backside Poly-Si Strip	AME5000	CCl_4 / SF_6	ICL
6.13	Backside Oxide Strip	oxide	7:1 BOE	ICL
6.14	Resist Strip	asher		ICL
6.15	Wafer Clean	pre-metal	Piranha in piranha-strip tank (10 m) Piranha in piranha-clean tank (10 m)	ICL

			HF dip in HF tank (15 s)	

7. Source/Drain Contact Definition

#	Step	Café Name	Parameters	Notes
7.01	HMDS Prime	HMDS	125 °C, 25 m	ICL
7.02	PR Coat/Pre-bake	coater6	KTI pos. PR820 35cs, 5500 rpm, 1150 nm Pre-bake: 115°C, 60 s	ICL
7.03	Exposure	stepper2	Mask#5DF	ICL
7.04	PR Develop	developer	Develop: OCG 934 1:1 pos. PR developer Post bake: 130 °C, 60 s	ICL
7.05	Oxide Etch	oxide	7:1 BOE	ICL
7.06	Measurement	UV1280	Oxide thickness	ICL
7.07	Implant	Implanter	As 90 KeV 7 x 10^{15} cm^{-2} 7 °tilt	Send out
7.08	Resist Strip	asher		ICL
7.09	Wafer Clean	pre-metal	Rinse in piranha-strip dump rinser first Piranha in piranha-strip tank (10 m) Piranha in piranha-clean tank (10 m) HF dip in HF tank (30 s)	ICL
7.10	Wafer Clean	RCA	5:1:1 H_2O: H_2O_2: NH_4OH (10m) 80°C 50:1 H_2O:HF (15 s) 6:1:1 H_2O: H_2O_2: HCl (15m) 80°C	ICL
7.11	Implant Anneal	rta2	1000 °C, 20 sec	ICL
7.12	Measurement	SIMS	Thickness of doped Si	Sent out

				(monitor)
7.13	Measurement	four point probe	Resistivity of doped Si	ICL (monitor)

8. Oxide Passivation

#	**Step**	**Café Name**	**Parameters**	**Notes**
8.01	Wafer Clean	RCA	5:1:1 H_2O: H_2O_2: NH_4OH (10m) 80°C 50:1 H_2O:HF (15 s) 6:1:1 H_2O: H_2O_2: HCl (15m) 80°C	ICL
8.02	LPCVD Oxide	tubeA7	400 °C, SiH_4 50 sccm, O_2 150 sccm, 350 mT, 300 nm	ICL Recipe:#462 (103A/min)

9. Contact Via Definition

#	**Step**	**Cafe Name**	**Parameters**	**Notes**
9.01	HMDS Prime	HMDS	125 °C, 25 m	ICL
9.02	PR Coat/Pre-bake	coater6	KTI pos. PR820 35cs, 5500 rpm, 1150 nm Pre-bake: 115°C, 60 s	ICL
9.03	Exposure	stepper2	Mask#8DF	ICL
9.04	PR Develop	developer	Develop: OCG 934 1:1 pos. PR developer Post bake: 130 °C, 60 s	ICL
9.05	Oxide Etch	oxide	7:1 BOE	ICL
9.06	Observation	SEM	Structure	ICL

9.07	Measurement	UV1280	Oxide thickness	ICL
9.08	Resist Strip	asher		ICL
9.09	Wafer Clean	pre-metal	Piranha in piranha-strip tank (10 m) Piranha in piranha-clean tank (10 m) HF dip in HF tank (15 s)	ICL
9.10	Metal Deposition	Endura	1.25 μm Al/ 50 nm TiN/10 nm Ti	ICL
9.11	HMDS Prime	HMDS	125 °C, 25 m	ICL
9.12	PR Coat/Pre-bake	coater6	KTI pos. PR820 35cs, 5500 rpm, 1150 nm Pre-bake: 115°C, 60 s	ICL
9.13	Exposure	stepper2	Mask#6LF	ICL
9.14	PR Develop	developer	Develop: OCG 934 1:1 pos. PR developer Post bake: 130 °C, 60 s	ICL
9.15	Metal Etch	rainbow	BCl_3 (90 sccm)/Cl_2(130 sccm)/Ar (40sccm) at 20 mT and 350 W	ICL
9.16	Water Rinse	acid hood	Dump rinse	TRL
9.17	Resist Strip	asher		ICL
9.18	Sinter	tubeA3	400°C, 30 mins	TRL

10. Tip Exposure

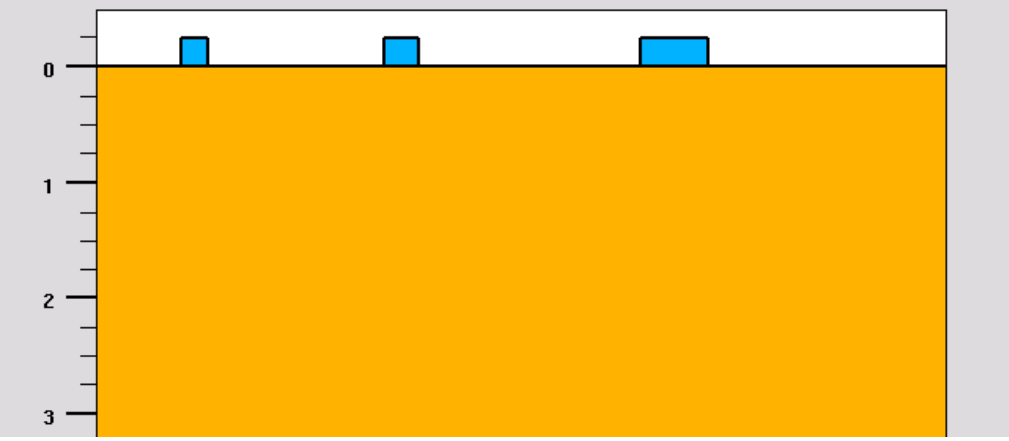
#	**Step**	**Cafe Name**	**Parameters**	**Notes**
10.1	HMDS Prime	HMDS	125 °C, 25 m	ICL
10.2	PR Coat/Pre-bake	coater6	KTI pos. PR820 35cs, 5500 rpm, 1150 nm Pre-bake: 115°C, 60 s	ICL

10.3	Exposure	stepper2	Mask#7DF	ICL
10.4	PR Develop	developer	Develop: OCG 934 1:1 pos. PR developer Post bake: 130 °C, 60 s	ICL
10.5	Oxide Etch	oxide	7:1 BOE	TRL
10.6	Resist Strip	coater6	Acetone, isopropanol, and methanol	ICL
10.7	Oxide Etch	acid hood	100:1 H_2O:HF (30 s)	EML
10.8	Observation	SEM	Structure	DMSE (monitor)

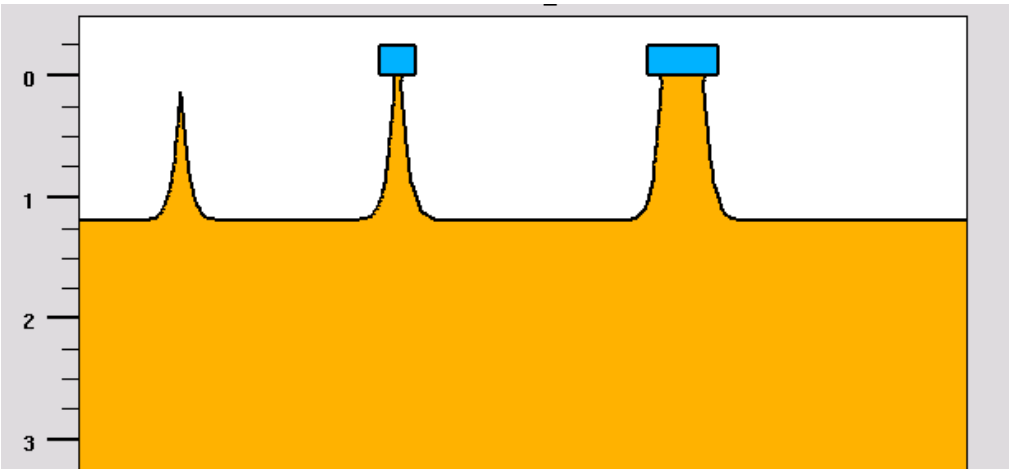
D. *Silvaco* Simulation Results for Three-Dimensional Oxidation

The oxidation sharpening process was simulated as shown in Figure D-1 (a) (b) and (c). The process simulation was done for dry oxidation at different temperatures and time duration. Figure D-1 (c) shows the oxidation at 950 ^{o}C for 15 hours. Oxidation simulation was done with viscous model. The tip heights of the 3rd small emitter, which had the original oxide disk of 1 μm, and the oxide thickness at the flat region for dry oxidation at different temperatures and time duration were summarized in Figure D-2 (a) and (b), and Table D-1, D-2, respectively. The tip radius could not be obtained in the simulation. However, whether the 3rd small emitter can be sharpened or not at different temperatures and time duration were concluded in Table D-3. The 3rd small emitter was picked in these simulations is because this is the feature size of the emitters in our device design.

(a)



(b)



(c)

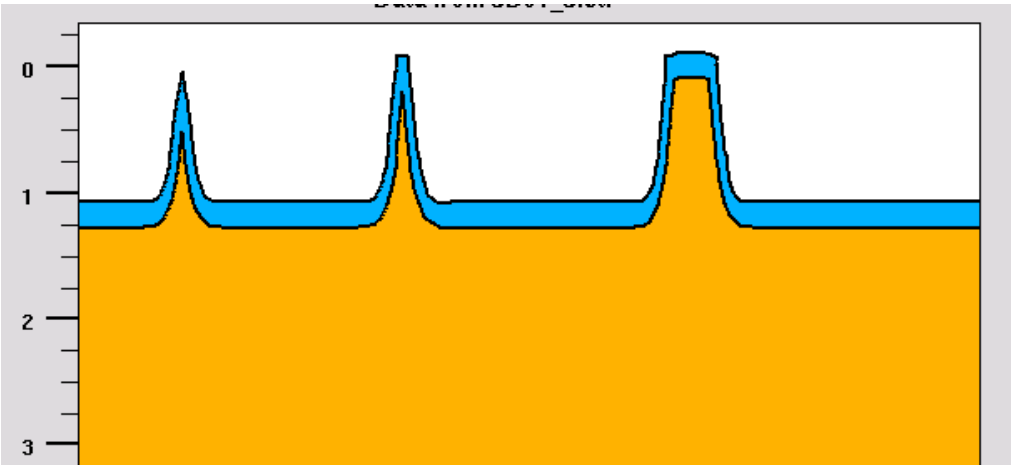
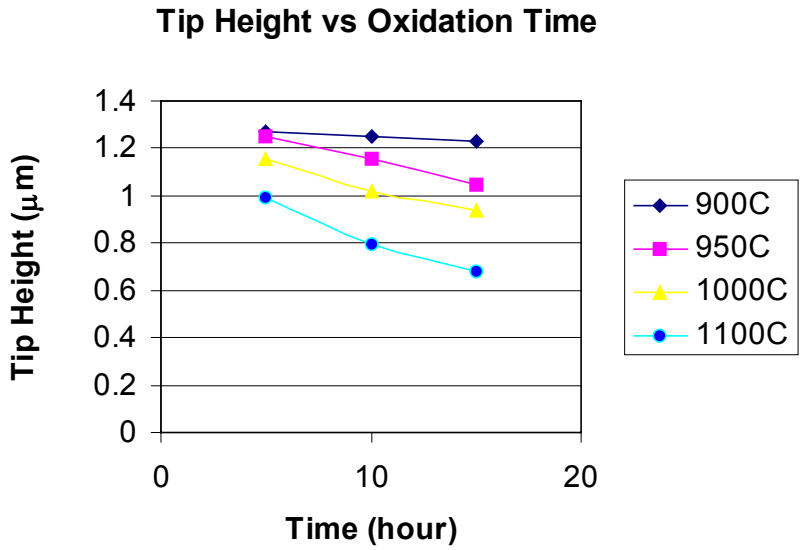


Figure D-1. Process simulation for (a) oxide disks definition, (b) silicon isotropic etch, and (c) oxidation sharpening in 950 ^{o}C and 15 hours.

(a)



(b)

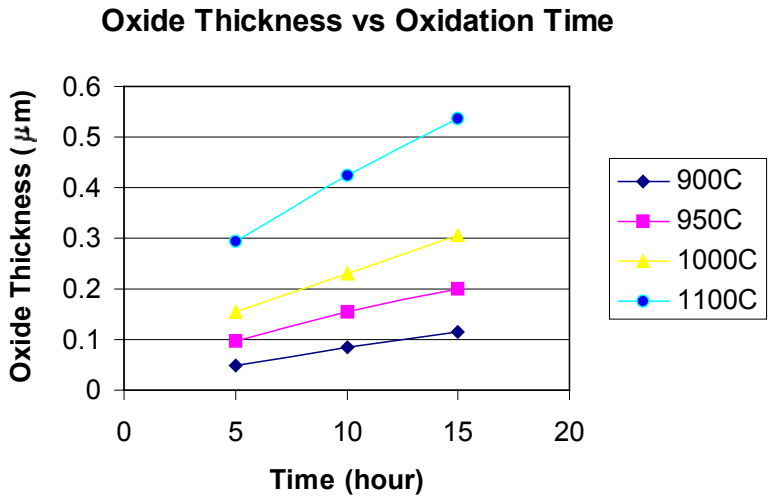


Figure D-2. (a) Simulated tip height of the 3rd small emitter, and (b) simulated oxide thickness at the flat region at different temperatures and time durations.

Table D-1. Simulated tip height of the 3rd small emitter.

	900 °C	950 °C	1000 °C
5 hr		1.25 μm	
10 hr	1.25 μm	1.154 μm	1.019 μm
15 hr		1.046 μm	

Table D-2. Simulated oxide thickness at the flat area.

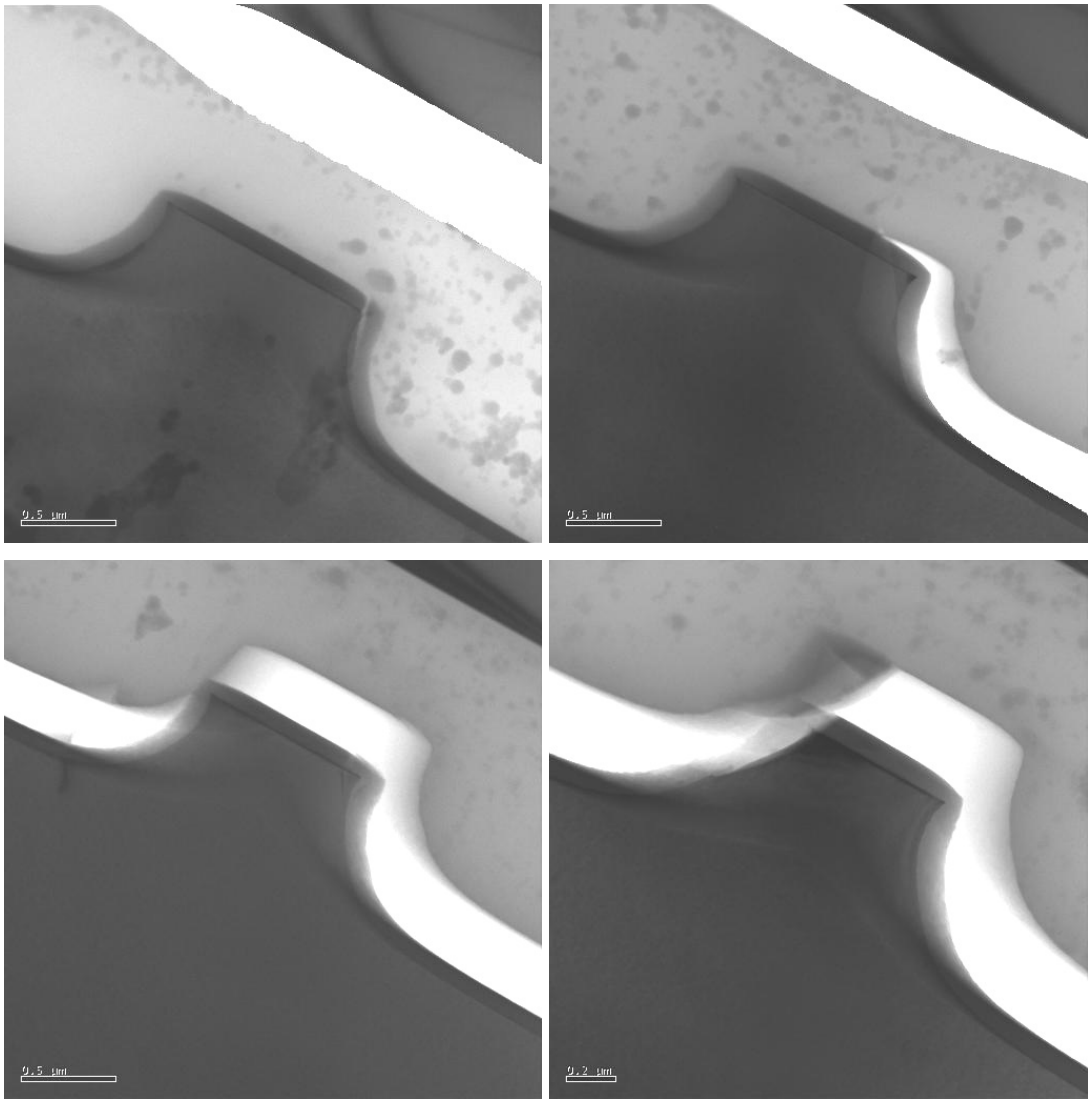
	900 °C	950 °C	1000 °C
5 hr		0.096 μm	
10 hr	0.085 μm	0.154 μm	0.231 μm
15 hr		0.2 μm	

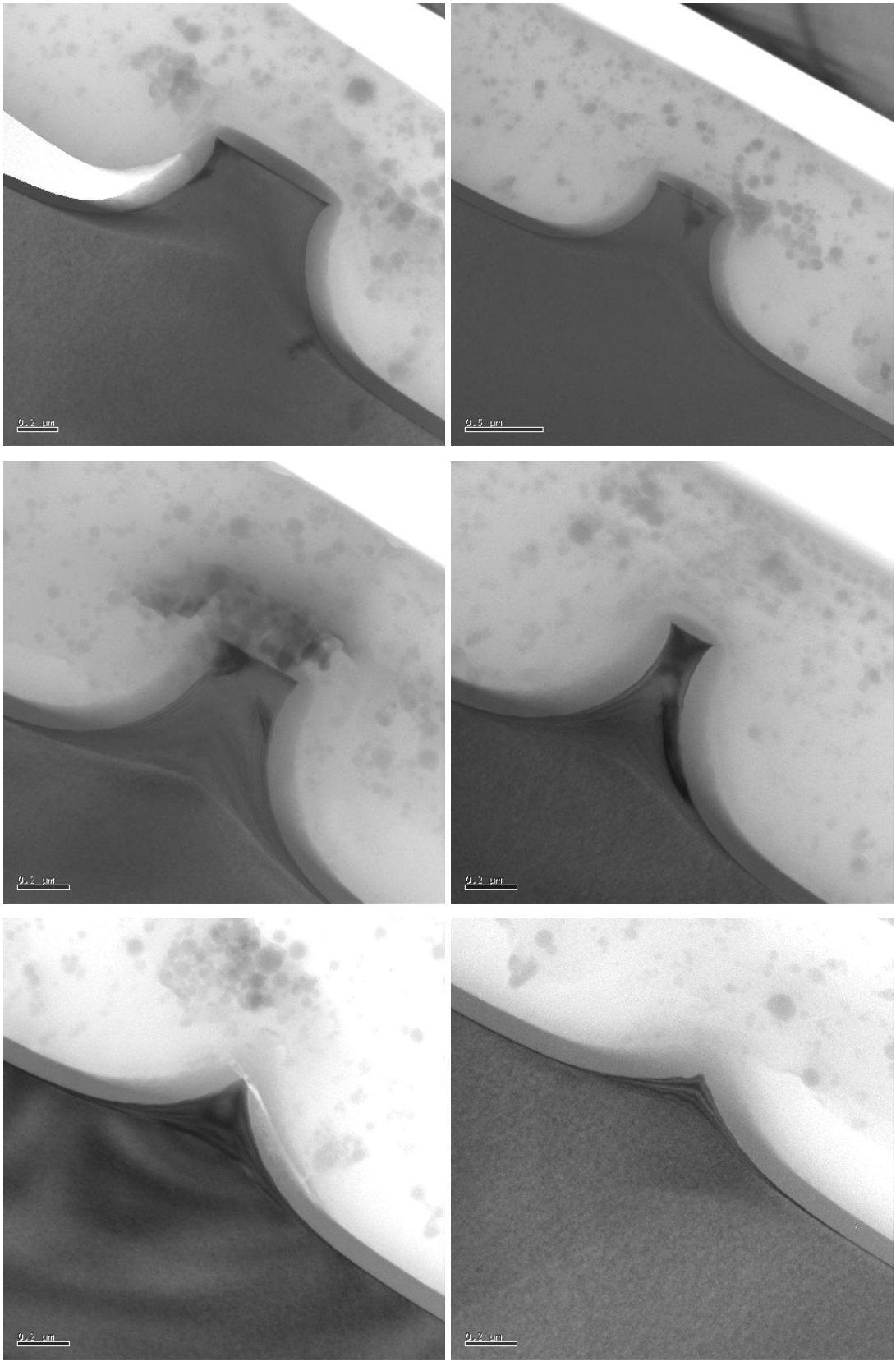
Table D-3. Matrix for oxidation temperature, time duration, and the emitter tip sharpness. ("x" represents that the tip is not sharpened yet and "o" represents the tip is sharpened in the 3rd small emitter)

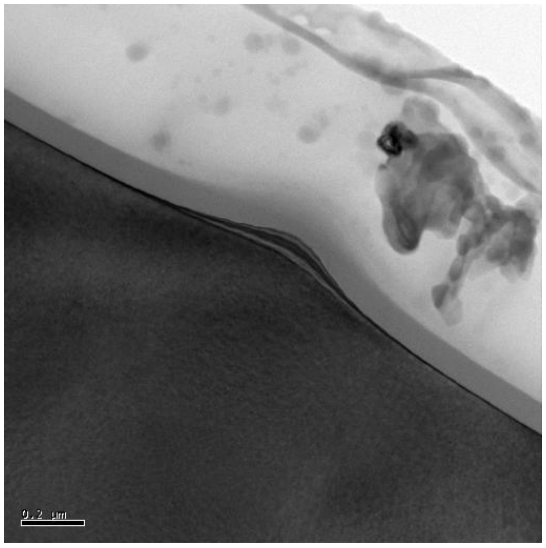
	900 °C	950 °C	1000 °C	1100 °C
5hr	x	x	o	o
10hr	x	o	o	o
12.5hr	x	o		
15hr	o	o	o	o

E. TEM Images of Oxidation Sharpening Experiments at Different Oxidation Temperatures and Time Duration

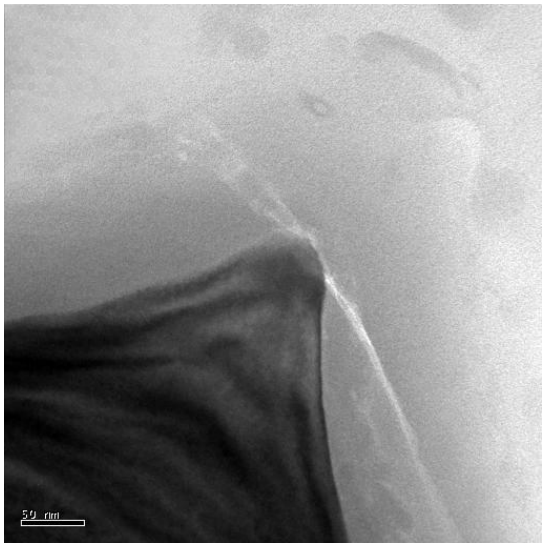
Oxidation at 900°C for 10 hours (The initial oxide cap sizes range from 1.8 μm to 0.8 μm in diameter)



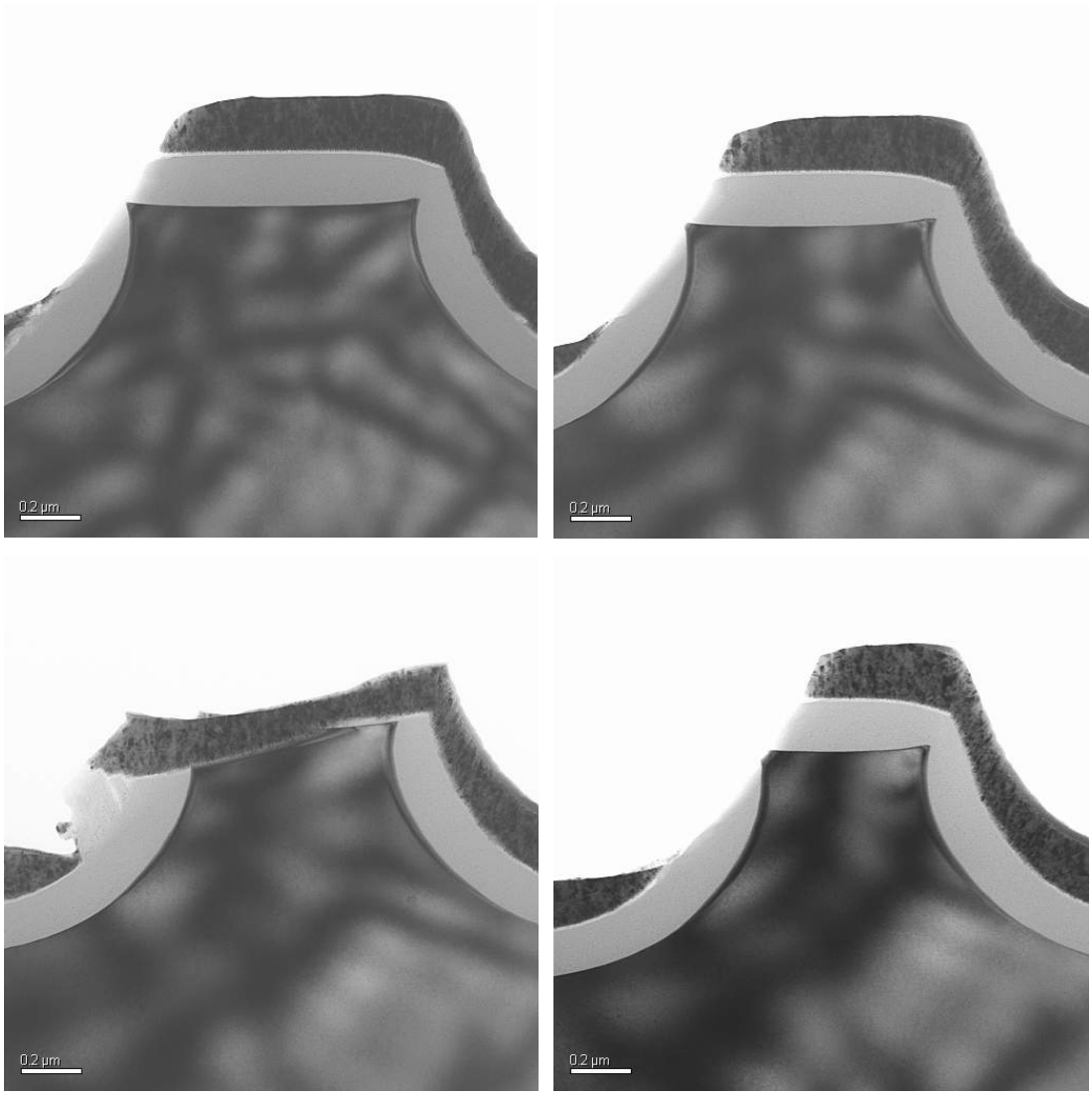


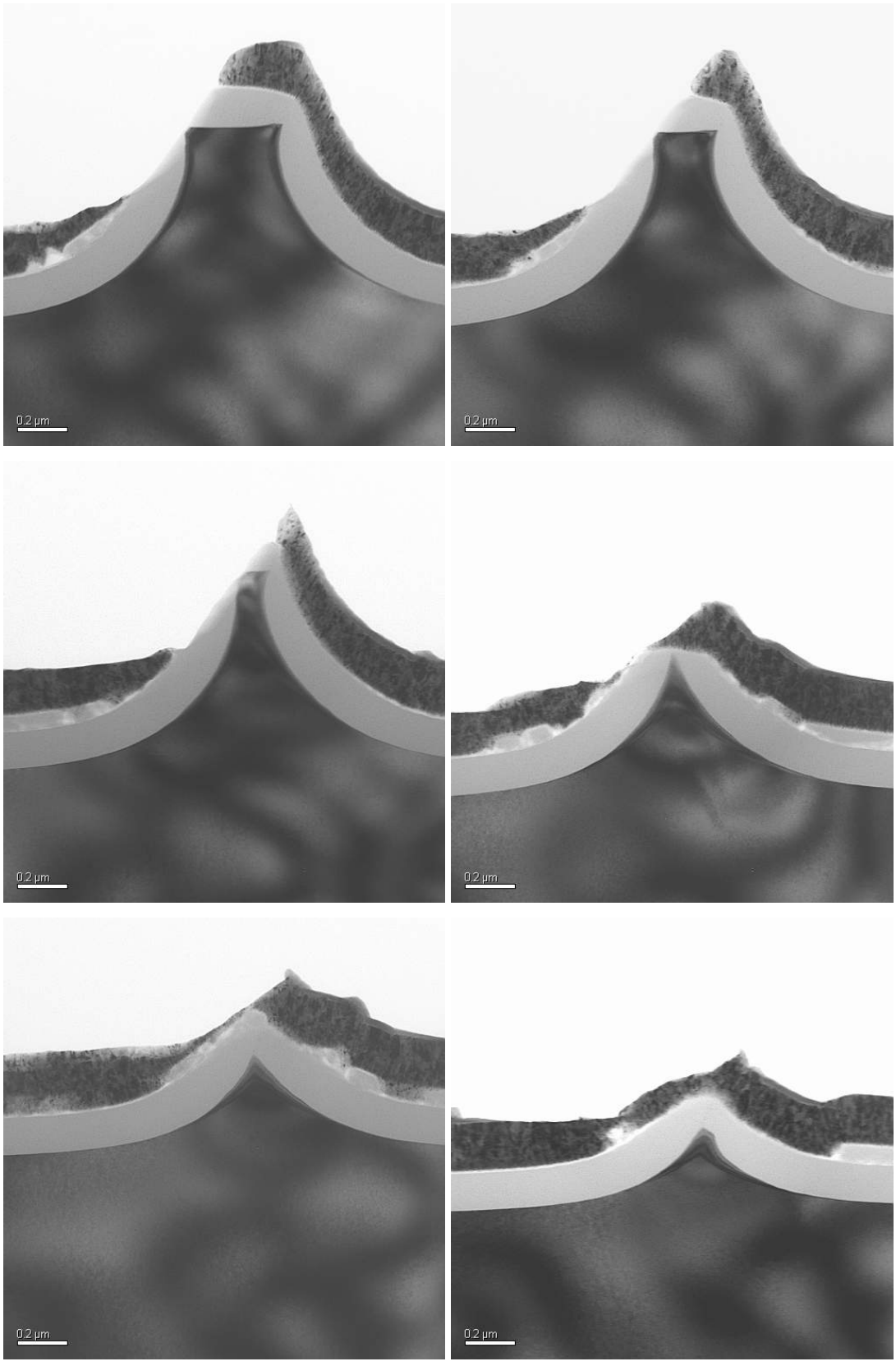


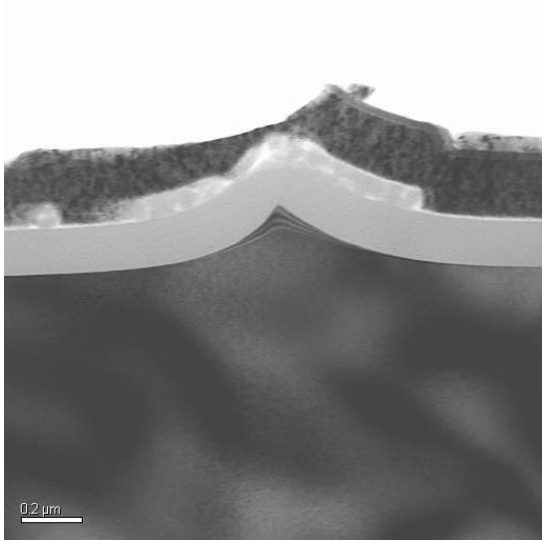
The higher resolution TEM of the tip region of the emitter with the initial oxide cap size of 1 μm.



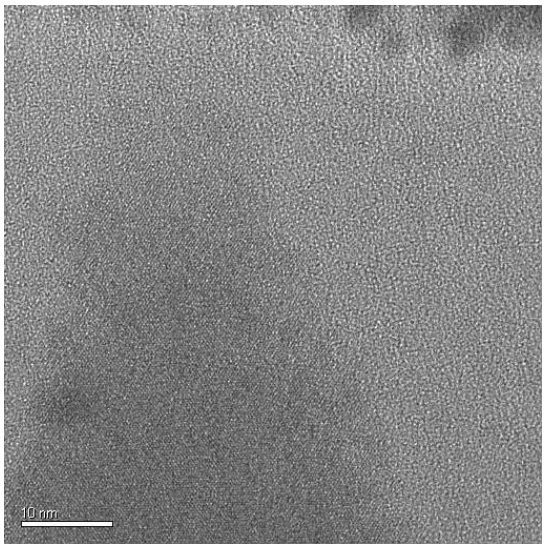
Oxidation at 950^{o}C for 10 hours (The initial oxide cap sizes range from 1.8 μm to 0.8 μm in diameter)

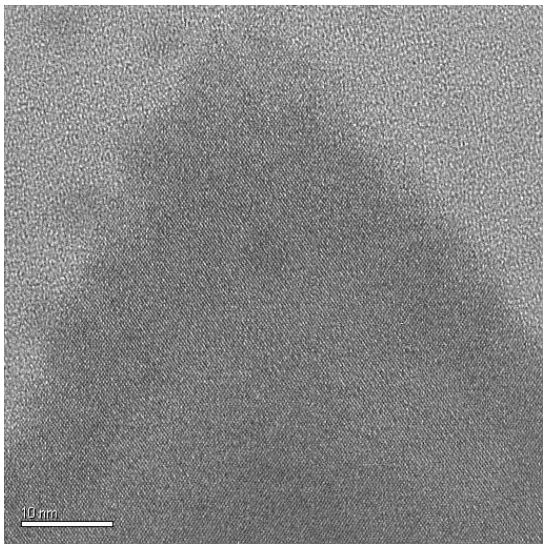



0.2 µm
0.2 µm
0.2 µm
0.2 µm
0.2 µm
0.2 µm

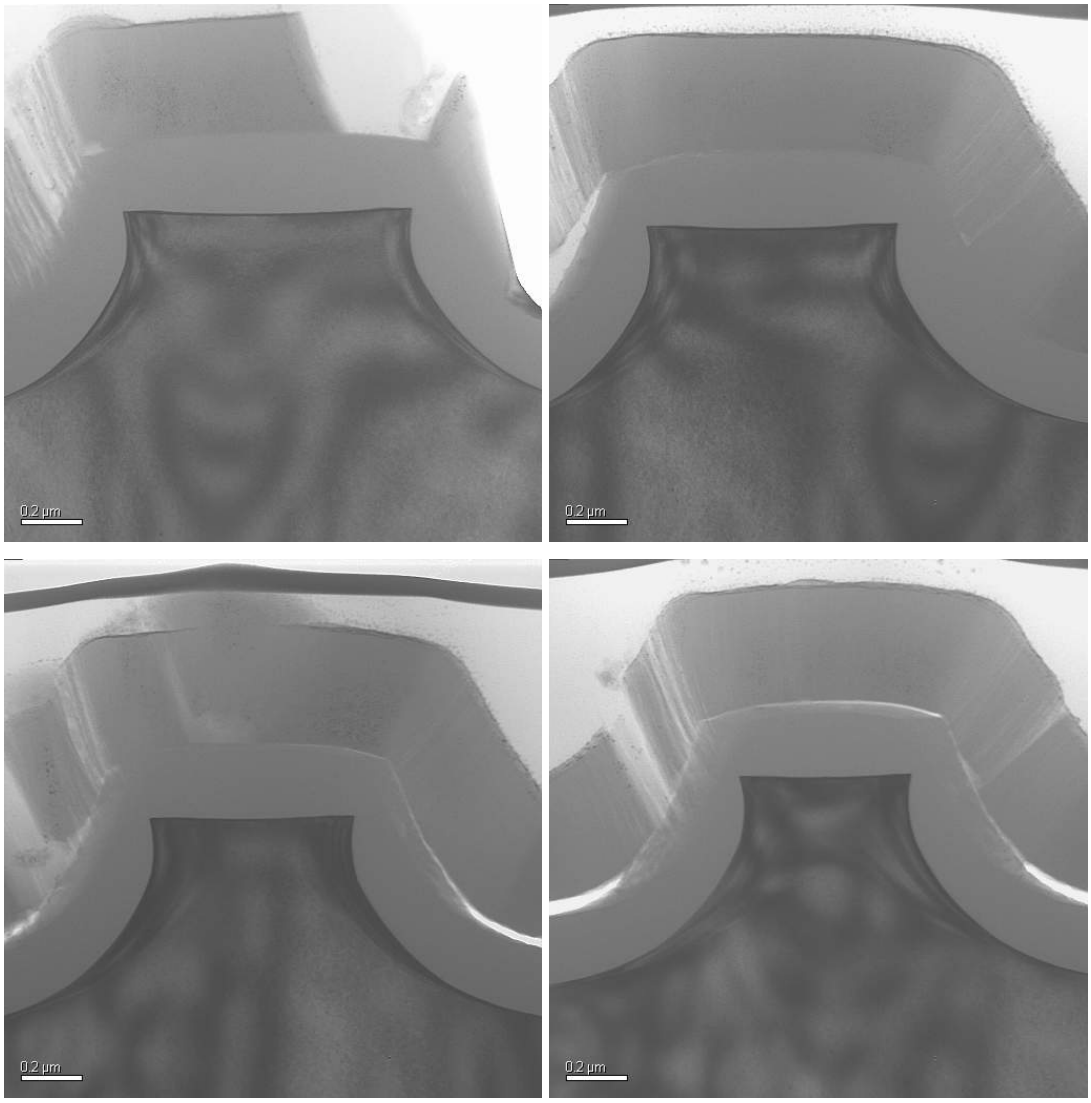


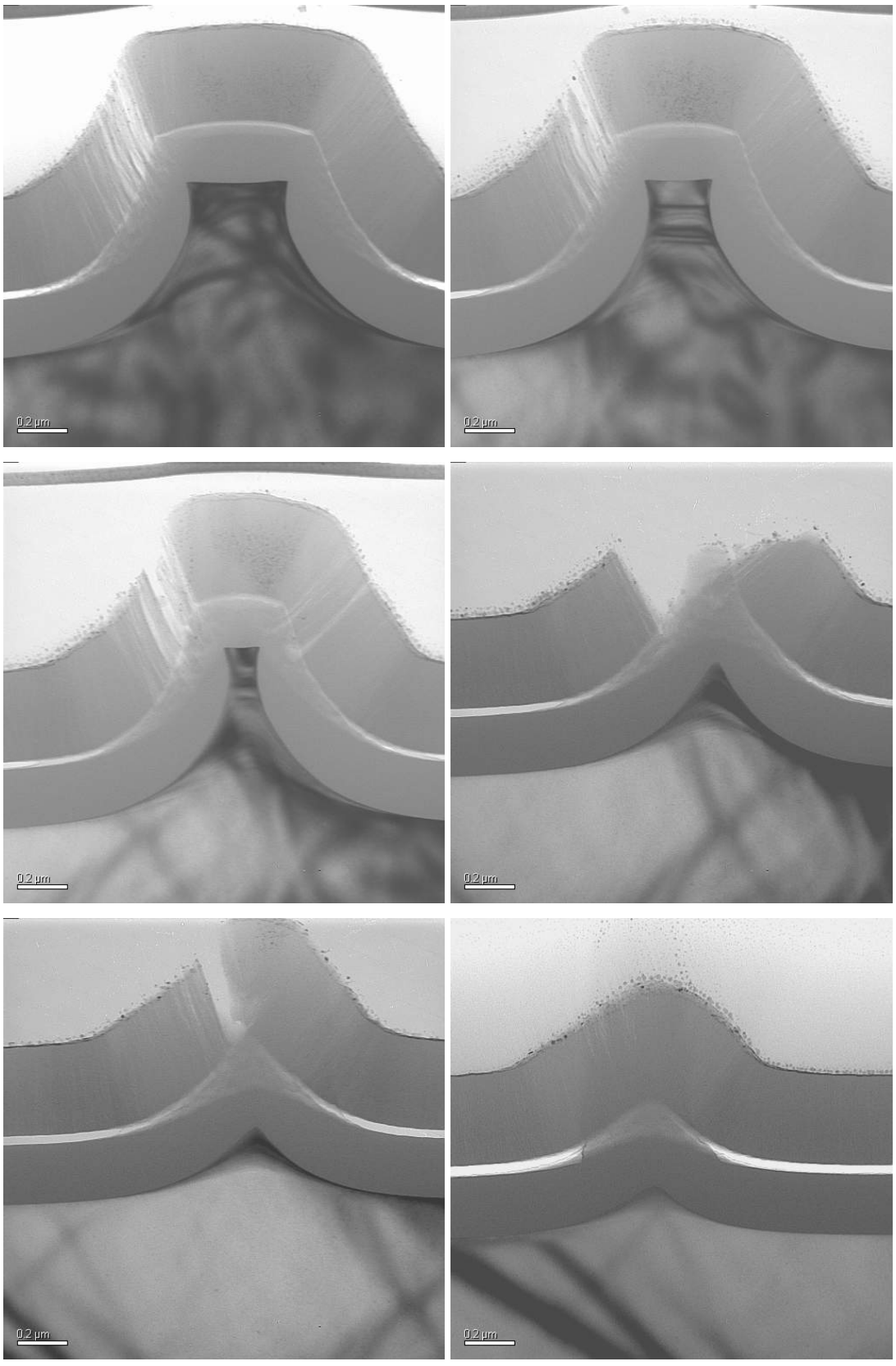
The high-resolution TEM images of the tip region of the emitters with the initial oxide cap size of 0.9 and 1 µm, respectively.

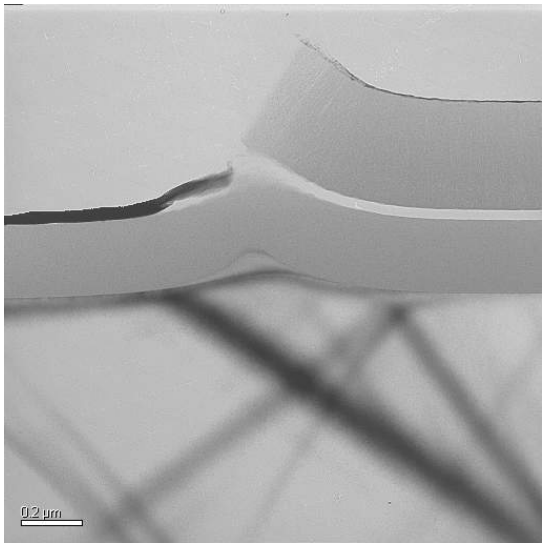




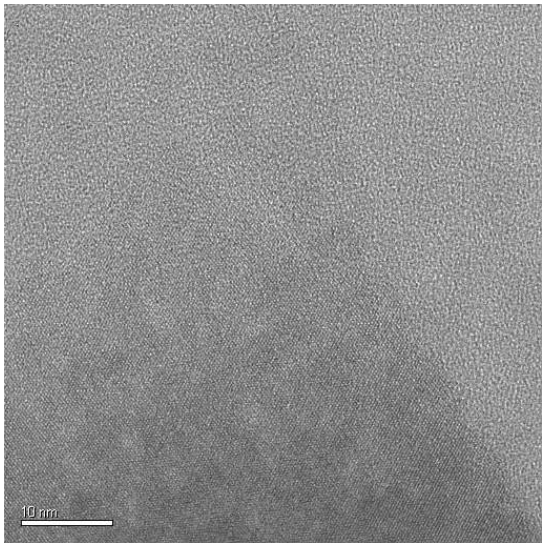
Oxidation at 1000°C for 10 hours (The initial oxide cap sizes range from 1.8 μm to 0.8 μm in diameter)

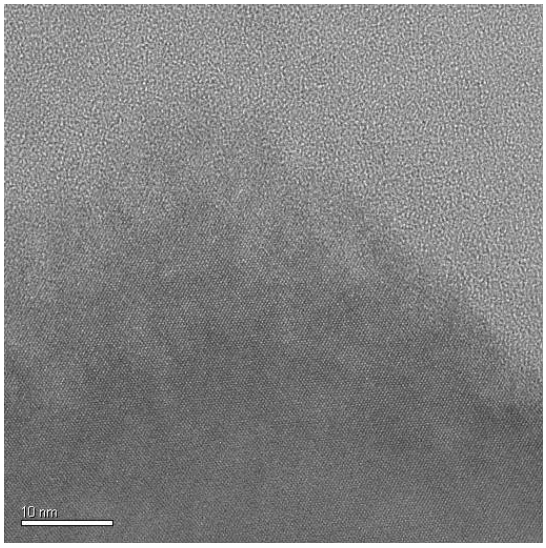



0.2 µm
0.2 µm
0.2 µm
0.2 µm
0.2 µm
0.2 µm

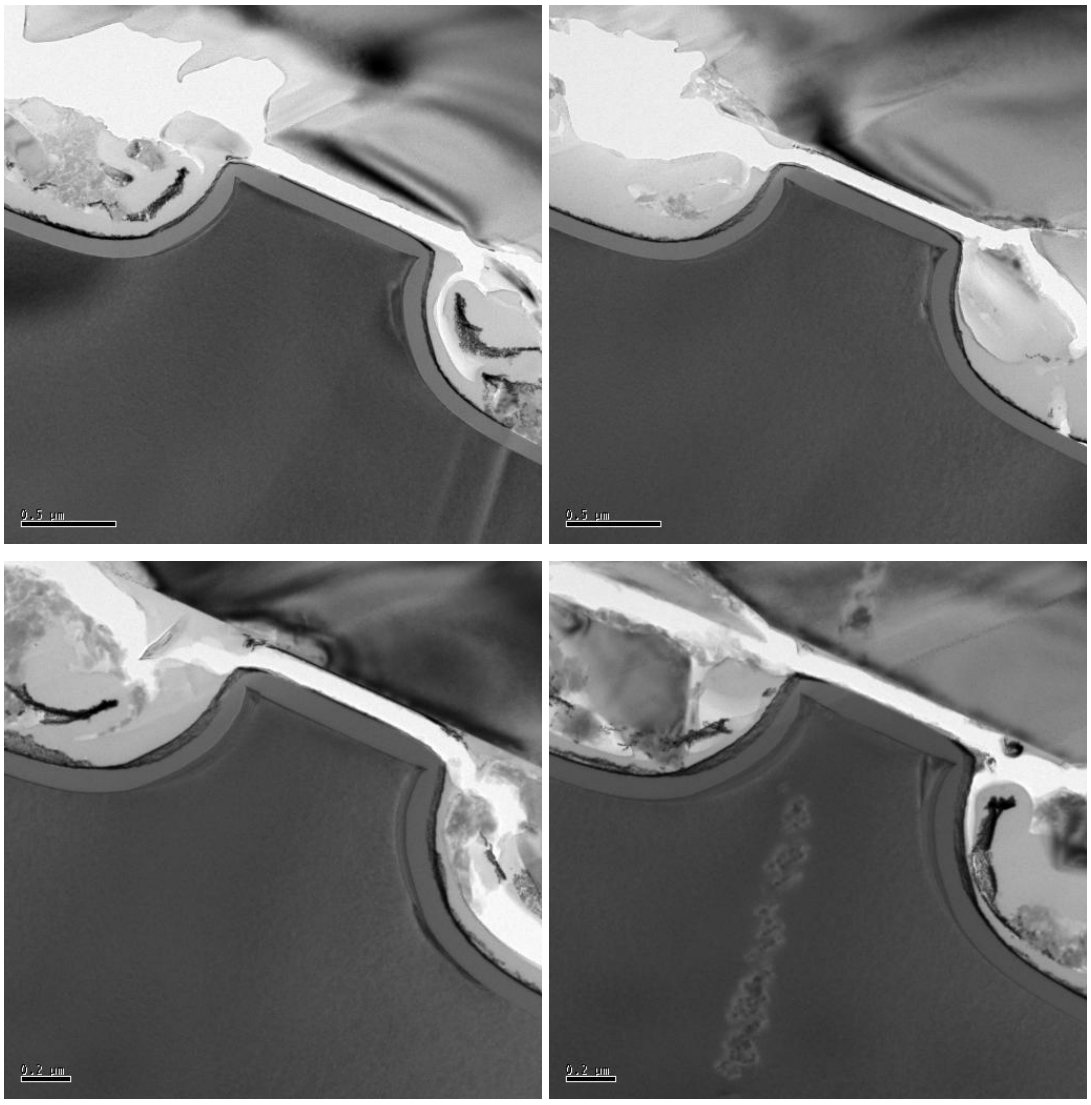


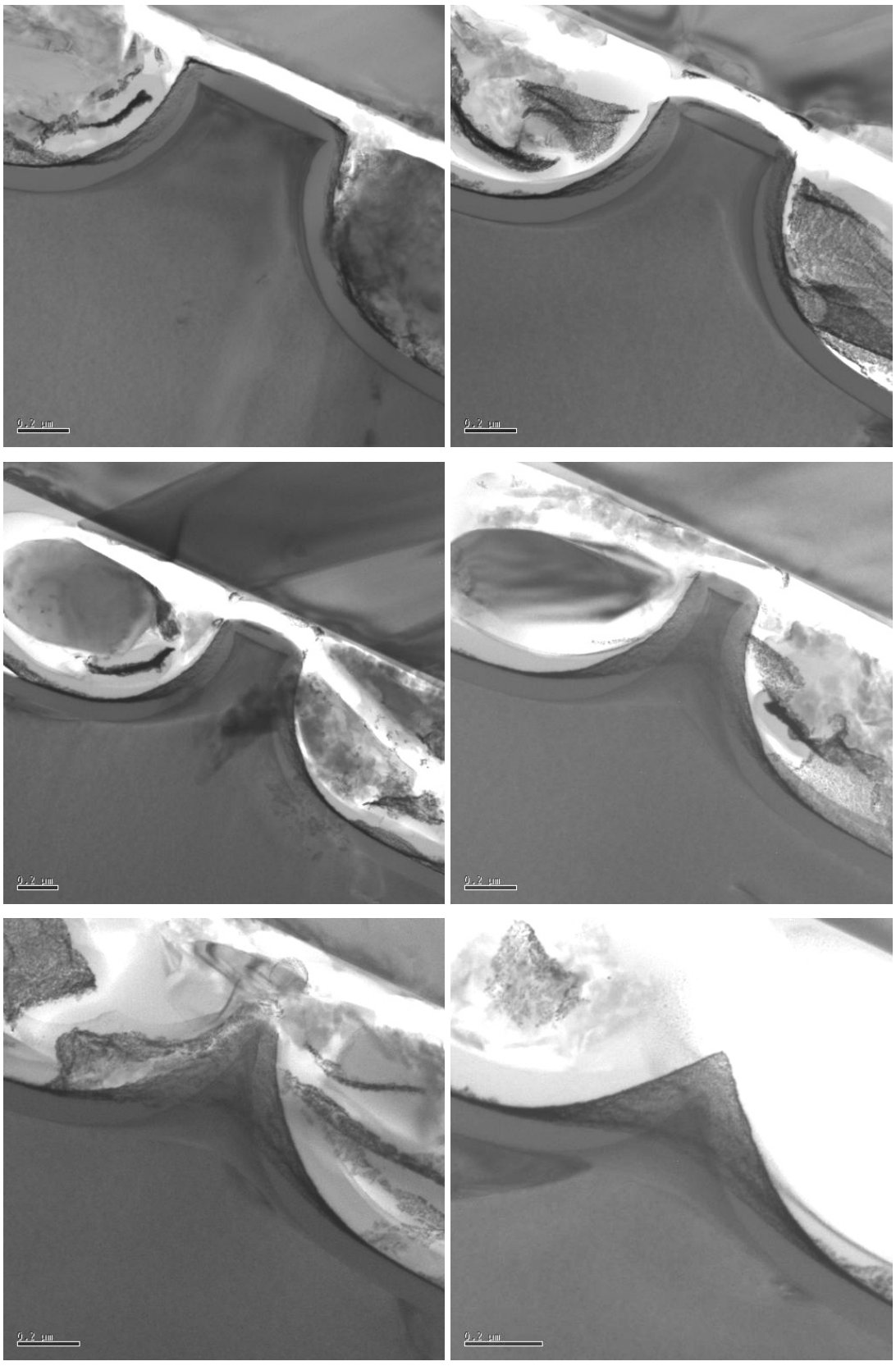
The high-resolution TEM images of the tip region of the emitters with the initial oxide cap size of 0.9 and 1 μm, respectively.





Oxidation at 950^{o}C for 5 hours (The initial oxide cap sizes range from 1.8 μm to 0.8 μm in diameter)




0.2 um
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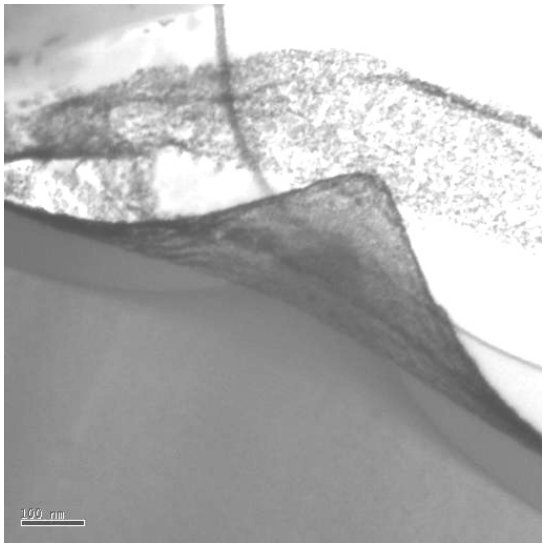

Table E-1. Oxide thickness at different positions and different oxidation conditions. The positions a-d are shown in Figure 3-15 (l).

900C 10 hours						
Oxide Cap Diameter (μm)	0.8	0.9	1	1.1	1.2	1.3
Thickness of a (nm)	80	80	80	80		80
Thickness of b (nm)				110	110	113.1
Thickness of c (nm)				21.05	50.55	51.3
Thickness of d (nm)				44.94	72.8	84.51
Tip height (nm)	140	270	400			
UV1280 (nm)	86	86	86	86	86	86
Tip radius (nm)			25.7			

Oxide Cap Diameter (μm)	1.4	1.5	1.6	1.7	1.8
Thickness of a (nm)	90	80	80	80	80
Thickness of b (nm)	105	110	103.73	113.4	116
Thickness of c (nm)	53	60.38	69.8	57	68
Thickness of d (nm)	87	90	90	90	90
Tip height (nm)					
UV1280 (nm)	86	86	86	86	86
Tip radius (nm)					

950C 10 hours						
Oxide Cap Diameter (μm)	0.8	0.9	1	1.1	1.2	1.3
Thickness of a (nm)	151	150.9	150	147.7	147.3	145.9
Thickness of b (nm)	170.3	174.2	173.7	173.75	167.73	166.44
Thickness of c (nm)					106.72	110.9
Thickness of d (nm)						
Tip height (nm)	217.5	330.12	386.2	582.8		
UV1280 (nm)	145	145	145	145	145	145
Tip radius (nm)	13.4	9.4	6.4	5.8		

Oxide Cap Diameter (μm)					
Thickness of a (nm)	1.4	1.5	1.6	1.7	1.8
Thickness of b (nm)					
Thickness of c (nm)	163.7	168.2	174.2		176
Thickness of d (nm)	112	117.3		118	123.6
Tip height (nm)	161.4	171		175.4	171.9
UV1280 (nm)					
Tip radius (nm)	145	145	145	145	145
1000C 10 hours					
Oxide Cap Diameter (μm)	0.8	0.9	1	1.1	1.2	1.3
Thickness of a (nm)	242.2	242.5	238.7	238.7	235	236
Thickness of b (nm)	249.5	254.28	265.5	250.9	242.2	252
Thickness of c (nm)					190.2	201
Thickness of d (nm)					200	217.5
Tip height (nm)	147.4	210.5	301.7	456.4		
UV1280 (nm)	234.4	234.4	234.4	234.4	234.4	234.4
Tip radius (nm)	35.8	31.6	10.5	6.1		
Oxide Cap Diameter (μm)	1.4	1.5	1.6	1.7	1.8	
Thickness of a (nm)	234					
Thickness of b (nm)	258	256	264.2	256	265.7	
Thickness of c (nm)	207	211	205.9/210.2	216.6/205.1	232.4	
Thickness of d (nm)	235	242.2	245.6	258.8	280.7	
Tip height (nm)						
UV1280 (nm)	234.4	234.4	234.4	234.4	234.4	

Tip radius (nm)						
950C 15 hours						
Oxide Cap Diameter (μm)	0.8	0.9	1	1.1	1.2	1.3
Thickness of a (nm)	210	210	200	200	190	190
Thickness of b (nm)	220	220	218	210	220	215
Thickness of c (nm)				100	130	140
Thickness of d (nm)	230	234		100	150	170
Tip height (nm)	260	350	480	620		
UV1280 (nm)	193	193	193	193	193	193
Tip radius (nm)	24.4	6	3			

Oxide Cap Diameter (μm)					
Thickness of a (nm)	1.4	1.5	1.6	1.7	1.8
Thickness of b (nm)	180				
Thickness of c (nm)	220	220	230	230	225
Thickness of d (nm)	150	150	160	160	160
Tip height (nm)	175	190	195	220	220
UV1280 (nm)					
Tip radius (nm)	193	193	193	193	193

950C 5 hours						
Oxide Cap Diameter (μm)	0.8	0.9	1	1.1	1.2	1.3
Thickness of a (nm)	90	90	90	90	90	90
Thickness of b (nm)	110	120	110	100	110	110
Thickness of c (nm)				50	60	70
Thickness of d (nm)	110	110		70	90	100
Tip height (nm)	280	380	580			
UV1280 (nm)	90	90	90	90	90	90
Tip radius (nm)	24.4	11	6.3			

Oxide Cap Diameter (μm)					
Thickness of a (nm)	1.4	1.5	1.6	1.7	1.8
Thickness of b (nm)	90	90	90	90	90
Thickness of c (nm)	110	110	110		120
Thickness of d (nm)	70	80	70	80	80

Tip height (nm)	100	100	110	100	100
UV1280 (nm)					
Tip radius (nm)	90	90	90	90	90

F. Field Emission Ridges

21 up-down I-V sweeps were performed in which the field emission ridge extraction gate voltage was swept up and down between 0 and 109 V as shown in Figure F-1. Similar to the I-V sweep done on FEAs, the first and last ten sweeps obtained current values at each voltage during the upward and downward ramps, and 20 current data points were averaged at each extraction gate voltage during the 11^{th} I-V sweep. It was also observed that the I-V curves from the up-sweep measurements are indistinguishable from the I-V curves from the down-sweep measurements as shown in Figure F-2. The horizontal dotted line in Figure F-2 shows that the voltage ranges over which a constant current of 70 nA could be obtained is ≈ 11 V. In other words, a gate-emitter voltage variation of ≈ 11 V is required in order to maintain a constant emission current of 70 nA. This also implies that a voltage controlled current source such as a MOSFET in saturation requires a saturation region of at least 11 V. The voltage spread is larger than that of a 10x10 FEA. It is believed that the total emitting sites are less in this field emission ridge than the regular field emission arrays. The gas absorption/desorption effect could not be averaged out in this field emission ridge.

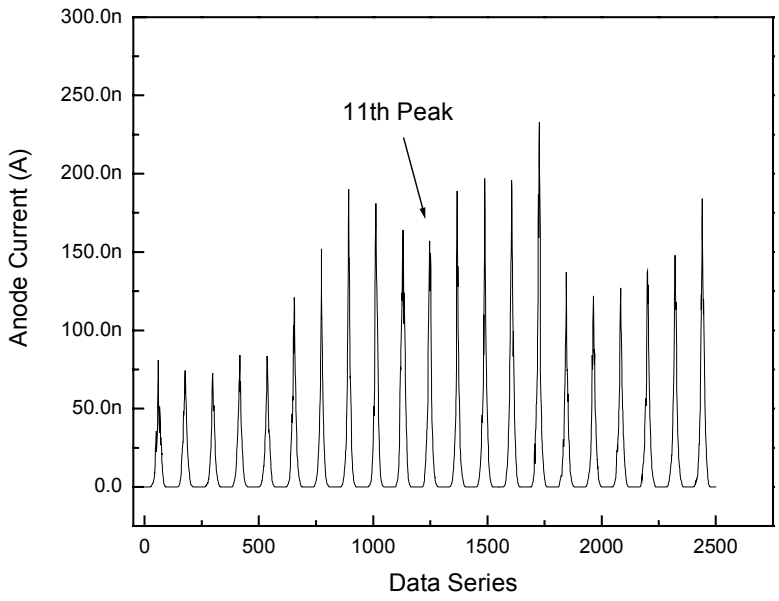

Figure F-1. The IV sweeps of the field emission ridge array.

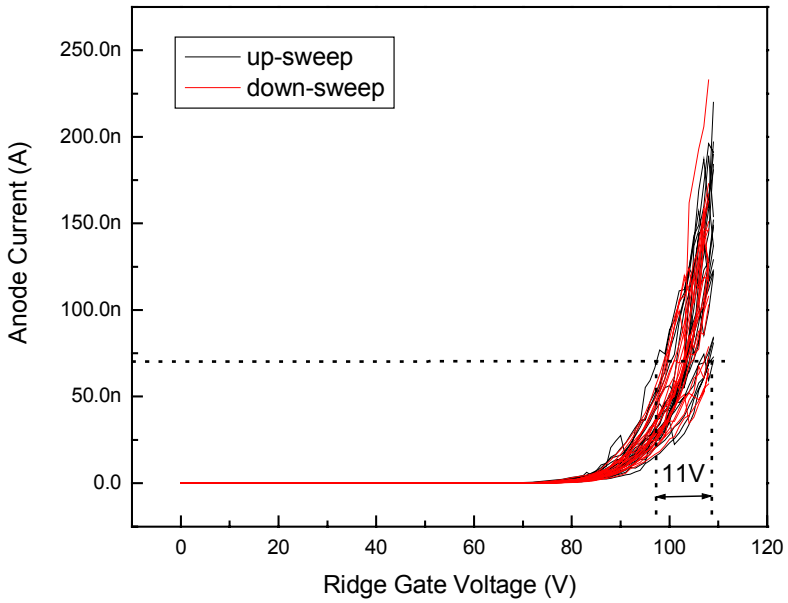

Figure F-2. Up-sweep and down-sweep anode current as a function of the applied ridge gate voltage.

We also analyzed the current-voltage data obtained during the 11th I-V sweep in Figure F-1. Figure F-3 shows that the turn-on voltage for this field emission ridge is 70 V, which is much higher than the FEAs. The slope of the F-N plot, Figure F-4, is 1289, also much higher than the one in field emitter tips. The theoretical value of β is 1/[r x ln(d/r)], instead of 1/r [F.1, F.2].

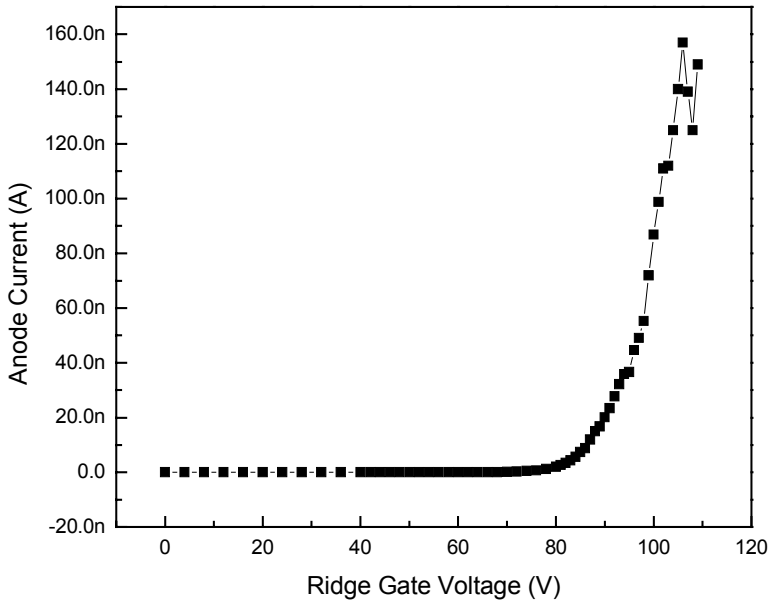

Figure F-3. IV characteristics of the 11th peak in Figure F-1.

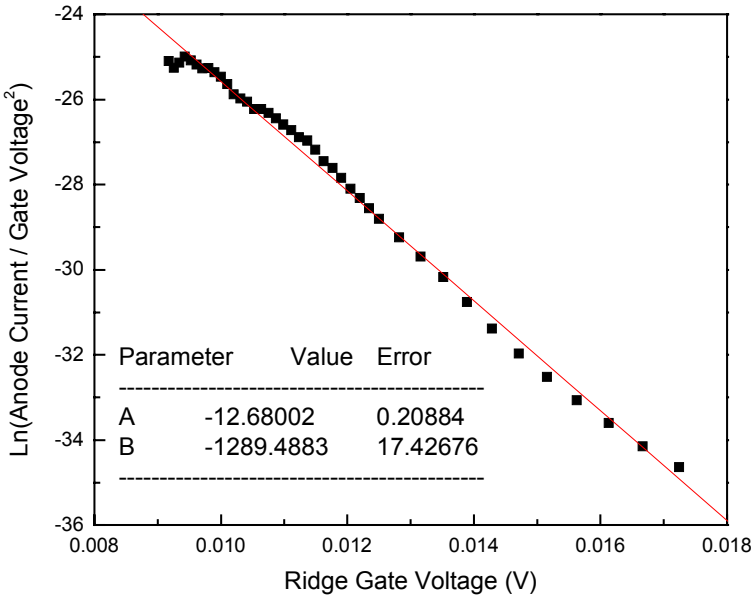

Figure F-4. FN plot of the 11th peak in Figure F-1.

Very high extraction gate leakage was found in the current-voltage characterization of the field emission ridge. The gate current in the same 21 up-down sweep measurement is

shown in Figure F-5. The gate leakage is more than 10 times larger than the anode current. The up-sweep of the 11th peak in Figure F-5 is shown in Figure F-6. The gate current increases exponentially with the extraction gate voltage but does not show the F-N characteristics. The large gate current might come from the dielectric layer leakage at the high operating gate voltages. Since the leakage at the low operating gate voltages is low, the device is not breakdown yet. Some of the gate current might come from the emission current, which was collected by the gate instead of the anode. However, it is hard to distinguish the dielectric leakage current and emission current.

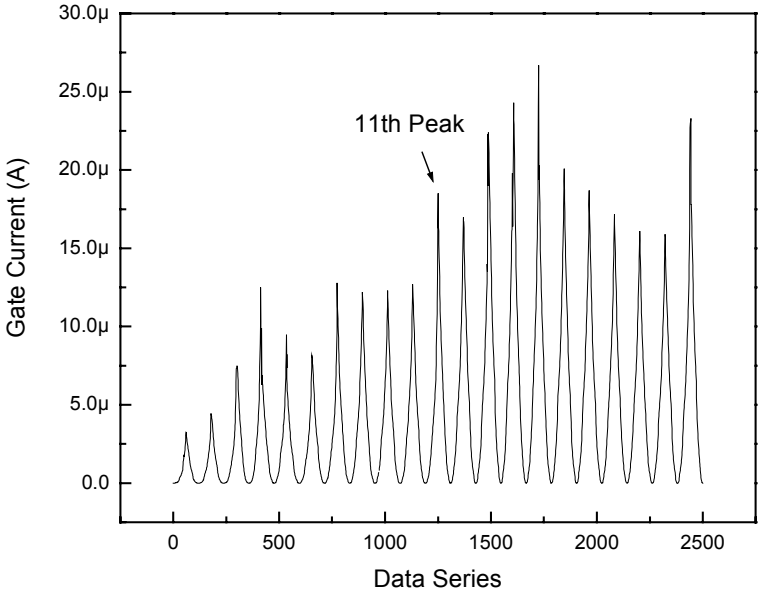

Figure F-5. The gate leakage as the extraction gate voltage up-down sweep for 21 times on a field emission ridge array.

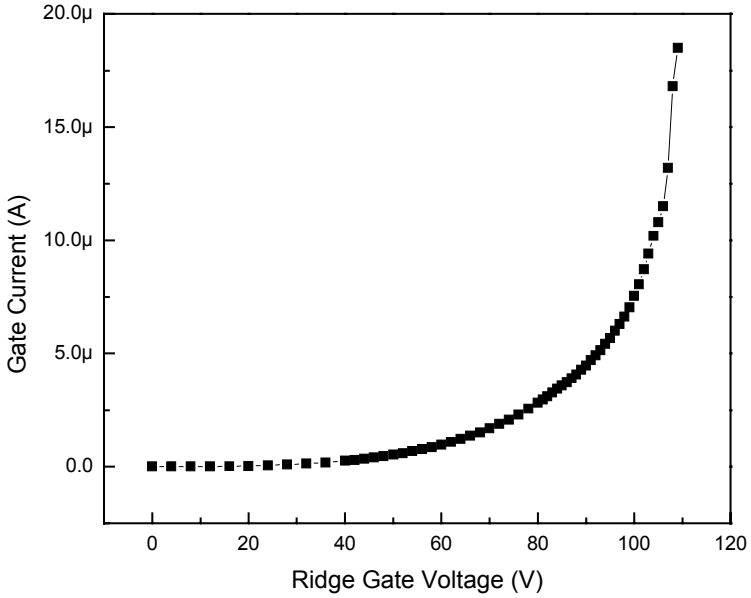

Figure F-6. The gate leakage-extraction gate voltage characteristics of the 11th peak in Figure F-5.

Field emission ridges were also integrated with LD-MOSFET. Unfortunately, LD-MOSFET has no control on the field emission ridges. This is because of the high extraction gate leakage. When the electron supply is controlled by the MOSFET, the electron goes to gate leakage instead of anode. Well LD-MOSFET controlled field emission ridge is expected once the extraction gate leakage is low.

G. I-V Characterization Results

The I-V characterization results shown in this thesis were picked from a bunch of experiment results. Here we present several data sets that we did not show in the previous chapters.

FEA Characterization

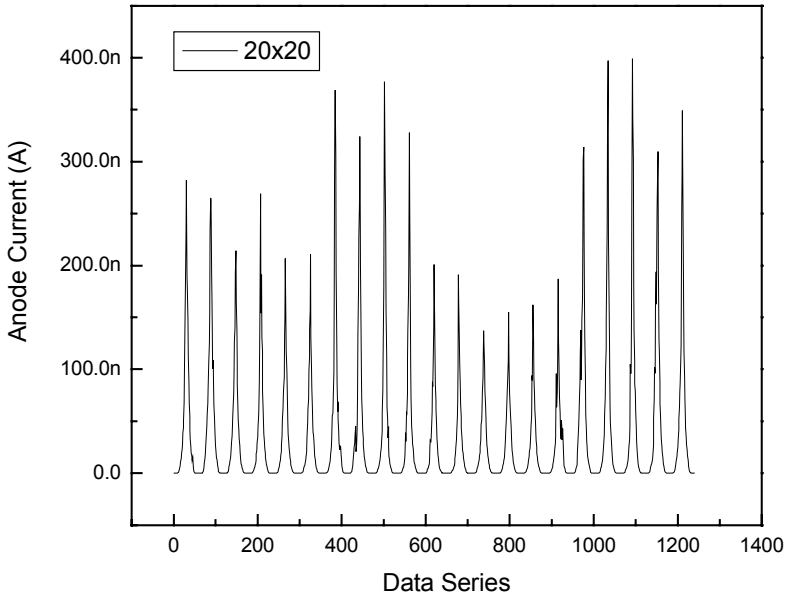

Figure G-1. I-V sweeps of a 20x20 FEA.

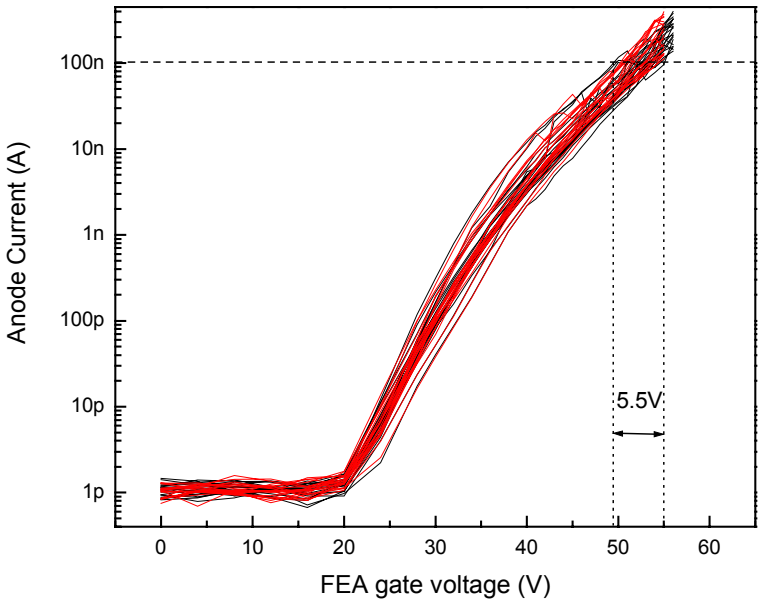

Figure G-2. Voltage spread of a 20x20 FEA at anode current of 100 nA.

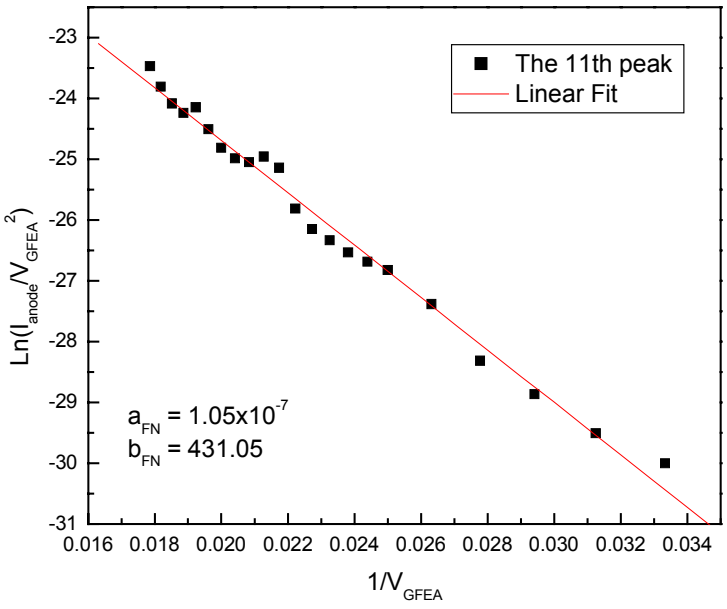

Figure G-3. Fowler-Nordheim plot of the 11th peak in Figure G-1.

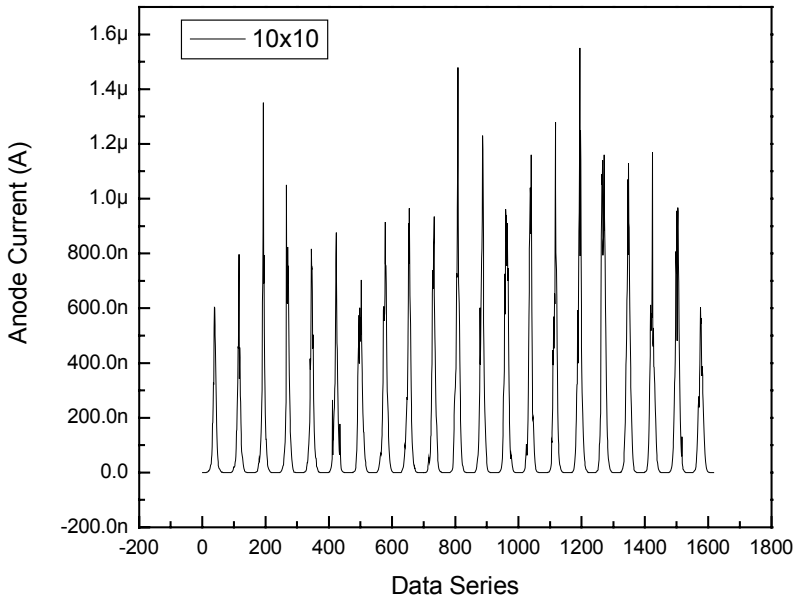

Figure G-4. I-V sweeps of a 10x10 FEA.

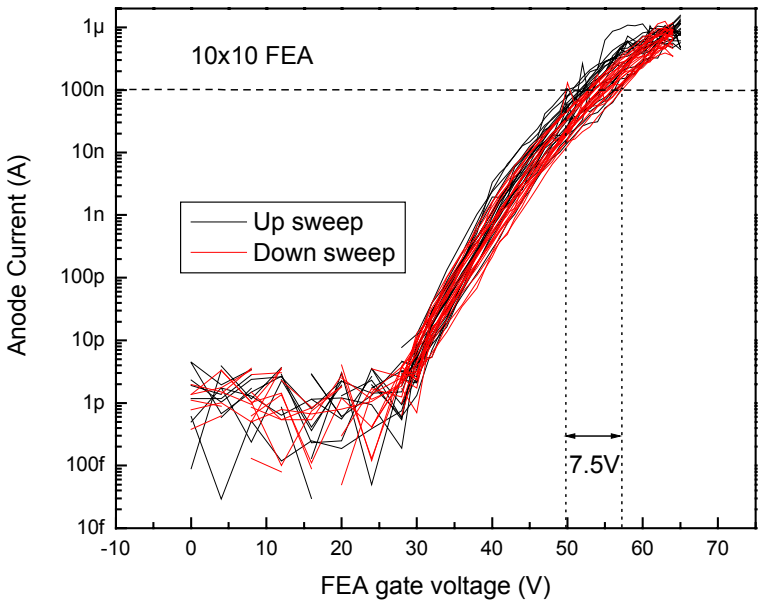

Figure G-5. Voltage spread of a 10x10 FEA at anode current of 100 nA.

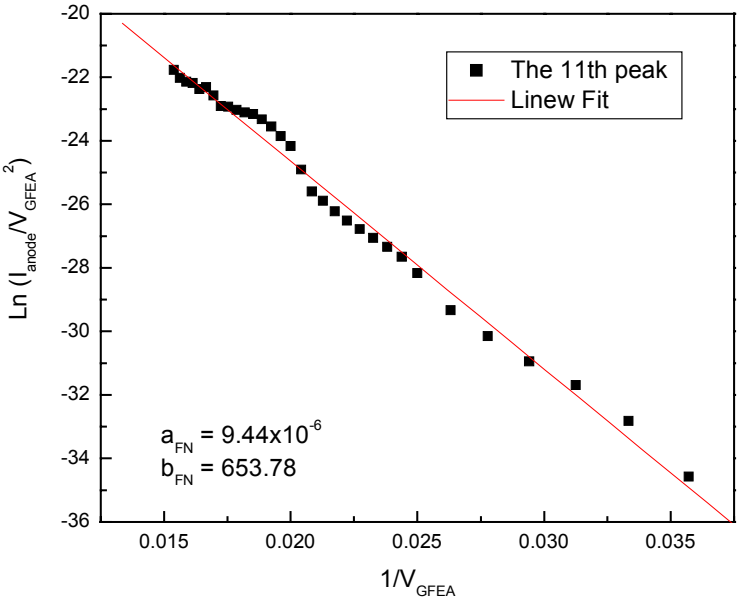

Figure G-6. Fowler-Nordheim plot of the 11th peak in Figure G-4.

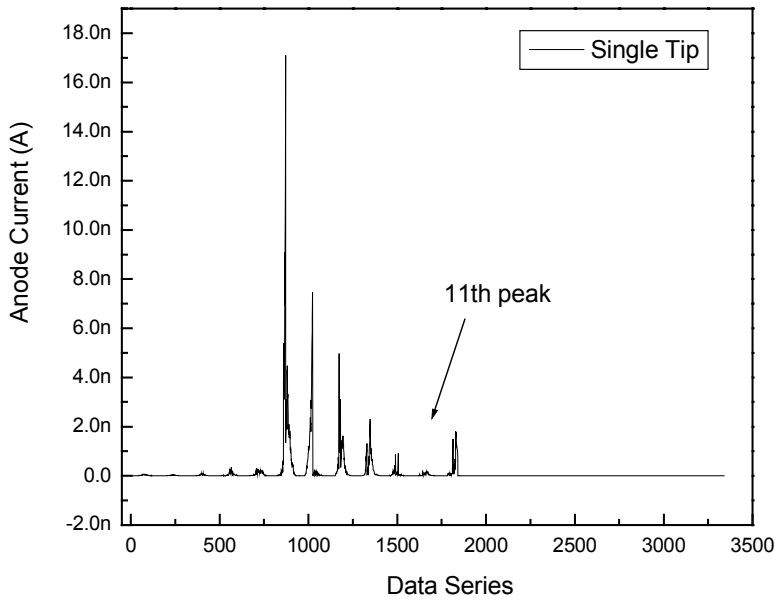

Figure G-7. I-V sweeps of a single emitter. The emitter went dead after the 12th sweep.

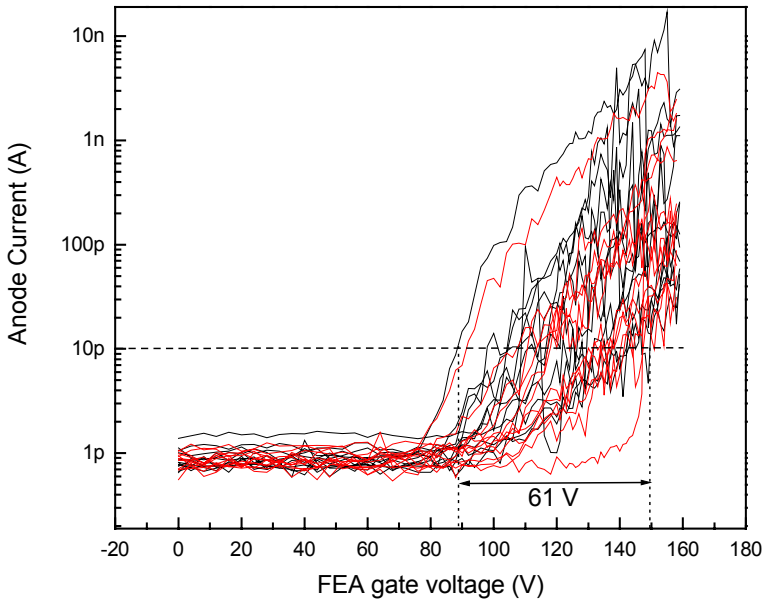

Figure G-8. Voltage spread of a single emitter at anode current of 10 pA.

LD-MOSFET/FEA Characterization

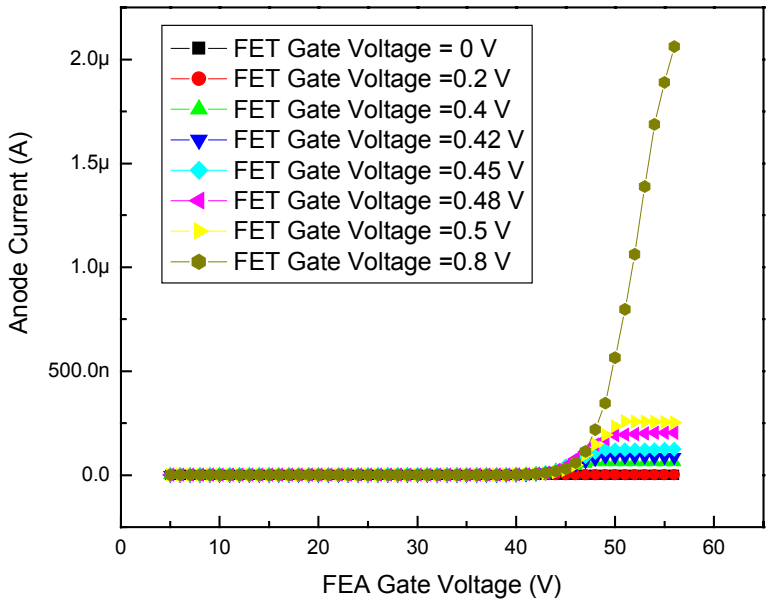

Figure G-9. Emission current as a function of FEA gate voltage of an integrated LD-MOSFET/FEA device. The integrated device has a FEA with 10x10 emitters and a MOSFET with channel width of 80 µm, channel length of 100 µm, and drift length of 100 µm.

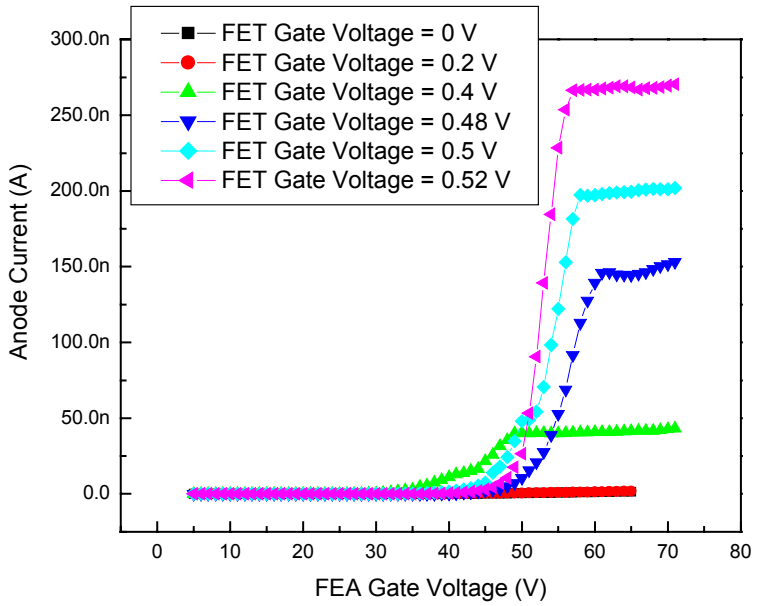

Figure G-10. Emission current as a function of FEA gate voltage of an integrated LD-MOSFET/FEA device. The integrated device has a FEA with 10x10 emitters and a MOSFET with channel width of 80 μm, channel length of 100 μm, and drift length of 100 μm.

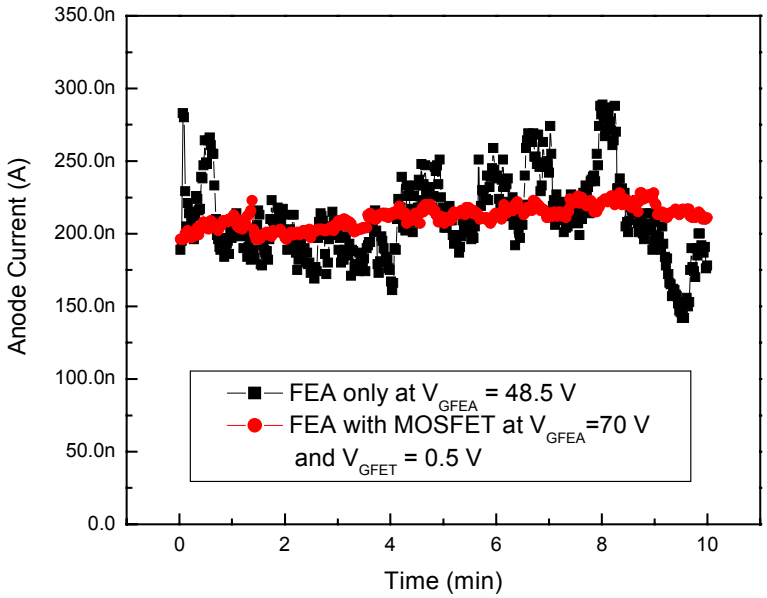

Figure G-11. Anode current comparison in an integrated LD-MOSFET/FEA device with and without MOSFET operation. V_{GFEA}= 48.5 V in the FEA device, while V_{GFEA}= 70 V in the integrated device to obtain the same anode current level.

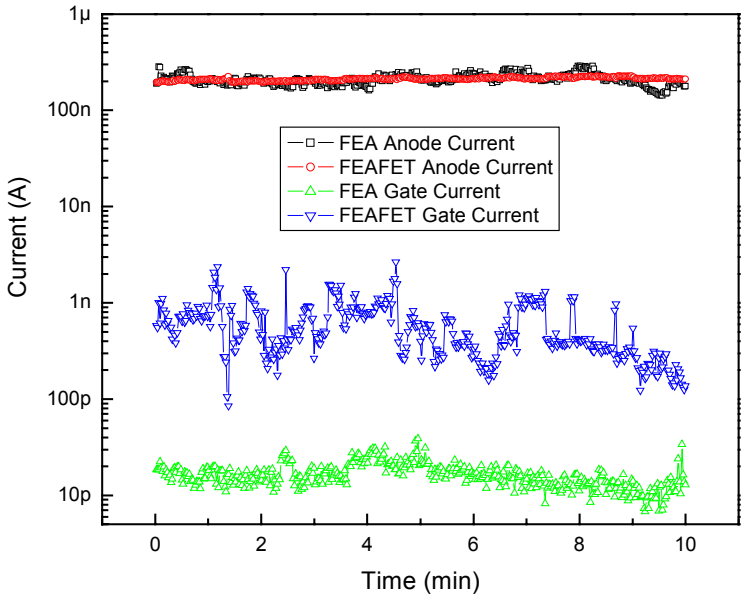

Figure G-12. FEA extraction gate current and anode current comparison in an integrated LD-MOSFET/FEA device with and without MOSFET operation in the same measurement as Figure G-11.

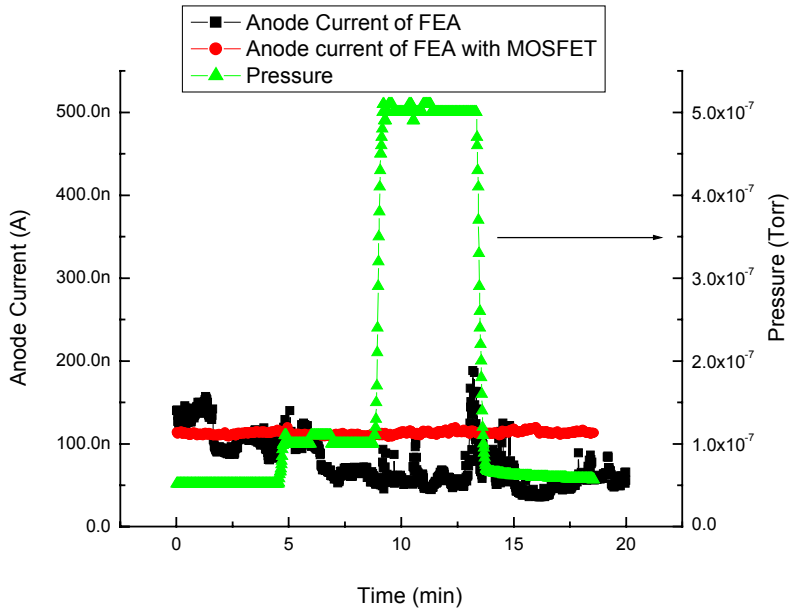

Figure G-13. Emission current stability in an integrated LD-MOSFET/FEA device with and without MOSFET control in hydrogen.

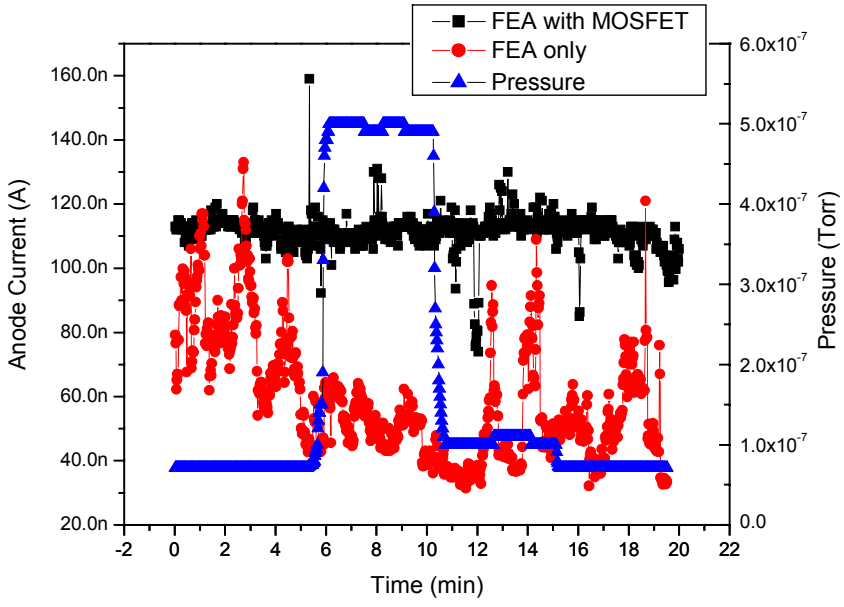

Figure G-14. Emission current stability in an integrated LD-MOSFET/FEA device with and without MOSFET control in nitrogen.

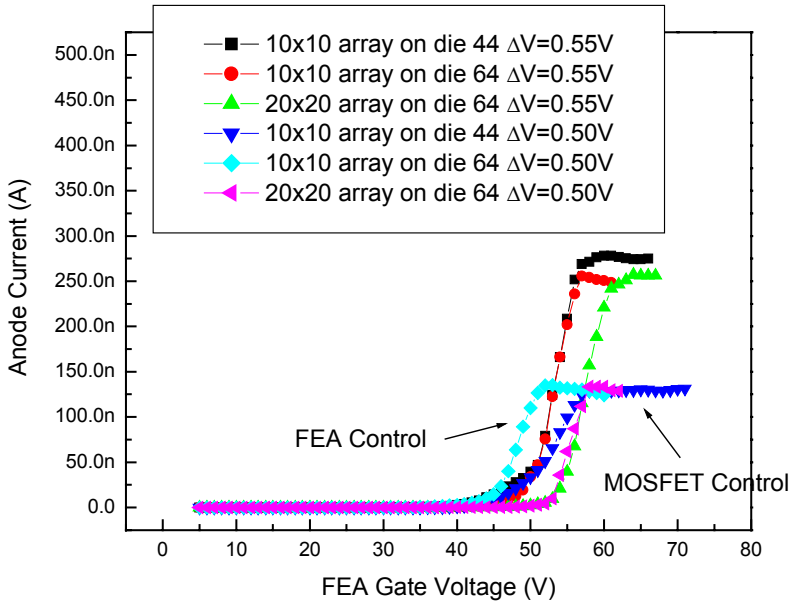

Figure G-15. Spatial emission current uniformity in the integrated LD-MOSFET/FEA devices at different positions on the wafer.

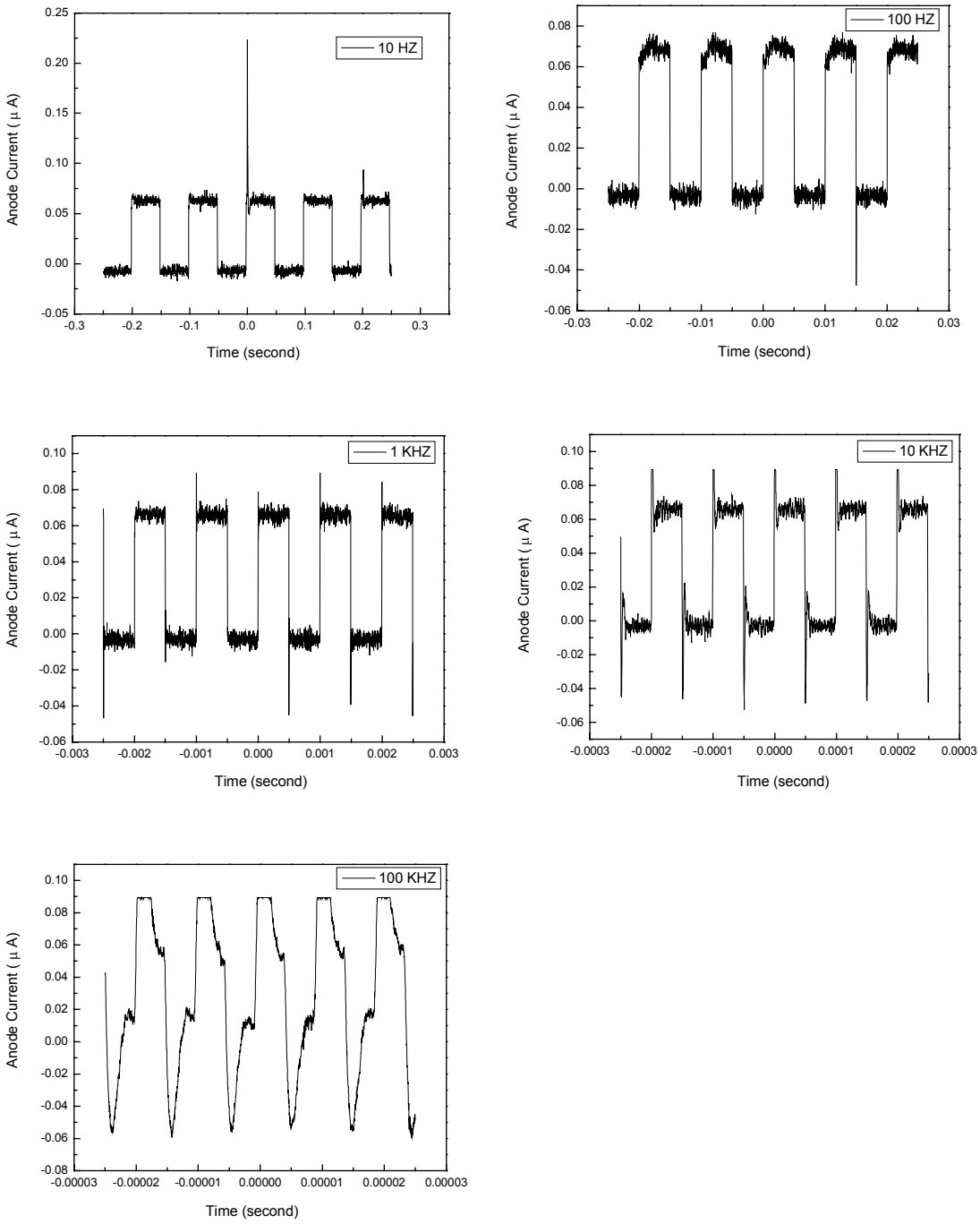

Figure G-16. The switch of an integrated LD-MOSFET/FEA device in different step function frequencies.

H. Sensitivity Analysis Derivation

(a) FEA Only

$$I = a_{FN} V^2 \exp(-b_{FN}/V),$$

$$a_{FN} = \frac{\alpha A \beta^2}{1.1\phi} \exp\left[\frac{B\left(1.44\ x10^{-7}\right)}{\phi^{1/2}}\right],$$

and

$$b_{FN} = \frac{0.95\, B\, \phi^{3/2}}{\beta}, \text{ where } \beta \sim 1/r$$

(i) Sensitivity with respect to work function

If r is constant,

$$I = f(\phi)$$

$$\Delta I = \frac{\partial I}{\partial \phi} \times \Delta\phi$$

$$\frac{\Delta I}{I} = \frac{\partial I / \partial \phi}{I} \times \Delta\phi$$

$$I = \frac{\alpha A \beta^2}{1.1\phi} \exp\left[\frac{B\left(1.44\times10^{-7}\right)}{\phi^{1/2}}\right] V^2 \exp\left(-\frac{0.95B\phi^{3/2}}{\beta V}\right)$$

$$\frac{\partial I}{\partial \phi} = \frac{-\alpha A \beta^2}{1.1\phi^2} \exp\left[\frac{B\left(1.44\times10^{-7}\right)}{\phi^{1/2}}\right] V^2 \exp\left(-\frac{0.95B\phi^{3/2}}{\beta V}\right)$$

$$-\frac{\left(0.72\times10^{-7}\right)\alpha AB\beta^2}{1.1\phi^{5/2}} \exp\left[\frac{B\left(1.44\times10^{-7}\right)}{\phi^{1/2}}\right] V^2 \exp\left(-\frac{0.95B\phi^{3/2}}{\beta V}\right)$$

$$-\frac{\left(1.425\right)\alpha A\beta}{1.1\phi^{1/2}} \exp\left[\frac{B\left(1.44\times10^{-7}\right)}{\phi^{1/2}}\right] VB \exp\left(-\frac{0.95B\phi^{3/2}}{\beta V}\right)$$

$$\frac{\Delta I}{I} = \frac{\partial I / \partial \phi}{I} \times \Delta\phi = \left[\frac{-1}{\phi} - \frac{0.72 \times 10^{-7} B}{\phi^{3/2}} - \frac{1.425 \phi^{1/2} B}{\beta V} \right] \times \Delta\phi$$

We can also express $\frac{dI}{d\phi}$ as the following equation

$$\frac{dI}{d\phi} = -\frac{\left[\frac{1}{\phi} + \frac{1.44 \times 10^{-7} B}{2\phi^{3/2}} + \frac{3}{2} \bullet \frac{0.95 B \phi^{1/2}}{\beta V} \right]}{\frac{1}{I}}$$

(ii) Sensitivity with respect to tip radius of curvature

If ϕ is constant,

$$I = f(r)$$

$$\frac{\Delta I}{I} = \frac{\partial I / \partial r}{I} \times \Delta r$$

$$I = \frac{\alpha A}{1.1 r^2 \phi} \exp\left[\frac{B\left(1.44 \times 10^{-7}\right)}{\phi^{1/2}} \right] V^2 \exp\left(\frac{-0.95 B r \phi^{3/2}}{V} \right)$$

$$\frac{\partial I}{\partial r} = \frac{-2\alpha A}{1.1 r^3 \phi} \exp\left[\frac{B\left(1.44 \times 10^{-7}\right)}{\phi^{1/2}} \right] V^2 \exp\left(\frac{-0.95 B r \phi^{3/2}}{V} \right)$$

$$- \frac{0.95 \alpha A \phi^{1/2}}{1.1 r^2} \exp\left[\frac{B\left(1.44 \times 10^{-7}\right)}{\phi^{1/2}} \right] VB \exp\left(\frac{-0.95 B r \phi^{3/2}}{V} \right)$$

$$\frac{\Delta I}{I} = \frac{\partial I / \partial r}{I} \times \Delta r = \left[\frac{-2}{r} - \frac{0.95 \phi^{3/2} B}{V} \right] \times \Delta r$$

We can also express $\frac{dI}{dr}$ as the following equation

$$\frac{dI}{dr} = -\frac{\left[\frac{2}{r} + \frac{0.95 B \phi^{3/2}}{V} \right]}{\frac{1}{I}}$$

(b) FEA with Resistor

$$I = \frac{\alpha A \beta^2}{1.1\phi} \exp\left[\frac{B\left(1.44x10^{-7}\right)}{\phi^{1/2}}\right] \bullet (V - IR)^2 \exp\left[-\frac{0.95B\phi^{3/2}}{\beta(V - IR)}\right]$$

(i) Sensitivity with respect to work function

Take logarithms of both sides to obtain

$$\log I = \log\left[\frac{\alpha A \beta^2}{1.1}\right] - \log\phi + \frac{1.44\times10^{-7} B}{\phi^{1/2}} + 2\log(V - IR) - \frac{0.95B\phi^{3/2}}{\beta(V - IR)}$$

Differentiate when V is constant

$$\frac{dI}{I} = -\frac{d\phi}{\phi} - \frac{1.44\times10^{-7} B}{2\phi^{3/2}} d\phi - \frac{2R}{(V - IR)} dI - \frac{0.95B}{\beta}\left[\frac{3}{2}\frac{\phi^{1/2}}{(V - IR)} d\phi + \frac{\phi^{3/2} R}{(V - IR)^2} dI\right]$$

$$dI\left[\frac{1}{I} + \frac{2R}{(V - IR)} + \frac{0.95B}{\beta} \bullet \frac{\phi^{3/2} R}{(V - IR)^2}\right] = -\left[\frac{1}{\phi} + \frac{1.44\times10^{-7} B}{2\phi^{3/2}} + \frac{3}{2} \bullet \frac{0.95B\phi^{1/2}}{\beta(V - IR)}\right] d\phi$$

$$\frac{dI}{d\phi} = -\frac{\left[\frac{1}{\phi} + \frac{1.44\times10^{-7} B}{2\phi^{3/2}} + \frac{3}{2} \bullet \frac{0.95B\phi^{1/2}}{\beta(V - IR)}\right]}{\left[\frac{1}{I} + \frac{2R}{(V - IR)} + \frac{0.95B}{\beta} \bullet \frac{\phi^{3/2} R}{(V - IR)^2}\right]}$$

(ii) Sensitivity with respect to tip radius of curvature

Take logarithms of both sides to obtain

$$\log I = \log\left[\frac{\alpha A}{1.1\phi}\right] - 2\log r + \frac{1.44\times10^{-7} B}{\phi^{1/2}} + 2\log(V - IR) - \frac{0.95Br\phi^{3/2}}{(V - IR)}$$

Differentiate when V is constant

$$\frac{dI}{I} = -\frac{2dr}{r} - \frac{2\,R}{(V-IR)}\,dI - 0.95B\phi^{3/2}\left[\frac{1}{(V-IR)}dr + \frac{rR}{(V-IR)^2}dI\right]$$

$$dI\left[\frac{1}{I} + \frac{2R}{(V-IR)} + \frac{0.95Br\phi^{3/2}R}{(V-IR)^2}\right] = -\left[\frac{2}{r} + \frac{0.95B\phi^{3/2}}{(V-IR)}\right]dr$$

$$\frac{dI}{dr} = -\frac{\left[\frac{2}{r} + \frac{0.95B\phi^{3/2}}{(V-IR)}\right]}{\left[\frac{1}{I} + \frac{2R}{(V-IR)} + \frac{0.95Br\phi^{3/2}R}{(V-IR)^2}\right]}$$

How do $\frac{dI}{d\phi}$ and $\frac{dI}{dr}$ change with R?

$$\frac{1}{I} = \frac{1}{\frac{\alpha A\beta^2}{1.1\phi}\exp\left[\frac{B(1.44x10^{-7})}{\phi^{1/2}}\right]\bullet(V-IR)^2\exp\left[-\frac{0.95B\phi^{3/2}}{\beta(V-IR)}\right]} = \frac{\exp\left[\frac{0.95B\phi^{3/2}}{\beta(V-IR)}\right]}{k_0(V-IR)^2}$$

$$\frac{dI}{d\phi} = -\frac{\left[\frac{1}{\phi} + \frac{1.44\times10^{-7}B}{2\phi^{3/2}} + \frac{3}{2}\bullet\frac{0.95B\phi^{1/2}}{\beta(V-IR)}\right]}{\left[\frac{1}{I} + \frac{2R}{(V-IR)} + \frac{0.95B}{\beta}\bullet\frac{\phi^{3/2}R}{(V-IR)^2}\right]} = -\frac{\left[k_1 + \frac{3}{2}\bullet\frac{0.95B\phi^{1/2}}{\beta(V-IR)}\right]}{\left[\frac{\exp\left[\frac{0.95B\phi^{3/2}}{\beta(V-IR)}\right]}{k_0(V-IR)^2} + \frac{2R}{(V-IR)} + \frac{0.95B}{\beta}\bullet\frac{\phi^{3/2}R}{(V-IR)^2}\right]}$$

$$= -\frac{\left[k_1(V-IR)+k_2\right]}{\left[\frac{\exp\left[\frac{0.95B\phi^{3/2}}{\beta(V-IR)}\right]}{k_0(V-IR)}+2R+\frac{0.95B}{\beta}\bullet\frac{\phi^{3/2}R}{(V-IR)}\right]}$$

When R increases, IR increases, and V-IR decreases. Therefore, the numerator decreases, the denominator increases, and $\frac{dI}{d\phi}$ decreases while R increases.

$$\frac{dI}{dr} = -\frac{\left[\frac{2}{r}+\frac{0.95B\phi^{3/2}}{(V-IR)}\right]}{\left[\frac{1}{I}+\frac{2R}{(V-IR)}+\frac{0.95Br\phi^{3/2}R}{(V-IR)^2}\right]} = -\frac{\left[k_3+\frac{0.95B\phi^{3/2}}{(V-IR)}\right]}{\left[\frac{\exp\left[\frac{0.95B\phi^{3/2}}{\beta(V-IR)}\right]}{k_0(V-IR)^2}+\frac{2R}{(V-IR)}+\frac{0.95Br\phi^{3/2}R}{(V-IR)^2}\right]}$$

$$= -\frac{\left[k_3(V-IR)+k_4\right]}{\left[\frac{\exp\left[\frac{0.95B\phi^{3/2}}{\beta(V-IR)}\right]}{k_0(V-IR)}+2R+\frac{0.95B}{\beta}\bullet\frac{\phi^{3/2}R}{(V-IR)}\right]}$$

Similar to $\frac{dI}{d\phi}$, the numerator decreases, the denominator increases, and $\frac{dI}{dr}$ decreases while R increases.

When R is very large, the voltage drop across the resistor, $V_R = IR$ is also very large, $V - IR << 1$, and I << 1,

$$\frac{dI}{d\phi} = -\frac{\left[\frac{1}{\phi} + \frac{1.44\times10^{-7}B}{2\phi^{3/2}} + \frac{3}{2}\bullet\frac{0.95B\phi^{1/2}}{\beta(V-IR)}\right]}{\left[\frac{1}{I} + \frac{2R}{(V-IR)} + \frac{0.95B}{\beta}\bullet\frac{\phi^{3/2}R}{(V-IR)^2}\right]} \approx -\frac{\left[\frac{3}{2}\bullet\frac{0.95B\phi^{1/2}}{\beta(V-IR)}\right]}{\left[\frac{1}{I} + \frac{0.95B}{\beta}\bullet\frac{\phi^{3/2}R}{(V-IR)^2}\right]}$$

$$\frac{dI}{dr} = -\frac{\left[\frac{2}{r} + \frac{0.95B\phi^{3/2}}{(V-IR)}\right]}{\left[\frac{1}{I} + \frac{2R}{(V-IR)} + \frac{0.95Br\phi^{3/2}R}{(V-IR)^2}\right]} \approx -\frac{\left[\frac{0.95B\phi^{3/2}}{(V-IR)}\right]}{\left[\frac{1}{I} + \frac{0.95Br\phi^{3/2}R}{(V-IR)^2}\right]}$$

Since

$$\frac{1}{I} = \frac{1}{\frac{\alpha A\beta^2}{1.1\phi}\exp\left[\frac{B(1.44x10^{-7})}{\phi^{1/2}}\right]\bullet(V-IR)^2\exp\left[-\frac{0.95B\phi^{3/2}}{\beta(V-IR)}\right]} \approx \frac{\exp\left[\frac{0.95B\phi^{3/2}}{\beta(V-IR)}\right]}{(V-IR)^2}$$

$$\frac{1}{I} >> \frac{0.95Br\phi^{3/2}R}{(V-IR)^2}$$

$$\frac{dI}{d\phi} \approx -\frac{\left[\frac{3}{2}\bullet\frac{0.95B\phi^{1/2}}{\beta(V-IR)}\right]}{\left[\frac{1}{I} + \frac{0.95B}{\beta}\bullet\frac{\phi^{3/2}R}{(V-IR)^2}\right]} \approx -\frac{I}{V-IR} \approx -(V-IR)\bullet\exp\left[-\frac{0.95B\phi^{3/2}}{\beta(V-IR)}\right]$$

$$\frac{dI}{dr} \approx -\frac{\left[\frac{0.95B\phi^{3/2}}{(V-IR)}\right]}{\left[\frac{1}{I} + \frac{0.95Br\phi^{3/2}R}{(V-IR)^2}\right]} \approx -\frac{I}{V-IR} \approx -(V-IR)\bullet\exp\left[-\frac{0.95B\phi^{3/2}}{\beta(V-IR)}\right]$$

To the limit, $R \to \infty$ $\frac{dI}{d\phi} \to 0$ and $\frac{dI}{dr} \to 0$.

(c) FEA with Current Source

$$I_E = \frac{\alpha A \beta^2}{1.1\phi} \exp\left[\frac{B\left(1.44\times10^{-7}\right)}{\phi^{1/2}}\right]\left(V_{GFEA} - (I_E - I_0)R\right)^2 \exp\left[-\frac{0.95B\phi^{3/2}}{\beta\left(V_{GFEA} - (I_E - I_0)R\right)}\right].$$

(i) Sensitivity with respect to work function

Take logarithms of both sides to obtain

$$\log I = \log\left[\frac{\alpha A \beta^2}{1.1}\right] - \log\phi + \frac{1.44\times10^{-7}B}{\phi^{1/2}} + 2\log\left(V - \left(I_E - I_0\right)R\right) - \frac{0.95B\phi^{3/2}}{\beta\left(V - \left(I_E - I_0\right)R\right)}$$

Differentiate when V is constant

$$\frac{dI}{d\phi} = -\frac{\left[\frac{1}{\phi} + \frac{1.44\times10^{-7}B}{2\phi^{3/2}} + \frac{3}{2}\bullet\frac{0.95B\phi^{1/2}}{\beta\left(V - \left(I_E - I_0\right)R\right)}\right]}{\left[\frac{1}{I_E} + \frac{2R}{\left(V - \left(I_E - I_0\right)R\right)} + \frac{0.95B}{\beta}\bullet\frac{\phi^{3/2}R}{\left(V - \left(I_E - I_0\right)R\right)^2}\right]}$$

(ii) Sensitivity with respect to tip radius of curvature

Take logarithms of both sides to obtain

$$\log I = \log\left[\frac{\alpha A}{1.1\phi}\right] - 2\log r + \frac{1.44\times10^{-7}B}{\phi^{1/2}} + 2\log\left(V - \left(I_E - I_0\right)R\right) - \frac{0.95Br\phi^{3/2}}{\left(V - \left(I_E - I_0\right)R\right)}$$

Differentiate when V is constant

$$\frac{dI}{dr} = -\frac{\left[\frac{2}{r} + \frac{0.95B\phi^{3/2}}{\left(V - \left(I_E - I_0\right)R\right)}\right]}{\left[\frac{1}{I_E} + \frac{2R}{\left(V - \left(I_E - I_0\right)R\right)} + \frac{0.95Br\phi^{3/2}R}{\left(V - \left(I_E - I_0\right)R\right)^2}\right]}$$

(d) Sensitivity with respect to V_{GFEA}

$$I = a_{FN} V^2 \exp\left[-\frac{b_{FN}}{V}\right],$$

$$a_{FN} = \frac{\alpha A \beta^2}{1.1\phi} \exp\left[\frac{B\left(1.44\ x10^{-7}\right)}{\phi^{1/2}}\right],$$

and

$$b_{FN} = \frac{0.95\, B\, \phi^{3/2}}{\beta}.$$

When there is a series resistor R

$$I = a_{FN} (V - IR)^2 \exp\left[-\frac{b_{FN}}{(V - IR)}\right],$$

Take logarithms of both sides

$$\log I = \log a_{FN} + 2 \log (V - IR) - \frac{b_{FN}}{(V - IR)}$$

Differentiate

$$\frac{dI}{I} = 2\left[\frac{1}{(V - IR)} dV - \frac{R}{(V - IR)} dI\right] + \frac{b_{FN}}{(V - IR)^2} [dV - R dI]$$

$$dI\left[\frac{1}{I} + \frac{2 \bullet R}{(V - IR)} + \frac{R \bullet b_{FN}}{(V - IR)^2}\right] = dV\left[\frac{2}{(V - IR)} + \frac{b_{FN}}{(V - IR)^2}\right]$$

$$\frac{dI}{dV} = \frac{\left[\frac{2}{(V - IR)} + \frac{b_{FN}}{(V - IR)^2}\right]}{\left[\frac{1}{I} + \frac{2 \bullet R}{(V - IR)} + \frac{R \bullet b_{FN}}{(V - IR)^2}\right]}$$

I. Langmuir Equation Derivation

Assumptions:

(1) The adsorptive properties of all sites are identical.

(2) There are no lateral interactions between neighboring adsorbed molecules.

The adsorbate-adsorbent system is at equilibrium. The total number of the sites is N_s (cm^{-2}) and the number of sites that are occupied by adsorbed molecules is N (cm^{-2}). The rate of adsorption per area per second is

$$\frac{dn}{dt} = k_a P(N_s - N)$$

where k_a (in s^{-1}) is the rate constant per site for unit pressure. The rate of desorption per area per second is

$$\frac{dn}{dt} = k_d N$$

where k_d (in s^{-1}) is the rate constant per adsorbed molecule for desorption.

At equilibrium,

$k_a P(N_s - N) = k_d N$,

or

$k_a P(\upsilon_m - \upsilon) = k_d \upsilon$

where υ is the volume of gas adsorbed and υ_m is the volume to give a complete monolayer, both in units of cm^3. Hence,

$\upsilon = k_a P \upsilon_m / (k_a P + k_d)$

Since the fractional coverage is

$\theta = N / N_s = \upsilon / \upsilon_m$,

$\theta = k_a P / (k_a P + k_d)$ [I.1].

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Chapter 1

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