Next Generation Optical Receivers: Integration and New Materials Platform

by

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Yiwen (Emily) Zhang

Submitted to the Department of Materials Science and Engineering on August 2, 2004 in partial fulfillment of the requirements for the Degree of Master of Engineering in Material Science

Abstract

Future growth of optical communication into new application and market space is highly dependent on the ability of optical receivers to increase functionality while reducing price and physical size. Current hybrid receiver technology is inadequate in meeting the cost and performance demands of future market. Monolithic integration and new material systems are potential solutions and have been the focus of research investigation. This thesis summarizes the research progress of monolithic integration on InP, and the achievements in realizing 1.55μm photodetector on GaAs and Si and their potentials for monolithic opto-electronic integrated circuits. The overall trend for next generation receivers is to move towards higher levels of integration, with investigation in new material systems that have the potentials for lower cost and larger scale integration. The impact of monolithic integration optical receiver components is analyzed in a cost analysis model.

Thesis Supervisor: Lionel C. Kimerling
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Contributions:

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I would like to thank my wonderful parents, for their love and teaching that has brought me to where I am. You have always been the wind under my wings. Thanks to my little brother Kevin, at four years old you have helped me in ways you could not have imagined.

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I. Introduction

Advantages of Fiber-Optics

The need to communicate began once humans were aware of each other and the world around us, beginning with the primitive ways of sound, visible signaling and writing which lasted thousands of years. About one hundred years ago, new ways of communication were made possible through technologies such as telephone or radio. These new technologies made amazing advances in the way people could connect to each other and started the phenomena of "shrinking world". Communication technology continually seeks to increase the amount of information and the distance over which it can travel. This is characterized as a bandwidth-distance product and it is an important figure of merit for communication media:

$$\text{Bandwidth} \times \text{Distance Product} = \text{Allowable bandwidth} \times \text{distance over which certain attenuation results} \quad (1)$$

Another new generation of communication media came along in the 1950's, about fifty years after radio and telephone changed the world. The idea was to use light to send large amounts of information over long distances through an optical fiber. In effect, the optical communication link was able to offer much greater bandwidth-distance product than conventional metallic or wireless links. The first optical fiber link went to service in 1982 between St. Louis and Chicago to carry long distance phone calls. Since then, optical communication has penetrated just about every continent, supporting everything we do from phone calls, Internet, banking transactions, etc. Figure 1 shows the optical network connections around in the world in 2002.

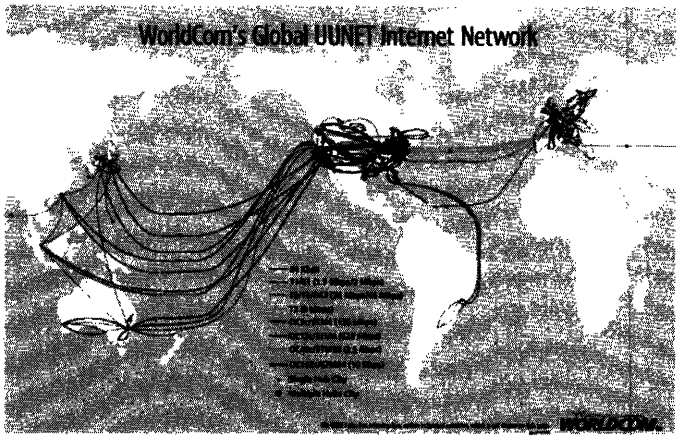
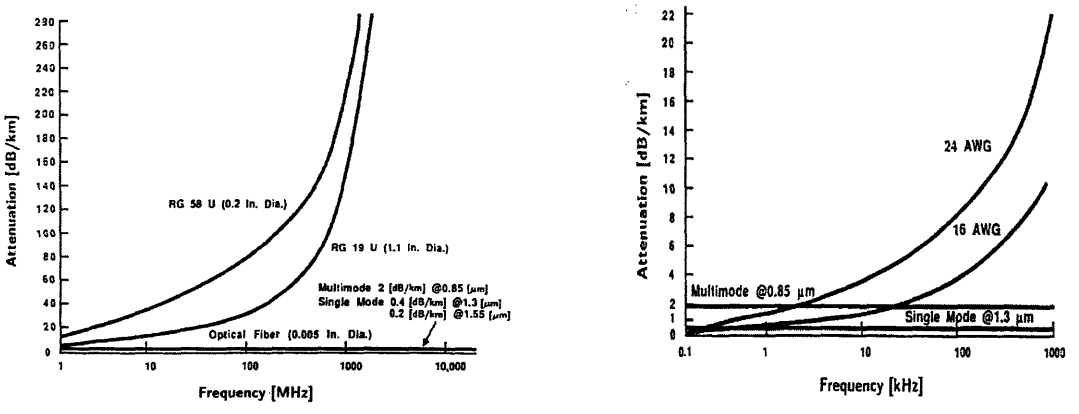


Figure 1: Optical network in the world as of 2002 (©MCI) [1]

The significant advantage of optical fiber over traditional twisted pair or coaxial copper cable is its high bandwidth-distance product. Generally for any communication media, as the bandwidth increases, the distance over which signal can be transmitted without significant loss or distortion tends to decrease. Current commercially available fibers have 3dB/km of attenuation loss at 1550nm wavelength, with less than 2dB/km demonstrated in the laboratory. In comparison, the attenuation of copper cable is about 1dB/m at 1GHz. Charts in Figure 2 compare the attenuation of optical fiber, twisted pair and coaxial cable at different frequencies.



(a) (b)

Figure 2: (a) Attenuation vs. frequency for optical fiber and coaxial cable. (b) Attenuation vs. frequency for optical fiber and twisted pair wire (©Hussperger 1995)

Both figures show that metallic wires are useful for transmission over relatively short paths, at frequencies up to about 100MHz. Beyond those distances and frequencies, attenuation becomes too great for useful transmission. But attenuation in optical fiber is insignificant even at frequencies up to 10GHz. Even at very high frequencies, the bandwidth-distance product is limited not by attenuation but rather by signal dispersion, where tightly spaced signals become smeared out as they travel down the fiber.

Fiber-optic technology revolutionized the way people could connect to each other in the world. Figure 3 shows that for about 80 years, information capacity has increased at a relatively linear rate. But optical communication, as a disruptive technology, dramatically increased communication information capacity.

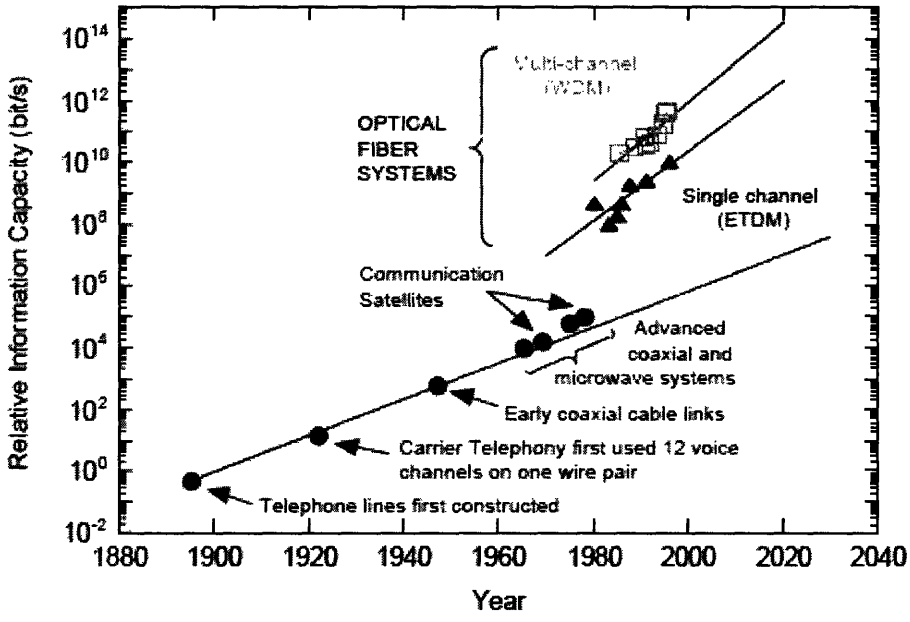


Figure 3: Growth in information carrying capacity of a single communications line over time (© Kimerling 2003)

Fiber-optic Link

The fiber-optic network is a network of optical links. Each link consists of a transmitter that generates the light signal, a certain length of fiber in which the light travels through and a receiver where light is detected. The link can also include passive optical devices such as filters and couplers that separate or add in a certain wavelength. Figure 4 shows the schematic of a simple optical link.

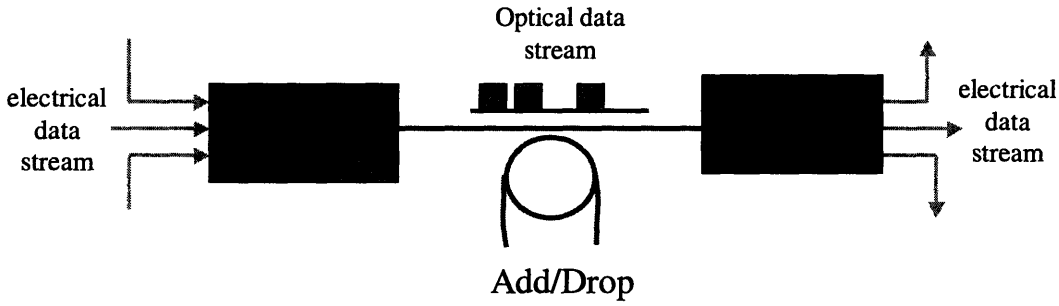
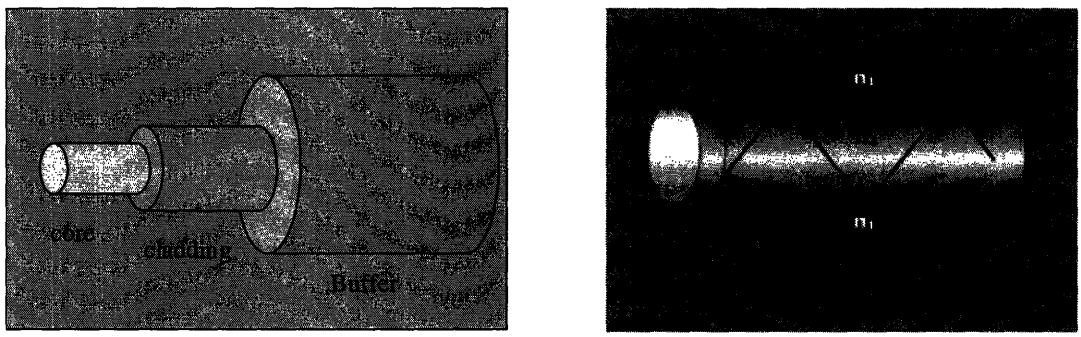


Figure 4: Schematic of optical link

Fiber

The optical fiber consists of a high refractive index core surrounded by a lower index cladding, as shown in Figure 5(a). Both core and cladding are made from silica glass, with chemical dopants introduced in the core to decrease its index of refraction.



(a) (b)

Figure 5: (a) Optical fiber structure. (b). Total internal reflection (© Corning)

Light is guided within the fiber through total internal reflection, as shown in Figure 5(b). Although information can be transmitted with the whole spectrum of light frequencies, wavelength of 1300nm and 1550nm were chosen for long distance communication. Communication at those wavelengths resulted in minimum attenuation and dispersion in the fiber. Figure 6 shows fiber attenuation versus wavelength.

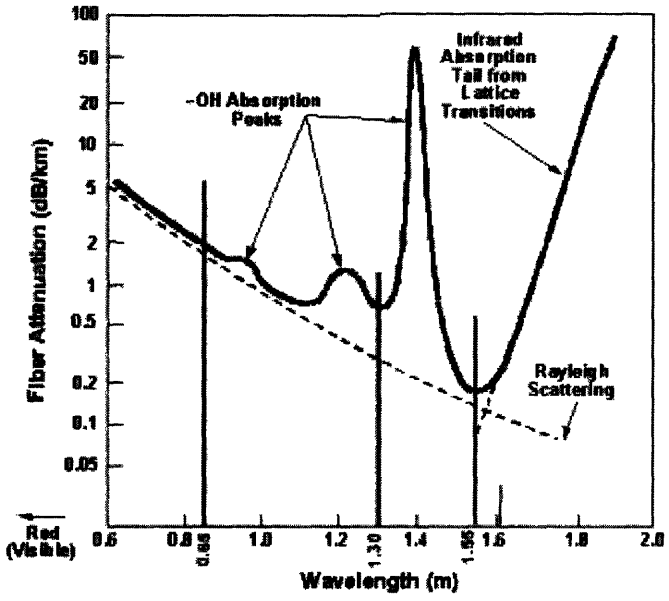


Figure 6: Fiber attenuation vs. light wavelength. [1]

Transmitter and Receiver

On the transmitter side, electrical signals generated from computers are routed together. These signals can be multiplexed in time through time-division-multiplexing (TDM), where a circuit generates clock information and assigns that to each packet of information. The information is passed on to the modulator, which modulates the light beam from the laser by turning it on and off. Light-on represents a 1 and light-off represents a 0. At the receiver, a photodetector converts the incoming light signal into current. This current is fed into a trans-impedance amplifier (TIA), which amplifies it and converts it into voltage signal. The signal passes through some more electronics processing and eventually show up as data on a computer screen or voice through a microphone.

What this thesis seeks to address:

This thesis discusses the current state of optical receiver technology and its limitations in meeting the demands of future market needs. Monolithic opto-electronic integration on InP, GaAs and Si has been under research investigation to address the limitations of current technology. This thesis presents and compares their demonstrated results on integration and manufacturing capability. The role of integration in receiver cost is analyzed through cost analysis.

II. Current Optical Receiver Technology

The most basic components in an optical receiver are: photodetector and trans-impedance amplifier (TIA). Most receivers will also include more amplifiers, filters, demultiplexing and signal-reshape circuitries.

Assembly and Packaging

Current optical receiver modules are assembled through hybrid integration. The photodiodes, TIAs and other electronic components are manufactured discretely, usually with different material systems that separately optimize performance and cost. Each component is separately packaged, in what are called optical subassembly (OSA). The purpose of the OSA is to best couple light between the fiber and the photodiode. OSA usually consists of electro-optical transformer (photodiodes), optical beam transformer (lenses) and a precise mechanical dock for fiber alignment. The optical components are mounted on a header with electrical leads for connections. Figure 7 shows a picture for a photodiode OSA.

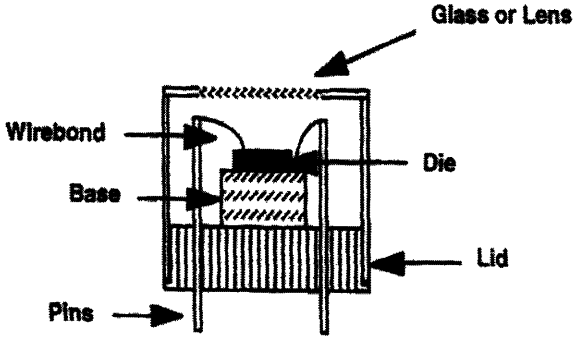


Figure 7: Schematic cross-section view of photodiode optical subassembly package [5]

Lenses or system of lenses are needed to collimate and focus the light from the fiber unto the detector surface. Fiber alignment performed by activating the photodiode during alignment to search for optimum position that gives high coupling efficiency.

The OSA is mounted on a submount and is electrically connected through wire bonding or flip-chip to other electronic circuitry on the receiver module. Figure 8 shows a picture of a receiver.

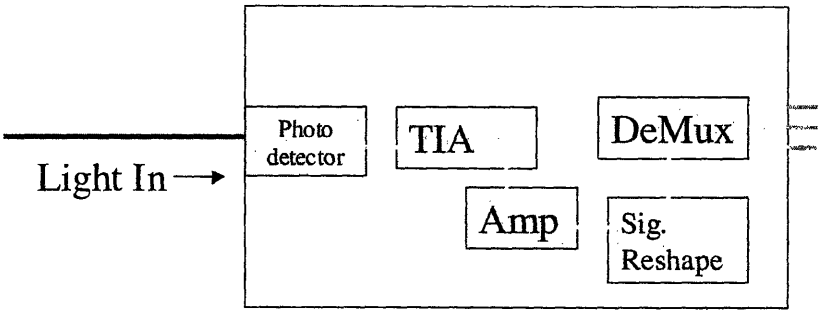


Figure. 8. Schematic of receiver module

After the components and fiber are all fixed in place, the metal package is sealed to prevent environmental stresses.

Photodetector

This section discusses the photodetector in more detail, the only optically active device in a receiver. Today's receivers generally use PIN photodiodes or avalanche photodiodes. Both of these diodes function as reverse biased junctions with certain depletion width. When light illuminates the diode, the photons will generate electron-hole pairs in the depletion region. The carriers are swept to the electrodes by applied electric field and are collected as current. Thus incoming light signal is converted into a current signal. Following section will present some figure of merit for photodetectors. For a detailed discussion of the physics of photodetector operation please refer to Solid State Electronic Devices, 5th edition, by Ben Streetman.

Photodetector Basics

Figure 9 shows a simple PIN photodiode structure:

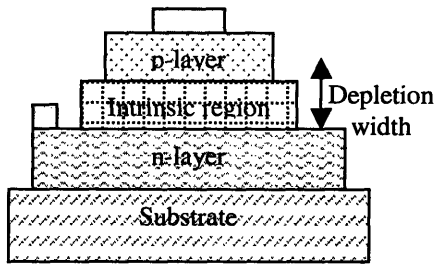


Fig. 9. Schematic of simply PIN photodiode structure

In choosing a photodetector for a particular application, one would like to have:

- High quantum efficiency (η), the efficiency carrier generation by photons.

$$\eta = (1-R)T(1-\exp(-\alpha w)) \qquad (2)$$

where

R: light reflection at diode surface

T: charge collection efficiency at the junction

α: absorption coefficient of depletion region

w: width of depletion region

- High responsivity: Amount of current generated per watt of incident light.

$$R = \eta q/h\nu \qquad (3)$$

Where

q: charge of electron

h: Planck's constant

ν: frequency of incoming light

- Fast speed, also referred to as bandwidth. Bandwidth equals the inverse of response time, τ.
    - If response time is limited by the time carriers take to travel to the electrodes:

$$\tau = w/v_d \quad (4)$$

Where

w: width of depletion region

v_d: carrier drift velocity under bias

    - If response time is limited by RC time constant:

$$\tau = RC \quad (5)$$

where

R: diode or circuit resistance

C: diode or circuit capacitance

- Low noise: distortions in the signal.

$$\text{Noise power} = i^2_{n,shot} + i^2_{n,thermal} \quad (6)$$

Where

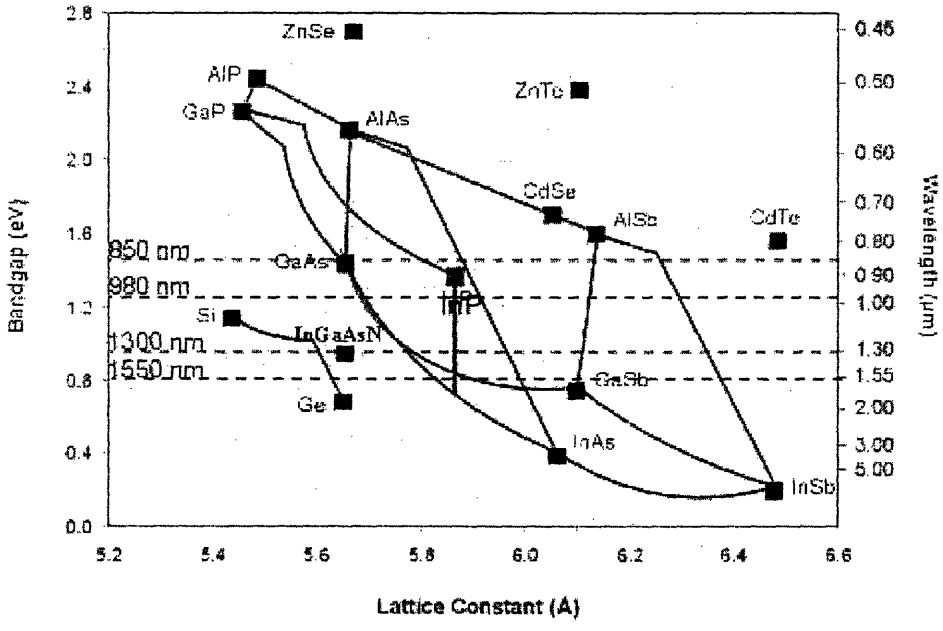
$i^2_{n,shot}$: shot noise, arises from thermal generation of electron-hole pair

$i^2_{n,thermal}$: thermal noise, arises from higher resistance at higher temperature

A good photodetector should have high quantum efficiency, responsivity, bandwidth and low noise. Both PIN diodes and avalanche diodes operate in similar fashion, except avalanche diodes have a gain mechanism and can detect very weak optical signals. PIN diodes are generally suitable for low-noise applications, and the photodiodes that this thesis refers to will be PIN diodes.

Photodetector Material System

As discussed in Chapter I, the wavelength of communication is dictated by the attenuation and dispersion spectrum of silica glass fiber. Wavelength of 1300nm and 1550nm became the wavelength-of-choice for they resulted in lowest dispersion and attenuation. These wavelengths in turn determine the material system for photodetectors. Today's photodetectors are generally made with semiconductor materials. For high quantum efficiency, the semiconductor bandgap needs to match incoming photon energy (0.95eV for 1300nm and 0.8eV for 1550nm). Materials with bandgap too large will be transparent at those wavelengths. But materials with bandgap too small will have poor responsivity because most of the incident photons will be absorbed by a thin surface film. Figure 10 shows the bandgap energy and lattice constant for a number of semiconductors and their composition alloys.



Lattice constant

Figure 10: Bandgap energy of group IV, III-V and II-VI materials [1]

Figure 10 shows that only a handful of materials have bandgap energies that correspond to the chosen wavelengths, and most of them are compound semiconductor alloys. Composition alloy of InGaAs has become the material of choice to fabricate photodetectors with high speed and responsivity. InGaAs span a region of bandgap

energies from about 1.4eV to 0.25eV. $In_{0.53}Ga_{0.47}As$ with 53% indium was chosen for its high absorption coefficient and the correct lattice constant match to InP substrate.

High absorption coefficient will result in high quantum efficiency and responsivity, according to Equations 2 and 3. InGaAs is also a direct bandgap material, efficient at generating photocarriers. It also has very high electron and hole mobility, which is ideal for very high-speed operations. $In_{0.53}Ga_{0.47}As$ films were grown on InP for lattice matching. The semi-insulating property of InP also allows easy device isolation and lowers parasitic capacitance. In fact, $In_{0.53}Ga_{0.47}As$ based on InP substrates material system not only supports photodetectors in today's fiber-optic receiver, but also lasers and modulators in the transmitter as well. Table 1 summarizes some key properties for a number of semiconductor materials.

	electron mobility (cm^2/V-s)	Eg (eV)	Lattice parameter (A)
Si	1350	1.11	5.43
Ge	3900	0.67	5.65
GaAs	8500	1.43	5.65
InP	5400	1.34	5.87
$In_{0.53}Ga_{0.47}As$	11030	0.73	5.87

Table 1. Materials properties summary

TIA and other Electronics

The TIA and other circuitries in the receiver are electronics. These circuits need to operate at the same speed as the photodiode while not introducing much extra noise to the receiver. InGaAs is not only an excellent material for making optically active devices, but fast electronic circuits as well. The high carrier mobility has enabled record high-speed transistors to be made from it. High electron mobility transistor (HEMT) made with InGaAs on InP produced a record cut-off frequency of 562GHz, the highest of any transistor type [8]. Operating circuits made from InP HEMTs now operate at W-band, 75-200GHz [9,10].

Limitations of Current Technology

Though current receiver technology has provided the performance needed by the fiber-optic network, it faces many challenges as optical communication is attempting to penetrate new market and applications. One of the most severe limitations of current receiver technology comes from hybrid assembly. Receiver performance is compromised by the parasitics associated with interconnecting of chips, resulting in lower receiver bandwidth, responsivity and reproducibility. A more severe limitation of hybrid assembly is cost. The pick-and-place assembly and active optical alignment method are highly manual and serial processes and are therefore low in throughput. About 75% of the cost of a current receiver module comes not from the cost of components, but assembly and packaging [7]. Hybrid assembly has worked so far for the fiber-optic industry by taking advantage of the low labor cost in developing countries. But as we will see more clearly later, future growth of optical communication is highly dependent on the receiver's ability to increase functionality. Hybrid assembly will be more and more inadequate as performance demand is increased and cost per functionality is decreased.

There are two general approaches to reduce cost, one is through integration and the other is through better manufacturing. "Integration" in this thesis means monolithic integration, not including techniques such as silicon-optical-bench. Monolithic integration of the optical and electrical components in the receiver can increase performance and reduce cost. Wire bonds will be replaced by on-chip transmission lines, which can lower circuit parasitic reactances, enable higher speed operations, enhance reproducibility and reliability. An integrated chip at assembly will decrease the number of packaging steps, which will increase throughput and decrease labor cost. As future optical receivers are expected to become more complex, the cost advantage of an integrated approach will become more significant. For example, wavelength division multiplexing (WDM) system architecture is currently being used to increase receiver bandwidth. In WDM, different wavelengths of light are combined and send down one fiber. In the case of Dense WDM, up to 100 wavelengths are multiplexed together. An optical receiver will need 100 photodetectors paired with 100 TIAs and plus all the other additional circuitries. Current WDM is being implemented in hybrid configuration.

Integrating all these components monolithically will bring module compactness, packaging simplicity and significant cost reduction at assembly. Figure 11 shows the vision of monolithic integration, for both receiver and transmitter.

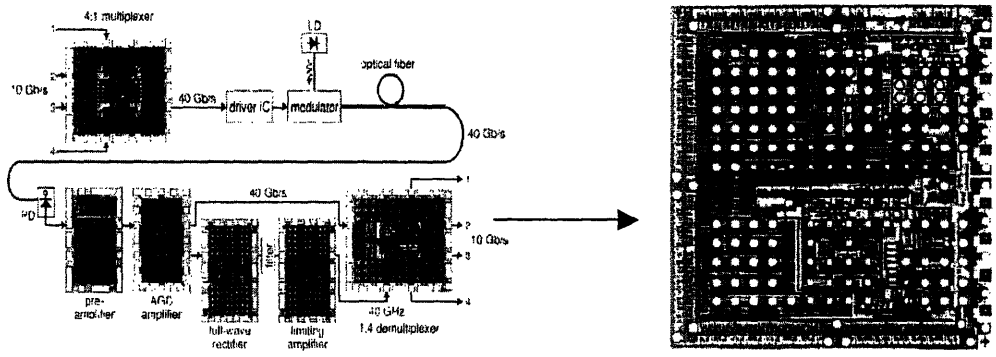


Figure 11: Vision of monolithic integration of a transceiver [11]

In the 1940's when transistors were first invented, simple electronic circuits were made by wire bonding the transistors together. But since then, integrated circuits fabricated by batch-scale wafer processing has revolutionized electronics and opened up new applications that utilized the functionality, cost and size of integrated circuits. Today's optical systems are reminiscent of those old electronic systems we now see in the museum. Many expect monolithic integration to take optical systems down the same path of electronic integration, creating new applications and market through increase in functionality and reduction in size and cost. With the many potential performance and cost benefits of monolithic integration, why hasn't it happened yet?

One reason is the technological challenges of opto-electronic integration, because it usually involves integrating two dissimilar devices, as shown in the monolithic integration of photodiode with field effect transistor in Figure 12. .

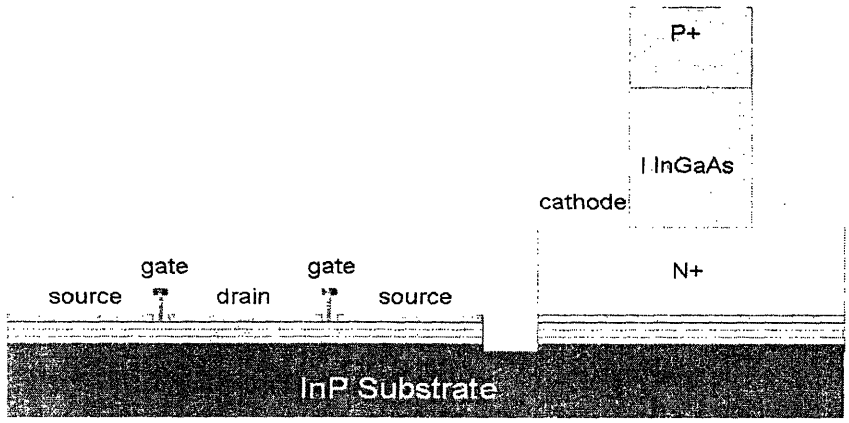


Figure12: Schematic of integrated receiver

Integration involves the stacking two dissimilar material stacks, and this needs new material growth and fabrication techniques. Integration of lasers and modulators in the transmitter is even more challenging, often involving complicated design, growth and processing. In contrast, integration in electronic CMOS technology is really a matter of packing more and more transistors into a given area. All transistors are based on the same material and made in the same way. In comparison to CMOS integration, significant material and process development are involved in opto-electronic integration.

But technological challenges certainly cannot be the only reason for the lack of integration in today's opto-electronic circuits. A literature search shows reports of integrated receivers, beginning from the 1980's. Monolithic integration of PIN photodiode with InP MISFET operating at 400Mb/s was demonstrated in 1988 [12]. Bell laboratories, a pioneer of much optical device and OEIC work, reported a 20Gb/s OEIC in 1995 [12,13]. Another obstacle to monolithic integration is the manufacturing challenge on InP substrate. InP had always lagged behind other semiconductor substrates such as GaAs and Si in terms of substrate cost, available wafer size and manufacturability. In early development phase in the 1980's, InP substrates were available in only 50mm diameters and moved up to 75mm wafer sizes in the 1990's. InP is also a more brittle material than GaAs or Si. The cost of making large dies on small and expensive substrates is very high, especially with high wafer breakage and low yield.

So traditionally, only optically active components and very high performance circuits were made on InP, where the InGaAs/InP material system must be used to deliver the needed performance. For TIAs and other receiver electronics, where current speed requirements have yet to necessitate the use of InGaAs/InP materials system, lower cost solutions have been found on GaAs or Si substrates.

To reduce cost, InP industry certainly has made a lot of efforts to improve the manufacturability of InP by moving to larger wafer sizes and increasing yield. Current state-of-the-art InP manufacturing facilities are using 100mm wafers, and 150mm InP wafers are beginning to be offered by suppliers for sampling [14]. But as InP wafers move to larger diameters, wafer breakage will become a bigger concern. InGaAs/InP is still an attractive system with the gift that combines optical functionality and record high bandwidth, especially as future receivers are expected to have greater bandwidth. Research efforts have focused on making monolithically integrated photonic circuits on InP, which will be discussed in more detail in Chapter IV.

Increase in functionality and reduction in cost for optical receivers is expected for future optical communication systems. These improvements for receivers are expected to come from better component manufacturing and monolithic integration. Chapter III will attempt to show that future market growth for optical communication will be very heavily dependent on the ability of receivers (and transmitters) to reduce cost. Chapter IV, V and VI will discuss some current research endeavors to meet the future market and application demands of optical receivers, including monolithic integration efforts on InP and two new materials system with the potential to increase manufacturability and create integrated photonic circuits.

III. Applications and Market

High bandwidth-distance product is the most prominent advantage of optical communication and one that long-haul voice and data communication has been able to exploit to reach commercial success. But optical links also offers a number of other advantages over conventional metallic or radio communication links. There are specialized markets that take advantage of these advantages of optical communication, and will be discussed below.

Specialized Applications

One other major advantage with light communication is the absence of electromagnetic interference. In electronic systems, wires can produce inductance and act like little antennas that pick up any electromagnetic fields that are present. These electromagnetic interference (EMI), coming from stray fields from adjacent wires or radio waves in the surrounding environment, can interfere with the normal operation of the electronics. Sometimes these EMI are purposely created by a hostile party to disrupt system operation, as in the case of military aircraft and combat communication system. In order for these systems to continue normal operation in the presence of EMI, wires shielding can be used such as in coaxial cables. However, shielding adds weight and cost and produces parasitic capacitance that limits bandwidth. The optical link is immune from most forms of EMI, since there is no metallic wire present. Although there are electronics in the receiver module, the module is usually packaged in a metallic housing which would shield it from EMI.

Fiber cables have diameters hundreds of times smaller than that of a coaxial cable, thus resulting in volume and weight. Figure 13 shows that two optical fiber is capable of carrying the same amount of information as the hundreds of metallic wires.

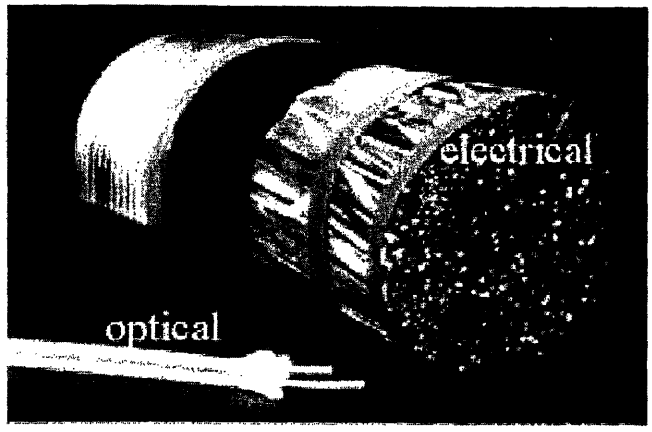


Figure 13: Electrical and optical connection that has the same information carrying capacity. [1]

The use of optical links instead of metallic links for high-speed connections can provide a tremendous reduction in weight and volume. For example, aircraft fuel consumption depends strongly on weight. A decrease of several hundred pounds in the total weight can mean thousands of dollars worth of fuel saved over the lifetime of the aircraft [2].

Optical communication can be used to build more secure communication links, which are important for military and other high security applications. Optical fibers provide more immunity from tapping or monitoring than do wires or radio links. In order to tap a signal from an optical fiber waveguide, one must somehow piece the light-confining cladding of the fiber. This is very difficult to do without disrupting the light-wave transmission within the fiber to an extent which can be detected. Optical fibers do not allow flow of electrical current, so that electrical short circuits can not occur. Since no spark is created when an optical fiber breaks, these fibers can also be used advantageously in combustible or even explosive environments.

Most of the optical links described so far are fibered links. There is also free-space optical communication under development that can be used for target guidance and satellite communication. Optical communication indeed has many advantages over conventional communication methods that make them suitable for many specialized applications. Despite the telecomm bubble burst in 2000 and the drop in corporate

funding for high speed fiber-optic components development, much efforts still remain and are supported by government funding.

Commercial Applications

Although optical communication will be able to carve out niche markets with their special advantages, there will not be significant growth unless the technology is able to capture commercial markets. During the boom of telecom and datacom in the 1990s, there was large growth in fiber-optics through link deployment and network equipment consumption. But the over-optimism of future growth has left an over capacity in network communication which became apparent at 2000 with the burst of the bubble. Future optical communication growth will continue to depend on the telecommunication and data communication market. Figure 14 shows that in the last ten years, voice communication has grown at a modest pace. Data communication, however, has enjoyed an almost exponential growth and many predicted that it would continue to do so.

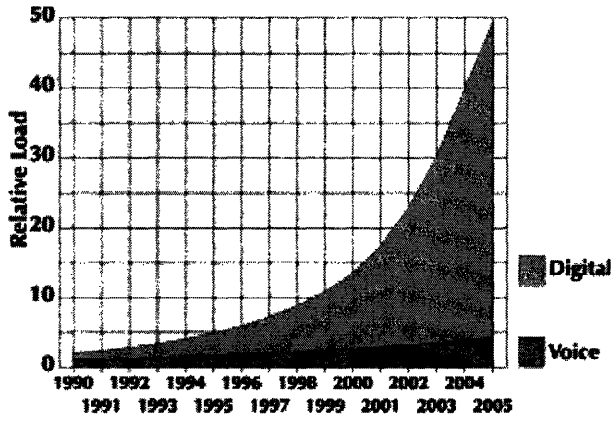


Figure 14: Transmission Capacity over the years. [19]

Data communication includes everything from Internet usage to ATM transactions, and new applications such as video teleconferencing and distance learning. Although the first long distance fiber-optic link was to carry telephone calls from St. Louis to Chicago, future market growth in optical communication will not likely come from voice communication market.

The growth in data communication is likely to come from more people signing up for Internet and more bandwidth requirement from existing users. As of 2002, nearly half a billion people have Internet access and use it regularly. The proportion of population using the Internet will increase, as a whole new generation is now growing up under the influence of The Internet. At the same time, current Internet users are also expected to demand more bandwidth. A survey finds that now about half US Internet users, which are 63 million people, have broadband service either at home or at work. With broadband services such as DSL or cable modem, available bandwidth can range from 2-10 Mb/sec, depending on the location of the user. This certainly allows the user to surf webpages at much greater speed than the 56K modem. But to download a 7.8Gb file, which is about the average size of a movie, current broadband service will still take about two hours.

Many service providers have envisioned new applications for home users that require much greater bandwidth than current broadband service can provide. Some of these applications are closer to reality than others. Interactive video networks will allow high quality video conferencing at home, these can be used for productive purposes or just to keep in touch with friends and family members. Digital home will combine all the audio (phone), video (TV an cable) and PC (Internet) connections to the home into one information pipeline. Thus, an entertainment center in the livingroom may provide all the functions of telephone calls, teleconferencing, cable channels, TV, plus Internet and other productive computer functions. Movie-on-demand will allow the "purchase" of a movie right at home. With Gigabit Ethernet, a 7.8GB file will take about 1 minute to download. There are also applications such as interactive banking and interactive distance learning, all helping people to be better connected and more productive.

Besides home and residential areas, larger bandwidth demand is also expected to come from corporations, universities and other organizations. Faster links are needed between buildings and even within buildings. Connection in storage and server area networks for are expected to rise to 40Gb/s and 1Tb/s . The board-to-board and rack-to-rack connections in network routers are also expected to increase as overall network bandwidth is increased.

Future technology and applications certainly point in the direction of more and even significant bandwidth demand, but does an increase in overall bandwidth capacity necessarily translate into growth for optical communication?

Current network communication consists of backbone network, the regional networks, metropolitan networks and local access network, as shown in Figure 15.

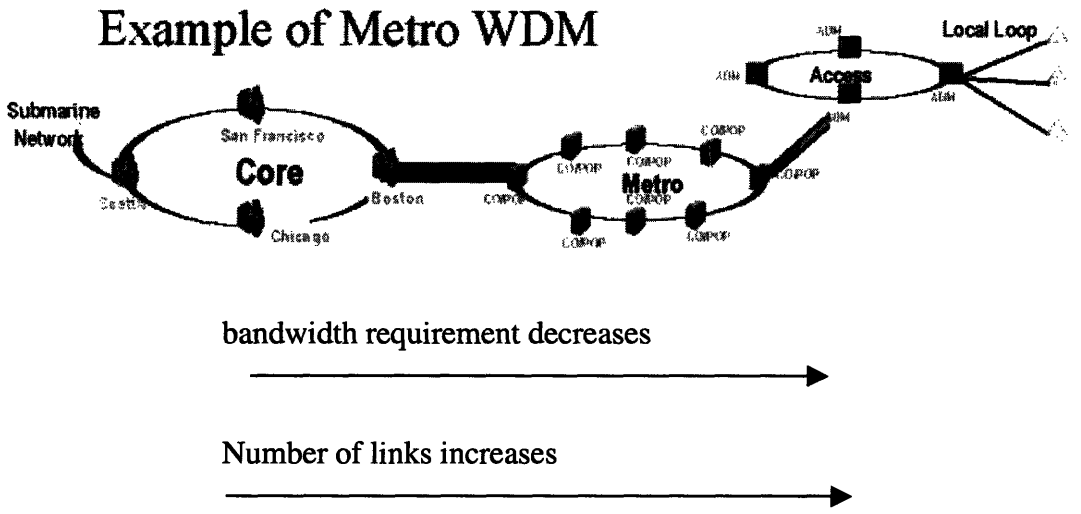


Figure 15: Schematic of optical communication network [1]

The submarine network and connections between large cities are called core or backbone networks. Current backbone networks are using 10Gb/s optical connection, and next generation connections are expected to operate at 40Gb/s. The metropolitan area networks (MAN) use either fiber or copper links, depending on the bandwidth and distance requirements. Optical links are currently providing > 1Gb/s connections to distance greater than 100 meters. Connections in local access loop (LAN) and to the end user, are still largely copper cables. The bandwidth a user enjoys is limited by the connection to the door, no matter how fast information are flowing in the backbone networks.

Fiber-optic will enjoy tremendous growth if it can be used to provide end users with greater bandwidth through deployment in the capillary areas, such as local area networks and home connections. While the backbone will continue to use optical connections for its high bandwidth-distance product, only a limited number of backbone connections are needed. But in this area of capillary links, optical links face stiff

competition from other technologies, such as copper or even wireless links. Since the needed bandwidth-distance product in shorter links is lower, optical links will need to compete on the basis of cost. In general, an average household is not likely to want to spend more than $150-$200 dollars a month for all its communication and entertainment needs. Current households spend about $50 for cable services, $50 for Internet and about $50 for telephone and wireless phones. For example, Gigabit Ethernet is currently being deployed in some local access networks. As the next graph from RHK shows (Figure 16), though optical links initially dominated GEthernet, copper links have succeeded in penetrating more of LAN than optical GbEthernet links.

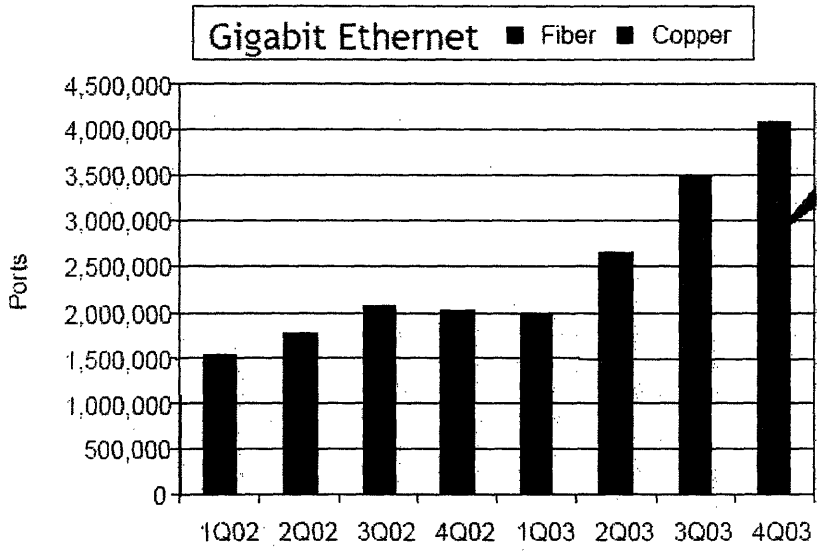


Figure 16: Comparison of Gigabit Ethernets optical and copper ports (©RHK) [16]

Therefore large growth of future optical communication will rely on the ability of optical link to reduce cost and bring its superior performance closer to the user level. Since as the links are getting shorter, there will be less fiber and a majority of the link cost will come from the transmitters and receivers. So the ability to reduce cost in receivers is crucial in enabling growth in future optical communication network.

Optics in Computing

There is an exciting and new area for optics that has less to do with communication but more with computing. This is a market with huge potentials. Current computation speed are limited by the bus speed that connect between circuit boards or chips on board. For example, while microprocessors are already available in 2 GHz, the bus speed that connect the processor and memory is only 900MHz. Optical link inside computer can help to increase computing speed.

Optical connections are envisioned even on-chip as well. Current Si IC industry is facing what many are called the "interconnect bottleneck". For gate length shorter than 200nm, a situation is reached where the delay is no longer dictated by the gate switching time but by the wiring delay. With 500 million transistors in one microprocessor, today's chips have a total interconnection length per unit area of the chip of some 5km/cm2 with a chip area of 450mm^2. In ten years from now these lengths will be expected to be 20km/cm2 for a chip area of 800mm^2 [17]. Vertical interconnect stacking has already reached 6 levels, and increasing the level of stacking is making issues such as resistance-capacitive coupling, signal latency and signal cross-talk more and more severe. Finally, as density of metal lines and transistors continue to increase, there is the problem of power consumption and heat dissipation through all the metallic wires. Many IC producers are beginning to looking at using optical interconnects to route signals on a chip, beginning with the routing of bus signals that travels the longest distance on the chip. Figure 17 depicts how optical connections can be used between boards in a computer, within the board and even an IC chip.

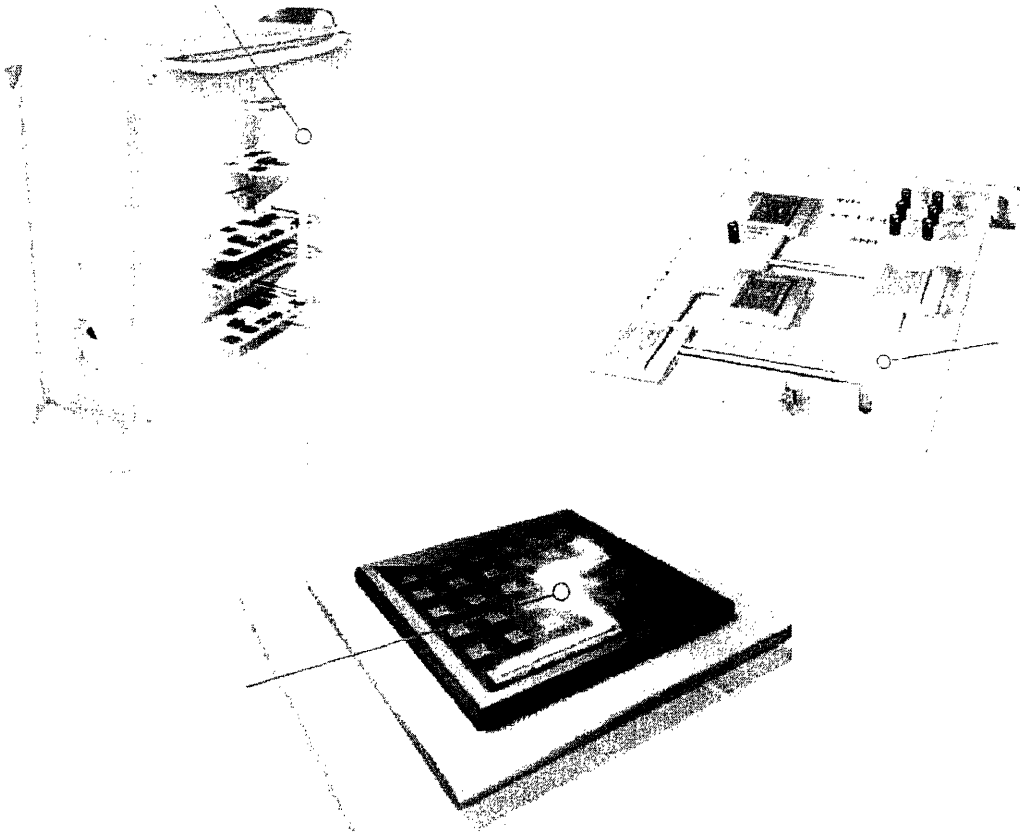


Figure 17: Optical interconnects [20]

Again, the trend is that future optical links will get shorter and shorter, disappearing even into our electronics. These applications will require optical connection to dramatically reduce in size and cost. Optical receivers cannot remain the same size of an IC chip, as they are today or even bigger. Receivers cannot cost hundreds to thousands of dollars for these applications, as they have been in optical backbone networks. There will be more receiving and transmitting component consumption, but less fiber will be involved. On-chip optical connections will use waveguides instead of optical fiber.

In conclusion, in order for there to be significant growth in optical technology, it needs to capture the bottom of the communication pyramid where the number of links are larger and the link distances are shorter. The ability of optical receivers to reduce cost and size (functionality/area) is crucial. The following three sections will look at how the

industry is attempting reduce cost and functionality/area through integration, better manufacturing and cheaper materials.

IV. Monolithic Integration On InP Material System

InGaAs on InP is the current material of choice for optical communication. Small-scale integration on InP generally integrates a photodiode and a TIA. OEICs that integrate single PIN diodes with InP HEMT or InP HBT amplifier has reached past 40Gb/sec operations [8]. Larger scale integrated photonic circuits will have many more components. For example, in wavelength division multiplexing (WDM), one will need:

- Photodetectors
- TIAs
- Other amplifiers
- Filters
- demultiplexing circuitry

For each wavelength, one will need a set of photodetectors, amplifiers, filters and clock and signal reshape circuitry. Monolithic integration can combine all these components in the receiver module unto a chip and thus significantly reduce receiver size and simplify assembly process. A schematic of such a system is shown in Figure 18.

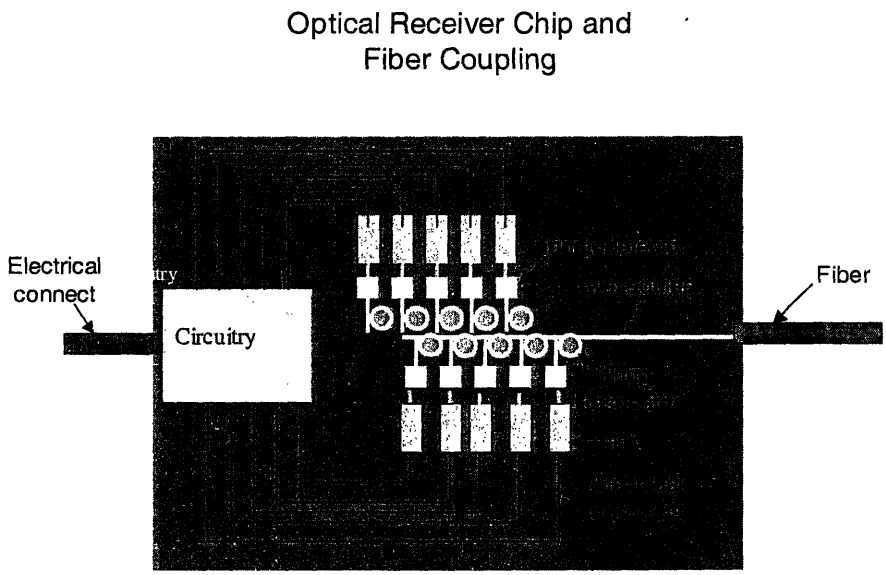


Figure 18. Schematic of future optical receiver.

The realization of large-scale integrated photonic circuit will require a few key technical achievements. One is the ability to grow and process the optical and electrical devices monolithically on the same chip. This has been demonstrated in the photodiode integration with TIA as mentioned above [19]. A second challenge is to efficiently couple light between optical devices and from fiber to detector. This requires low loss on-chip waveguides, efficient waveguide-to-device and waveguide-to-fiber coupling. Following sections will discuss each one of these aspects in some detail. For more thorough understanding, refer to Electromagnetic Principles of Integrated Optics by Donald L. Lee

Waveguides

Semiconductor waveguides are like "wires" that route optical signals between optical devices on a chip. In index-guiding waveguide, a high index-of-refraction core is surrounded by a low-index cladding. Light is guided by total internal reflection much like in a fiber waveguide. On InP substrates, low-loss waveguides core is usually InGaAsP, which can have index ranging from 3.17 to 3.45 with different alloy compositions. The core can either be clad with InP (index of 3.17) or can simply by air (index of 1). There is a variety of different waveguide geometry: rib, ridge, channel, buried rib.... Figure 19 shows some common waveguide geometries.

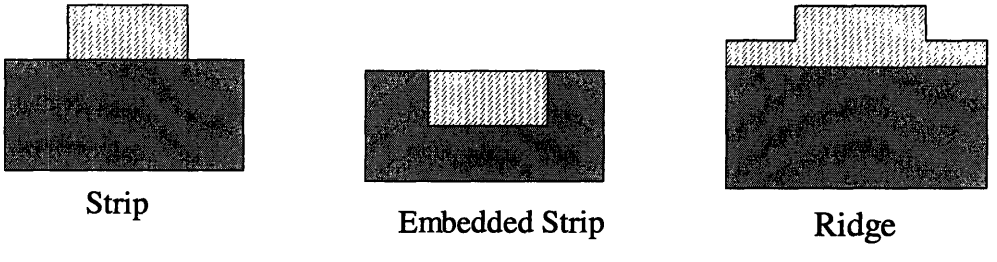


Figure 19. Some simple waveguide geometries

Vertical confinement is generally achieved through different refractive index and lateral confinement through effective refractive index. Waveguide index contrast is calculated through:

$$IndexContrast = \frac{n_1^2 - n_2^2}{2n_1^2} \qquad \text{with } n_1 > n_2 \qquad (7)$$

High-index-contrast (index difference between core and cladding) waveguide will generally have smaller dimensions and provide better light confinement. Waveguide propagation loss, usually termed α, measures the attenuation of optical power in dB/cm. Large propagation loss reduces maximum transmission length, and therefore places more stringent power requirements at the source and detector. There are three dominant loss mechanisms: material absorption, scattering and leakage.

Waveguide materials are chosen to be essentially transparent at the wavelength of propagation (InGaAsP is transparent at 1330nm and 1550nm). However, some photons are still absorbed due to residual band edge absorption. Absorption can also be induced by free carries. The initial achievement of high transparency waveguide material was primarily a result of improved material growth technique that reduced residual carrier concentration [20]. Scattering results from rough interfaces at the epitaxial layer boundaries and etched waveguide surfaces. 4nm of epilayer roughness can result in loss as high as 0.5dB/cm at 1550nm wavelength in a typical waveguide structure [20]. Leakage of guided light occurs when the refractive index of substrate or another epilayer is the same or greater, since the high index substrate essentially acts as an optical absorber. This situation exists for the GaAs-AlGaAs waveguide system.

Above are dominant loss mechanisms for a straight waveguide. When there is curvature present in a waveguide, the loss through radiation can become dominant. This comes from the phase velocity difference of the light at the edge of the bend and the center of the bend. This distributed radiation loss, measured in dB/cm or dB/degree, depends exponentially on the radius of curvature. In integrated photonic circuit, small waveguide bending radius is important to achieve small die size. Generally, the larger the refractive index difference between core and the cladding, the smaller the bending loss

and bending radius. With index contrast of 0.27, 4μm radius bend has been achieved [2, p87]. But there is a trade-off here since scattering loss will become more sensitive to surface roughness as index contrast is increased.

In the early days when III-V materials were grown mostly by liquid phase epitaxy, the resultant rough waveguide interfaces usually had propagation losses > 5dB/cm. This is too high for efficient on-chip optical power transfer. With the use of organo-metallic chemical vapor deposition (MOCVD) and molecular beam epitaxy (MBE), material quality has greatly improved. In 1989, there were several reports of single-mode guides on InP with 0.5dB/cm loss [21]. Current low-loss III-V waveguides have loss less than 0.2dB/cm, which is sufficient for integrated photonic circuits [22].

Waveguide-Detector Coupling

The figure of merit for waveguide-detector coupling is coupling efficiency, which can be expressed as the fraction of total power in the optical beam coupled into the detector or as a coupling loss in dB. While conventional detectors are often top or bottom illuminated, detectors integrated with waveguides are usually illuminated from the edge. This coupling approach allows optical absorption path to be independent of the carrier transit length and so they can be optimized independently. The absorber in the detector has higher refraction index than the waveguide core in order to absorb optical energy. Edge illumination can be done in butt-couple or vertical-couple fashion. In butt-coupling, the waveguide ends at the interface with the optical absorber and thus light is end-fired into the absorber, as illustrated Figure 20.

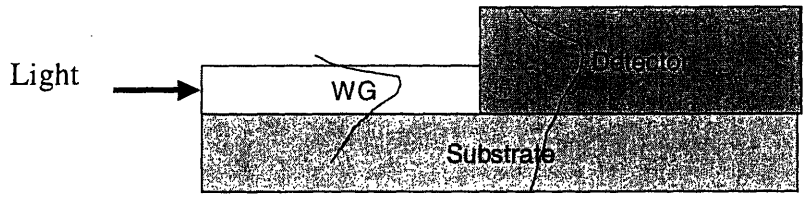


Figure 20: Schematic of butt-coupled photodetector with waveguide

This structure offers fabrication flexibility (i.e. electrode placements) and a short device length (limited only by material absorption a) which allows low capacitance and high bandwidth. Devices with internal quantum efficiency greater than 70% have been

realized with detector lengths as short as 10-15μm [21]. The small dimensions have led to bandwidths of 20GHz and may soon exceed 50GHz. Internal quantum efficiency calculated from measurements is about 98% [23]. The major disadvantage with butt-coupling is its fabrication complexity. It requires material re-growth and has stringent vertical and lateral waveguide-to-detector alignment requirements. Studies showed that 1μm lateral misalignment could limit bandwidth to less than 3GHz [21]. Material re-growth can usually result in poor interface that compromised film quality and lead to high leakage currents and low diode breakdown voltage.

Another waveguide-detector coupling approach is vertical or evanescent coupling. The waveguide runs the length of the absorber and light is evanescently coupled into the absorber layer, as shown in the Figure 21.

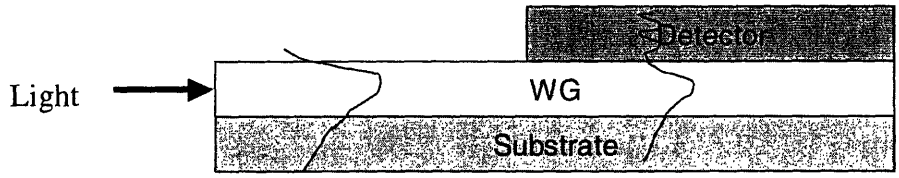


Figure 21. Schematic of Evanescent or Vertical Coupling for waveguide and detector

The vertically coupling approach has the advantage of simpler fabrication process but presents a trade-off between RC-limited bandwidth and responsivity. This technique requires no material re-growth and therefore no vertical alignment. The tolerance of lateral guide-to-detector alignment is also relaxed. Since the coupling efficiency is lower due to reflection at the waveguide-absorber interface, detector length is increased to maximize optical absorption. For single-mode coupling, the photodetector is usually a few hundred micrometers long. This increase in dimensions introduces higher capacitance that decreases detector bandwidth. Various techniques have been proposed to improve the weak vertical field coupling. For example, an impedance matching layer can be exerted between the core and the absorber. This layer has an index of refraction intermediate between that of the waveguide core and the absorber. The refractive index

and the thickness of the impedance matching layer are optimized to minimize light reflection from the absorber back into the waveguide. MetroPhotonics in 2003 reported 1.1A/W for single-mode coupling of waveguide with detector, by assuming a 2.7dB coupling loss at the fiber-waveguide interface [24]. Bandwidth, however, has so far been limited to just a few GHz due to large detector size. The coupling efficiency is higher for multimode coupling. 45 GHz integrated waveguide-detector has been reported, with internal quantum efficiency of 90% [33].

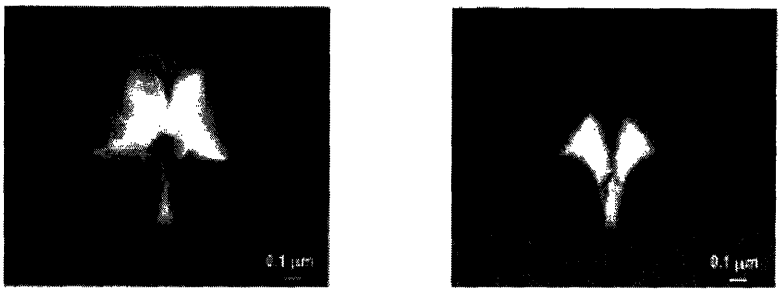
In both coupling mechanisms, large modal mismatch and reflection at detector-waveguide interface are concerns. Optical directional coupler in the form of waveguide or detector taper can be used for modal matching and minimize reflection and scattering.

Fiber-waveguide Coupling

On-chip waveguides generally have radius in the orders of a few micrometer, to facilitate single-mode propagation. This also keeps the mode size to less than 3μm, which improves the performance of on-chip optical components. The disadvantage is a large modal mismatch in coupling to a fiber that typically has a mode diameter of 6-10μm [21]. A good coupling technique should allow efficient coupling and large fiber-to-waveguide alignment tolerances. The modes are mismatched in terms of both size and shape, and mode size converters are generally employed to achieve efficient coupling. Monolithically integrated mode size converters are generally a taper at the waveguide. A number of different taper design are summarized by Moerman *et. al* in an article published in 1997 [25].

Integration with other electronic circuitry

Integrated photonic circuitry will likely have large electronic circuitry on them to handle the large information processing needs. This calls for large-scale electronic integration based on InP substrates. We have discussed some manufacturing drawbacks of InP substrates but significant improvements have been made through better processing and larger wafer size (currently 150mm diameter wafer). Making the transistor gate is generally the yield-limiting step in InP HEMTs, since gate length is the minimum feature on the circuit (0.25μm to 0.1μm). Fujitsu introduced a Y-shaped gate that has lower stem-to-top aspect ratio than conventional T-gate (shown in Figure 22), which helps to reduce cracking between the top and the stem [26].



(a) (b)

Figure 22: (a) Cross-section of conventional T-gate (©Fujitsu) (b). Cross-section of Y-gate (©Fujitsu)

Selective gate etching has also become increasingly popular since it improves device uniformity across the safer in comparison to timed gate etching. A standard deviation of 0.13mV across 75mm wafer is reported for gate threshold, which is –0.633V [26]. With new gate topology and selective etching, reported gate yield is greater than 99.9%, which is suitable for fabricating ICs with a thousand transistors count. Fujitsu fabricated InP ICs with 1000 transistors and operating at 40Gbit/s, as well as 2:1 multiplexer that has over 200 transistors and operating at 90Gb/sec [26].

Heavy research has been invested to overcome the technological challenges of creating integrated photonic circuit on InP and has produced promising results. Low-loss waveguides that are sufficient for integrated photonic circuit have been demonstrated. Waveguide-detector and waveguide-fiber coupling have made significant improvements. Improved InP manufacturing technology has also increased the scale of integration on InP. In all the development of monolithic integration, one must remember that the goal of integration is not only to increase performance but to reduce cost as well. Integration should not bring with it too much processing complexity, therefore loosing the cost advantage that integration should bring.

Although InP manufacturing technology has made progress, it still lags behind two other popular semiconductor substrates, GaAs and Si. Since one of the main goals of integration is to reduce cost, many have investigated the possibility of manufacturing receivers using these cheaper and more manufacturable material systems. Next two

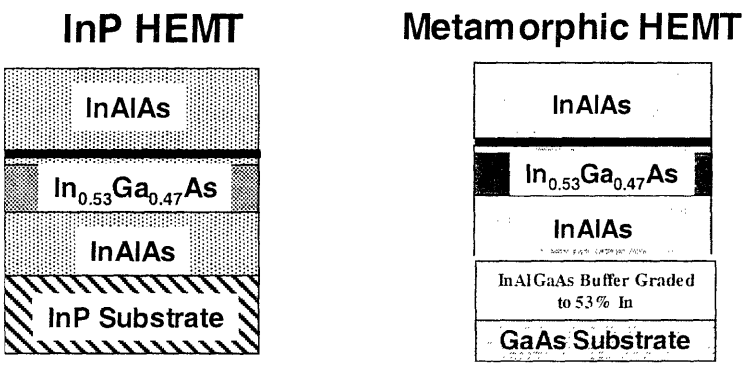
Chapters will look at their technical achievements and their potentials are at realizing integrated receivers.

V. Metamorphic GaAs Technology

Metamorphic GaAs HEMT

This section introduces an alternative material system for high performance opto-electronic circuits, gallium arsenide (GaAs). GaAs has been another technology of choice for many RF applications such as power amplifiers for cell phones and radars. Thin film of InGaAs, up to about 20% indium, can be grown on GaAs under strain. The strain of 2.4% lattice mismatch between $In_{0.2}Ga_{0.8}As$ (5.73A) and GaAs (5.87A) can be elastically accommodated. GaAs's semi-insulating property allows easy device isolation and lowers parasitic capacitance, which are important for high speed operations greater than 1GHz. High electron mobility transistors made with such material system are termed pseudomorphic HEMT (PHEMT). When film's indium content is greater than 20%, the film becomes highly strained and many dislocations begin to form in order to lower film free energy. This is unfortunate because the optical active layer for 1550nm photodetector is $In_{0.53}Ga_{0.47}As$ with 53% indium. $In_{0.53}Ga_{0.47}As$ also has better carrier mobility than $In_{0.2}Ga_{0.8}As$, which is desirable for high speed digital processing, optical communication and a wide range of microwave amplifiers, as we have discussed in the previous section.

The lattice constant of GaAs is 5.65A, a mismatch of about 4% to that of $In_{0.53}Ga_{0.47}As$ (5.87A). The dislocations formed in a relaxed film can severely limit device performance. In photodiodes, the dislocations can lower responsivity by trapping the electron-hole pair produced. They can increase the noise of the photodiode by providing a conductive path for leakage current to flow. In transistors they can trap carriers, form highly conductive or resistive path. These lead to lower gain and bandwidth. So traditionally, devices that contain InGaAs with > 20% indium content were fabricated on InP (with lattice constant of 5.87) and are called InP HEMTs, as mentioned in previous section and shown in Figure 23a.



(a) (b)

Figure 23: InP HEMT (a) and metamorphic HEMT (b) material structure cross-section.

GaAs is a more attractive manufacturing substrate than InP. GaAs substrates are available in larger sizes and are cheaper than InP. Some state-of-the-art GaAs foundries are already using 150mm wafers. 150mm GaAs substrates cost about $350/wafer and 100mm is $125/wafer, but 100mm InP wafers still cost $1000/wafer. GaAs wafers tend to have less breakage because they are not as brittle as InP. To utilize manufacturing advantage of GaAs, a method is needed to match the lattice constant of GaAs to that of the high-indium content films. This can be done through a metamorphic buffer, as shown in Fig. 23b. The buffer consists of a number of graded alloy layers, and the indium content is ramped up to a desired value through these layers. The choice of alloy has so far included InAlGaAs (Raytheon, UI), InAlAs (TriQuint) and AlGaAsSb (BAE). Threaded dislocations are largely contained in the buffer layer and as a result, high quality $In_{0.53}Ga_{0.47}As$ film can be obtained. The following cross-section micrograph from Raytheon shows the GaAs substrate, the graded buffer layers and the HEMT layers. Dislocations propagate horizontally in the buffer leaving the HEMT layers smooth with few defects.

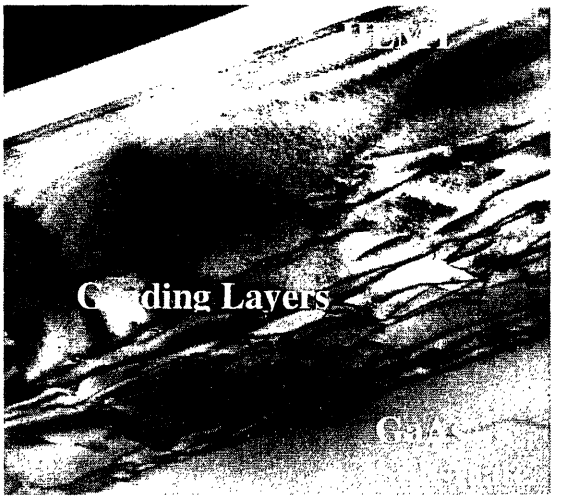


Figure 24: TEM cross-section micrograph of metamorphic HEMT material. [©RRFC, Raytheon]

The development of metamorphic buffer technology was first motivated by efforts to fabricate InP HEMTs on the cheaper GaAs substrates. Although many saw the technology's potential in creating $In_{0.53}Ga_{0.47}As$ photodiodes on GaAs. Research in metamorphic technology in the last ten years has turned potential into reality. The dislocation density of HEMT channel film as measured from TEM cross-section is less than 10^6 /cm^2. Although that is still higher than InP HEMT, which is about 10^3 /cm^2, but good enough for the fabrication of high performance device. Since defect density of 10^6 /cm^2 means the defects are on average 10μm apart from each other, which is much larger than the source-drain spacing (~2-4μm) of the transistor. Hall measurements have shown that the quality of metamorphic HEMT active layers are equivalent to that of InP HEMT, as shown in a comparison in the following table of published material data for InP and metamorphic HEMT over the years. [14, 27, 28, 29]

HEMT latticed matched to InP substrate

Affliation	mobility (cm^2/V sec)	sheet density (10^{12} cm^{-2})	Year
HRL	10,500 - 11,500	2.5 - 3.0	1998
IQE	10,400	2.9	2003

Metamorphic HEMT on GaAs substrate

Affliation	mobility (cm^2/V sec)	sheet density (10^{12} cm^{-2})	Year
Raytheon	10,300	2.85	2002
UI, Urbana Champaign	10,070	2.08	2002

Table 2. Comparisons of Hall data for metamorphic HEMT and InP HEMT

The key electrical characteristics of metamorphic HEMTs today, such gain, noise, and output power, are virtually identical to that of InP HEMTs [14, 29]. These performances further affirm the quality of metamorphic buffer and its high-indium content device layers. Reliability test of metamorphic HEMT low noise amplifiers at Raytheon have shown lifetime of 10^6 hours at room temperature, showing negligible degradation in the buffer over time. Metamorphic HEMT technology has already been introduced into production facilities at Raytheon and WIN semiconductor [30]. Raytheon has patented metamorphic HEMT technology, with patent number 6,489,639.

1.55μm photodetector on Metamorphic GaAs

The success of metamorphic HEMT shows that high quality $In_{0.53}Ga_{0.47}As$ layers can now be grown on GaAs, so long-wavelength PIN diode that were once only possible on InP can now be built on GaAs as well. Growing high quality PIN stack presents a greater challenge than HEMT because a thicker film is needed. The diode will need about 1μm thick active region for high absorption, much thicker than the 30nm thick active HEMT channel layer. This material growth challenge has been overcome at

Raytheon and Illinois University, Urbana Champaign, who are leading the development of metamorphic PIN diodes. Figure 25 shows schematic of metamorphic PIN diode.

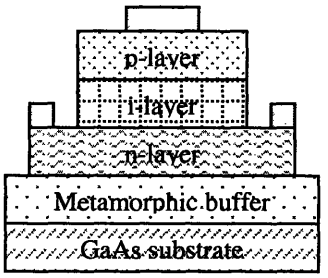


Fig. 25. Schematic of metamorphic PIN diodes

Raytheon has reported metamorphic PIN diodes with bandwidth of 52GHz, responsivity of 0.64A/W and dark current of 10nA at reverse bias of 10V. These diodes are 10μm in diameter and responsivity was obtained from top illumination. Jang *et. al* from Illinois University has also reported metamorphic PIN diodes with 38GHz bandwidth, 0.7A/W responsivity. For both, InGaAlAs buffer alloy was used and material growth were accomplished with molecular beam epitaxy (MBE). These results are comparable to InP photodiodes that are currently being used in industry.

Raytheon reported the monolithic integration of PIN diode with a TWA, all on a metamorphic GaAs substrate. This OEIC has a bandwidth of 40Ghz and a responsivity of 210V/W into a 50Ω system. The responsivity over frequency plots of five devices in Figure 26 show very little variations.

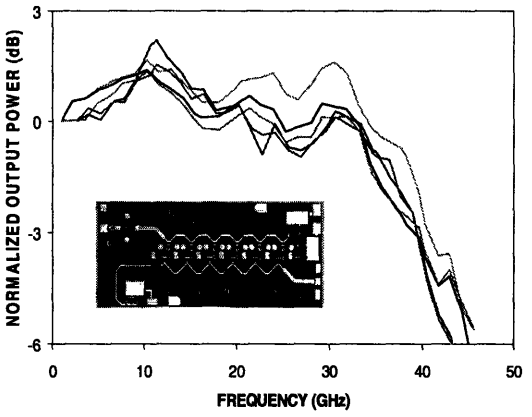


Fig. 26. Frequency response of metamorphic OEIC [©RRFC, Raytheon]

The monolithically integrated receiver shows 8GHz wider bandwidth and 7dB more gain in comparison to a hybrid photoreceiver [29]. Metamorphic OEIC have also been demonstrated at University of Illinois, with 0.53A/W responsivity for photodiode and 140GHz cut-off frequency for the metamorphic HEMT TIA [28].

With metamorphic buffer, GaAs substrate is essentially "transformed" into InP substrate, therefore combining the performance advantages of InP with the higher manufacturability of GaAs. Although long-wavelength photodetector and small-scale OEIC have been realized on GaAs, reports of waveguide integration with photodetector at 1550nm have been very limited. The use of InGaAsP/InP waveguide system is possible on metamorphic GaAs substrate, as shown in Figure 27, but no results has yet been reported.

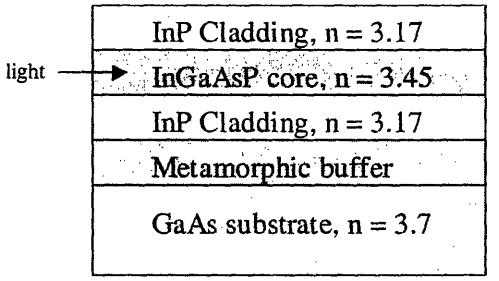


Figure 27: Cross-section view of InGaAsP/InP waveguide on Metamorphic GaAs substrate

With appropriate alloy compositions for InGaAsP, index contrast for InGaAsP/InP waveguide can be as high as 0.1. Such high index contrast provides enough modal confinement with a small evanescent tail that extends into the cladding. So InP cladding layer thickness can be in the order of a few micrometers to prevent light leakage into the high-index GaAs substrate (n = 3.7).

Traditional GaAs/AlGaAs waveguide system on GaAs was developed for light guidance at 850nm. Although GaAs/AlGaAs waveguides can be used at 1550nm, propagation loss is relatively high at 0.45dB/cm. (29) Waveguide-detector coupling is very poor due to large reflections at the interface, as shown in Figure 28

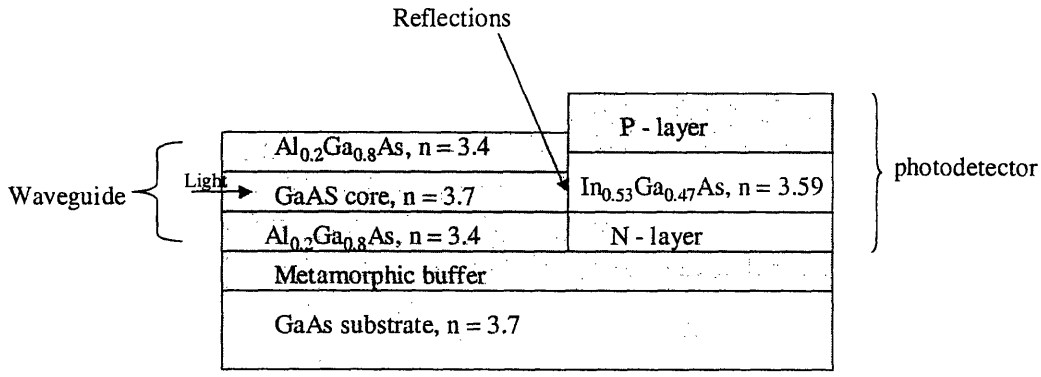


Figure 28: GaAs/$Al_{0.2}Ga_{0.8}As$ waveguide coupling to $In_{0.53}Ga_{0.47}As$ Photodetector on Metamorphic GaAs Substrate

To facilitate light absorption from the low-index waveguide to the high-index photodetector layer, University of Maryland reported the use of etched mirrors behind the photodiode, as shown in follow Figure 29.

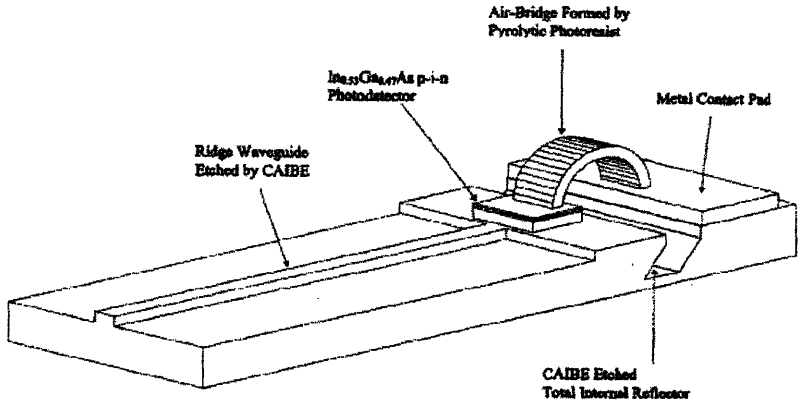


Figure 29: GaAs/AlGaAs waveguides on GaAs substrate integrated with $In_{0.53}Ga_{0.47}As$ photodiode (©University of Maryland)

In this work, $In_{0.53}Ga_{0.47}As$ films were grown on GaAs substrate through InP buffer. The waveguide runs underneath the photodetector, and etched mirror reflects light into the detector's absorption region. The mirrors are etched with chemically

assisted ion beam etching, and a certain tilt angle is achieved by adjusting the wafer orientation with respect to the incident ion beam. Reported external responsivity (including fiber coupling loss) is 0.37A/W and 3-dB bandwidth is 3.6GHz [34].

Materials engineering has enabled GaAs to support high performance electronics and long-wavelength photodetectors that were once only possible on InP. Through metamorphic buffer on GaAs, PIN photodetector, high-indium content amplifiers and small-scale OEICs have all been demonstrated with comparable performance and reliability to that of traditional InP based devices. Metamorphic technology makes it possible to enjoy the superior manufacturability of GaAs and the high performance of InP based devices. Implementations of waveguide integration to form larger scale photonic integrated circuit have so far been limited, largely due to limited market. But this is a very worthwhile area to explore and can significantly draw from the knowledge base of the InGaAsP/InP and GaAs/AlGaAs waveguide systems. Metamorphic GaAs materials system is a strong candidate to reduce receiver cost in the near future, and more research endeavors are needed to realize larger scale photonic integration with waveguides for long-term future.

VI. Silicon Microphotonics

Another material contender in the area of integrated photonics is silicon, the material upon which the $160 billion microelectronics industry is built on. But on the area of photonics and opto-electronics, silicon so far has had very limited market penetration. Its bandgap is 1.1eV, which is ideal for detecting wavelength of 850nm but transparent at 1300nm and 1550nm. It is also an indirect band-gap material and has weak electro-optic effects. Silicon hasn't been able to match compound semiconductors in high-speed electronics due to its intrinsic lower carrier mobility. But silicon enjoys one very important advantage, which is cost and economy-of-scale. The silicon substrates are available in larger sizes and cost less than III-V substrates. 200mm Si substrates cost about $15/wafer and 300mm is $100/wafer. Silicon foundries currently use 200mm wafers and some have upgraded to 300mm. Advanced processing technology and continued development has allowed silicon CMOS devices to achieve performances that many predicted would be impossible for it. The continued shrinking size of silicon transistors has been the key enabler of increase in speed, with 0.13μm line-width in use in silicon foundries. Recently, material engineering such as SiGe alloy and strained silicon technology further advanced the frontiers of speed and complexity of Si ICs [silicon photonics.

The biggest incentive for building opto-electronic integrated circuit on Si is cost reduction. Though fiber-optic communication system is based on light, most of the communication system is made up of electronics. The optical components in a fiber-optic link are basically laser, modulator, detector, optical fiber and some passive optics for filtering or coupling. Since silicon is the dominant material in microelectronics, the ability to monolithically integrate optical function on silicon electronics can potentially reduce cost and compactness. Si photonics is also an attractive solution to the "Interconnect Bottleneck" faced by the IC industry, as discussed in Market Analysis Section.

To realize integrated receiver on Si, the essential components are efficient photodetector, low-loss waveguides and efficient waveguide-detector coupling.

Photodetectors on Si

For detection at 850nm, monolithic integration of 8Gb/s Si photodetector with 130nm CMOS technology have been demonstrated on a SOI wafer [17, p31]. For detection in the 1330-1550nm windows, SiGe or Ge film grown on silicon is used. In 1990, IBM demonstrated the first Si/SiGe integrated rib waveguide-photodetector for long wavelength at 1300nm. The frequency response was 1-2 GHz with 50% quantum efficiency [31].

MIT Microphotonics group has reported Ge photodetectors on Si substrate. As shown in Figure 30, bulk Ge has a direct bandgap of 0.8eV, corresponding to 1550nm. But Ge has a minimum energy bandgap of 0.66eV, which affects the efficiency of Ge photodetector.

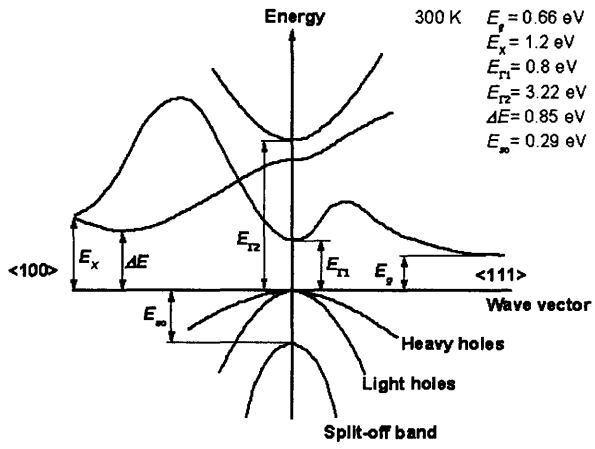


Figure 30: Bandgap diagram of Ge.

Shrinking Ge direct energy bandgap can improve detector efficiency at 1550nm. Professor Kimerling's group at MIT has shown that direct bandgap shrinkage can be accomplished through tensile strain in Ge film. Figure 31 shows that energy gap between the light-hole bands of Ge are reduced under biaxial strain.

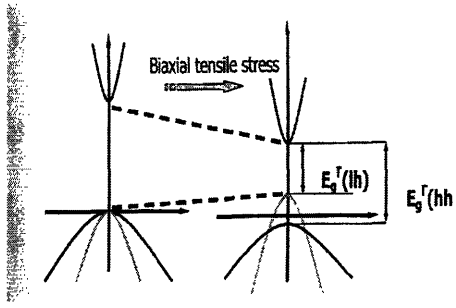


Figure 31: Ge bandgap shrinking under biaxial tensile stress (© Kimerling) [17]

The lattice constant of Ge is 5.65A and Si is 5.43A, about 4% lattice mismatch. When a Ge film of a few atomic layers is grown on Si, a compressive stress is induced in the film. As the film gets thicker, misfit dislocations will generate to accommodate the elastic strain and minimize free energy. When the sample is cooled down to room temperature, film tensile strain dominates because the thermal expansion coefficient of Ge is greater than that of Si. After growth, cyclic annealing is used to remove the dislocations so the film remains largely dislocations free. A tensile strain of 0.19% has been achieved with this method, which leads to direct bandgap of 0.773eV [17, p108]. This extends responsivity region Ge to 1600nm.

High performance photodetectors can be fabricated from properly grown Ge film. Bulk Ge has electron mobility of 3900 cm^2/V-sec and a hole mobility of 1900cm^2/V-sec. The maximum working frequency is calculated to be 25GHz for a Ge detector, with 1μm intrinsic layer thickness and at a reverse bias of 1V. This is, of course, assuming the detector speed is not limited by RC delay. Ge detectors with response time < 200ps have been demonstrated at MIT, corresponding to a bandwidth of 2GHz. Measured responsivities are 0.89A/W and 0.75A/W at 1300nm and 1550nm, respectively. The high responsivity value indicates the quality of germanium layers. With improved device design and fabrication, frequency of 25GHz and extension of responsivity to 1620nm are expected [17, p90].

The growth and fabrication process of Ge detector is compatible with CMOS processing and so can be monolithically integrated with CMOS circuits. CMOS circuits

can be fabricated first on silicon substrate with some marked areas for germanium detector growth. The growth (selective area growth) and fabrication of optical devices are done before metallization. Finally, metal can be deposited to connect all the CMOS and optical devices. Professor Kimerling has a pending patent on germanium photodetector technology: 20030235931.

Si waveguides and coupling

Waveguides on silicon substrate can be made from a variety of materials. Some common ones in use are silicon, silica, silicon nitride or silicon oxynitride. In index-guiding waveguides, the higher index core is usually clad with silicon oxide or simply air. A silicon oxide layer is generally grown on the Si substrate to prevent leakage of optical energy into the high index substrate. High-index contrast waveguides, such as silicon-on-insulator (SOI) with index contrast around 2, are ideal for densely integrated photonic circuits because of their small dimension (can be in sub-micrometer range) and bending radius. Figure 32 shows a schematic cross-section for SOI waveguides.

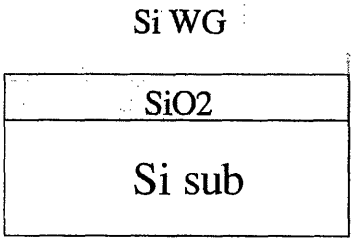


Figure 32: SOI waveguide cross-section schematic.

However, a natural problem that comes with small waveguides is their low coupling efficiency to the fiber. Various techniques have been proposed to solve this problem, such as adiabatic tapers, V-grooves, and grating couplers [17, p20]. In addition, waveguide scattering loss becomes much more sensitive sidewall roughness when high index contrast is increased. The trade-off relationship between scattering loss and bending radius as a relationship of index contrast is shown in Figure 33.

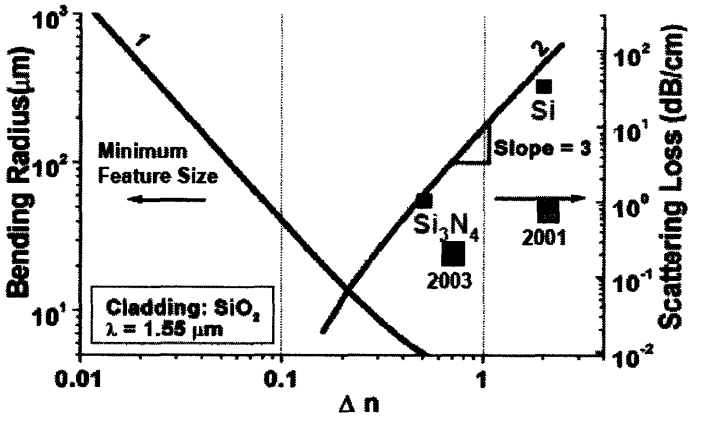


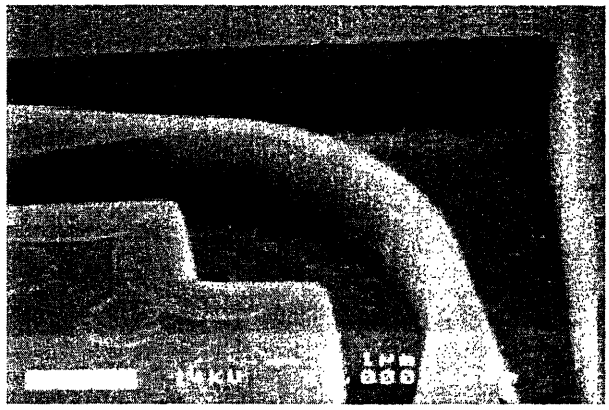
Figure 33: Bending radius and Scattering loss as a function of index contrast, for Si based waveguides (© Kimerling) [17].

Figure 33 shows as Δn approaches 1, the minimum device dimensions falls below 10μm but scattering loss from sidewall roughness becomes a major concern. A data point for fabricated Si waveguides shows scattering loss around 30dB/cm, in close agreement with theoretical predictions (solid line). Therefore, the ability to fabricate waveguides with smooth sidewalls is critical to achieve the acceptable scattering loss of less than 0.1dB/cm for integrated photonic circuit. Possible solutions include dry oxidation, wet chemical etching and laser annealing. Initial work with dry oxidation at MIT has shown the transmission loss in silicon waveguides to be less than 0.2dB/cm. Optical loss as low as 0.1dB/cm at 1.55μm also been reported [17, p30].

For waveguides that have lower index contrast than SOI, silicon nitride and silicon oxynitride can be used. These waveguides generally have an index contrast of between 0.1 and 1, spanning the middle region of Figure 33. With index contrast less that SOI but greater than low-index waveguides, they are promising in creating small dimension and low-loss waveguides on Si. Work at MIT has produced Si_3N_4 waveguides that have optical loss of 1dB/cm and bending radius of 50μm, as shown by the data point in Figure 33.

Low-index contrast waveguides generally have index contrast between 0.001 and 0.1. In silica on silicon waveguides, doping is used to alter the index of the silica core.

These guides have high waveguide-fiber coupling efficiency due to its low modal confinement and therefore larger mode size. But due to their large dimensions (usually about 50μm thick) and large bending radius (usually about 10mm), these guides are not suitable for integrating a large number of optical components on a single chip. Although creative methods have been demonstrated to achieve tight bends on low-index contrast silica-based waveguides. MIT Microphotonics group introduced an air trench at the bend, as illustrated in Figure 34.



Δn=0.1029; n(cladding) = 1.4456, n(core)=1.5485 (at 1.55μm)

Figure 34: Air-trench at bend for low-index-contrast waveguides (©Microphotonics Center, MIT)

Index contrast at the bend is increased by etching away the silicon oxide cladding, shrinking the mode and allows light to pass the bend with less radiation loss. With this air trench, the bending radius of conventional low-index guide is reduced from 10mm to 5-10 μm. This is a significant improvement and increases the potential of low-index guides for densely integrated photonic circuits.

Fast silicon electronics

With suitable detectors and waveguides in place, one remaining question is that whether the speed of Si electronics can meet the demands of future optical receivers. In 1988, the cut-off frequency of silicon and silicon-germanium alloy transistors were about 10GHz [32]. In 2003 cut-off frequency of 130GHz was reported, which would permit operations up to about 45GHz [11]. SiGe HBT with CMOS (SiGe BiCMOS)

technologies have been used to fabricate TIA with 9GHz bandwidth [36]. Hitachi has demonstrated 40Gb/s Si IC chipsets for fiber-optic communication systems, including 4:1 multiplexer, transimpedance preamplifier, automatic gain control amplifier, a limiting amplifier, and a 1:4 demultiplexer [11]. Hitachi also demonstrated a single-chip 10Gb/s transceiver chip (not including optically active elements) with SiGe BiCMOS and it is shown in Figure 35.

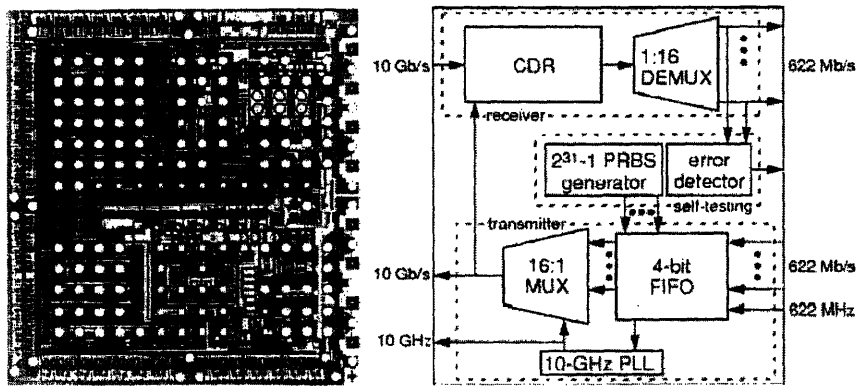


Figure 35: Integrated transceiver electrical circuitry with Si BiCMOS technology. [11]

This all in one transceiver electrical circuitry contains 26000 active elements: 16,000 SiGe HBTs and 10,000 CMOS transistors [11]. This demonstrates the ability to create high speed and integrated electronics for future optical receivers based on silicon substrates.

Although the speed of electronics based on Si has continually reached record cut-off and operating frequencies, devices based on III-V compound semiconductors still have a leg up in speed. For higher speed and data rates, wavelength division multiplexing will be needed. Single 40Gb/s InGaAs PIN detectors have been repeatedly demonstrated and are ready for next generation receivers. A 40Gb/s receiver based on Si will need to multiplex two wavelength together using two Ge detectors, if each Ge detector can operate at 25GHz. Because the small bandgap and semi-conducting nature of Si substrates, Si has lower breakdown voltage than GaAs and InP. Therefore, silicon falls short in competition with III-V materials when high dynamic range and biasing range is needed in certain analog receiver applications.

Silicon's low cost and economy-of-scale has continually motivated research endeavors to increase the functionality of silicon, through the creation of Ge detectors, low-loss waveguides and integrated high speed electronics, all compatible with silicon substrate. CMOS process compatible Ge detectors on silicon have been demonstrated in the laboratory, with comparable responsivity to standard detectors. Although reliability and passivation are still under work, initial demonstrations are promising. Research has also demonstrated a variety of low-loss waveguides on silicon. Work on coupling waveguide to Ge detector is ongoing, with few results reported so far. To reach the speed of current state-of-the-art GaAs or InP receivers, Si will have to rely on wavelength multiplexing. With appropriate research efforts, silicon is catching up fast to InP to realize optical integration and is emerging as a strong contender in future digital optical receivers. With compatibility to Si electronics, silicon microphotonics is especially for attractive for the current interconnect delay faced by ICs and computers.

Silicon microphotonics, along with InP and GaAs opto-electronics, expect to reduce cost through better manufacturing and integration. The impact of monolithic integration on receiver cost will be the topic of discussion for next Chapter.

VII. Cost Analysis

Note: Numbers presented in this analysis are approximations, not to be taken as exact.

Introduction

Above sections discussed that the receiver industry is working to reduce cost from two general approaches. One is through better component manufacturing (cheaper substrates, larger wafer sizes) and the other is through integration. Which materials platform provides a more cost effective solution is a difficult question to address, since it is highly dependent on market and business approaches. The manufacturing of opto-electronic components is likely to take just a portion of any given foundry capacity, and therefore these component costs will be sensitive to the volume of other products going through the foundry. For example, the cost of InP opto-electronics will be sensitive to market of InP HEMTs and Si opto-electronics cost will be sensitive to the market of Si electronics. The cost analysis in this thesis would focus on the implication of integration on cost.

Monolithic integration brings two potential cost benefits, one at the chip manufacturing level and the other at the module assembly level. The cost benefit of an integrated chip at module assembly level is well accepted, since the number of assembly steps saved will directly translate into cost savings. But whether integration actually translates into chip manufacturing cost saving is a more difficult question, since yield and throughput time can change. This analysis begins with looking at the cost of manufacturing discrete or integrated photodiodes and TIAs, then moving on to a larger scale of integration.

A 100mm GaAs fab that is currently in production as a basis for this analysis, and therefore the photodiode and TIA material and processes are based on the metamorphic GaAs technology discussed in Section V. But the general conclusion drawn from this section is also applicable to InP as well, for their processing technology is relatively similar. 100mm InP substrates with epitaxial layers cost about $1000/wafer and GaAs

cost about $500/wafer. Currently, this facility manufactures microwave amplifiers on GaAs substrates, and available equipments allow a maximum wafer capacity of 11,000 per year. The following table presents some estimation of the largest fixed and variable costs for the fab:

Equipment Capital	$46M
Facility Capital	$34M
Facility operation	$3M/yr
Labor cost	$11M/yr
4 inch substrate cost	$1000/wf

Table 3. Primary fixed and variable cost for 100mm GaAs fab, 11,000 wafers/year

The microwave amplifier wafer material and fabrication process is essentially the same as that of the TIA. The opto-electronic chips are also based on GaAs substrate but have different epitaxial layers, with metamorphic buffer layers as discussed in the previous section. These optical receiver chips will operate at 1550nm wavelength with frequency above 20 GHz. The developed fabrication process for opto-electronics is not significantly different from that of microwave amplifiers or TIA, requiring no special equipments or a very lengthy process step. The fabrication process flow is listed in Appendix. Following sections look at the cost of manufacturing optical receivers using two approaches.

Cost Model I

The most simple way to calculate cost per area is to take the sum of annual fixed cost and operating cost, divided by the good sellable die area produced per year.

$$\frac{Cost}{Area} = \frac{AnnualFixedCost + AnnualOperatingCost}{TotalSellableGoodDieAreaPerYear} \tag{8}$$

Here we suppose the fab is running very close to its maximum capacity making microwave amplifiers. In light of market opportunities in opto-electronic, management would like to dedicate a portion of the current wafer capacity to fabricate receivers.

Process technology are available to either manufacture the receiver circuits discretely or monolithically. In Scenario I, photodiodes and TIAs are fabricated on similar substrate but separate wafers. In Scenario II, monolithic integration puts the photodiode and TIA together in an OEIC.

According to Equation 7, the cost per area for Scenario I is:

$$\frac{Cost}{Area} = \frac{AnnualFixedCost + AnnualOperatingCost}{(N_{g,diode} \times A_{diode}) + (N_{g,TIA} \times A_{TIA}) + (N_{g,amp} \times A_{amp})} \quad (9)$$

Where

$N_{g,\,diode}$: the number of sellable good photodiode dies produced per year

$N_{g,\,TIA}$: the number of sellable good TIA dies produced per year

$N_{g,\,amp}$: the number of sellable good amplifier dies produced per year

A_{diode}: the area of a photodiode die

A_{TIA}: the area of a TIA die

A_{amp}: the area of an amplifier die

The total number of good photodiode dies produced per year, $N_{g,diode}$, is calculated by taking into account number of wafer starts, breakage, yield, die and useful wafer area. This is shown in Equation 10:

$$N_{g,diode} = \{\frac{(W_{diode} \times B_k) \times A_{wf} \times p_{use}}{A_{diode}}\} \times Y_{diode} \quad (10)$$

Where

W_{diode}: the total number of photodiode wafers to be started

B_k: breakage factor accounting for the percentage of wafers that either break or have been mis-processed.

A_{wf}: the total area on a 100mm wafer

P_{use} : percentage of useful wafer area excluding edge die and process control areas

A_{diode} : the area of a photodiode die

Y_{diode} : the final die yield of the photodiode process

$N_{g,\,TIA}$ and $N_{g,\,amp}$ are calculated similarly to equation 9. The cost per area for Scenario II is also calculated in a similar manner.

As Equation 8 and 9 show, the cost per wafer and cost per area calculated this way is the same regardless of which product is on the wafer. Though this is not the best approach and the results obtained are not very realistic, they are useful for illustrative purposes. The cost of a particular die is simply the die area times cost per area. Table 4 presents the cost result for different percentage of line capacity dedicated to opto-electronics:

Line dedication to opto-electronics	5%	20%	90%
Cost for Scenario One			
Cost per wafer	$3,583	$3,581	$3,568
cost per mm2	$0.75	$0.75	$0.74
cost per diode die	$0.07	$0.07	$0.07
cost per TIA die	$4.76	$4.75	$4.74
cost of diode and TIA pair	$4.82	$4.82	$4.80
Cost for Scenario Two			
Cost per wafer	$3,613	$3,700	$4,173
Cost per mm2	$0.75	$0.78	$0.93
cost per OEIC die	$4.81	$4.98	$5.90

Table 4: Results from Cost Model I

The results show that cost/wafer and cost/mm^2 decreases with greater opto-electronics utilization for Scenario I but increases for Scenario II. We also see that at 5% capacity utilization, OEIC die is slightly less expensive than a diode and TIA pair. But OEIC die costs about 16 cents more at 20% capacity utilization and about $1 more at 90% utilization. This result is showing that integration becomes more and more expensive as more opto-electronic circuits are fabricated. This certainly contradict the expectation that integration should decrease cost with larger economies of scale, but a closer look at the monolithic integration process explains why.

There are 7 mask levels or photo steps for photodiode process, 12 for TIA, 12 for microwave amplifier, and 14 for OEIC. The throughput time of a process is largely

determined by the number of photo steps it takes. First glance shows that integration saves about 5 photo steps per wafer, which should translate into cost savings. But the photodiode dies are much smaller in size than the TIA or OEIC dies:

Photodiode die area:	0.09 mm^2
TIA die area	6.375 mm^2
OEIC die area	6.375 mm^2

Therefore, number of photodiode dice produced per wafer is about 72 times more than TIA or OEIC. Table 5 shows the number of photo steps and the number of dies from one wafer for each product:

	Number of photo steps	Number of dies
One Photodiode Wafer	7	63,000
One TIA Wafer	12	886
One OEIC Wafer	14	886

Table 5: Comparison of number of photosteps for individual photodiode, TIA and OEIC wafers

The number of photodiodes and TIAs manufactured should be approximately equal because they sell in pair. To make a certain volume of receivers, many more TIA and OEIC wafers are required, as shown in Table 6.

	Number of wafer Needs	Number of photosteps of all wafers	Number of dies
Photodiode Wafer	1	7	63000
TIA Wafer	71	852	63000
OEIC Wafer	71	994	63000

Table 6. Comparison of number of photosteps for photodiode, TIA and OEIC to manufacture a certain number of optical receivers per year.

Therefore, we should compare the total number of photo steps needed per year by Scenario I with Scenario II, instead of just photo steps per wafer. To manufacture $N_{g,r}$ number of receiver components per year, the number of photo steps Scenario I involves is:

$$PS_I = \frac{MS_{diode} \times N_{g,r}}{D_{g,diode}} + \frac{MS_{TIA} \times N_{g,r}}{D_{g,TIA}} \tag{11}$$

Where

MS: the number of mask levels for a process

D_g : the number of good sellable dice obtained from one wafer

Similarly, the number of photo steps Scenario II involve is:

$$PS_{II} = \frac{MS_{OEIC} \times N_{g,r}}{D_{g,OEIC}} \tag{12}$$

The number of good sellable dice from one wafer is calculated with the following equation:

$$D_g = \frac{A_{wf} \times p_{use} \times Y}{A_{die}} \quad (13)$$

Where

A_{die}: the area of a particular die

Taking the difference of equation 11 and 12 substituting in equation 13, we have:

$$PS_{II} - PS_I = K\{\frac{MS_{OEIC} \times A_{OEIC}}{Y_{OEIC}} - (\frac{MS_{diode} \times A_{diode}}{Y_{diode}} + \frac{MS_{TIA} \times A_{TIA}}{Y_{TIA}})\} \times N_{g,r} \quad (14)$$

Where

$K = 1/(A_{wf} \times P_{use})$

$N_{g,r}$ = total number of receiver components to make per year

Substituting the appropriate numbers for mask levels, die areas and other parameters, we have:

$$PS_{II} - PS_I = (\frac{1}{8107mm^2 \times 0.81})\{\frac{14 \times 6.375mm^2}{Y_{OEIC}} - (\frac{7 \times 0.09mm^2}{Y_{diode}} + \frac{12 \times 6.375mm^2}{Y_{TIA}})\} \times N_{g,r} \quad (15)$$

Since the diode area is so small, the diode term is largely negligible in equation 8. The greater the number of components to make per year, the greater the number of photo steps Scenario II incur. Table 7 tabulates the result based on equation 8 for three different manufacturing volumes of receivers.

Number of receivers to make/yr ($N_{g,r}$)	300,000	500,000	700,000
photodiode wafers to start/yr	4	7	10
TIA wafers to start/yr	291	485	680
OEIC wafers to start /yr	291	485	680
Scenario I photo steps /yr	3524	5873	8222
Scenario II photo steps /yr	4077	6796	9514
Difference in photosteps /yr	554	923	1292

Table 7: Comparison of number of photosteps for Scenario I and II for different manufacturing volume of optical receivers.

Above table calculation was done assuming all yield are the same and are at 100%. That is not true in reality, of course. In fact, OEIC has lower yield than TIA or photodiode, which further serves to increase the number of photo steps Scenario II needs. The yield for OEIC is about 87%, photodiode 92% and TIA 93%. For a more detail discussion of yield mechanisms, next section will have more details about yield.

Since this cost approach assumes the fab is operating at or near its maximum capacity, the extra photosteps that the OEIC process incur can shrink the wafer throughput of the line and therefore increase cost per wafer. Realistically, most semiconductor fabs do not operate at or near its maximum capacity. The addition of a more complicated process, such as OEIC, may not necessary translate into capacity decrease. A second cost calculation takes this into account.

Cost Model II

In this cost approach, we start by assuming that the facility is still making microwave amplifier circuits. Current amplifier wafer volume is about 80% of its maximum capacity, which is about 8800 wafers per year. Additional opto-electronic wafers that are processed will share the remaining 20% capacity. Instead of calculating

the same cost per area for all three different products, this second cost approach weights in the fact that each completed TIA wafers occupies equipment twice as long as a photodiode wafer, so the photodiode wafer cost should be lower than that of TIA. Similarly, since each OEIC wafer takes about 15.5% more time than an amplifier wafer the OEIC wafer cost should be more costly than the amplifier wafer. So here we look at the marginal cost an extra photo step would occur. With these refinements, we calculate another cost per area for the two Scenarios.

At 80 percent capacity and making amplifiers, only three shifts of labor are employed. The total fixed and variable operating costs are shared by all amplifier wafers. The cost per amplifier wafer is $4541. A cost per photo step is calculated through the following formula:

$$C_{photo} = \frac{AnnualizedCapitalCost + AnnualOperatingCost}{W_{amp} \times MS_{amp}} \qquad (16)$$

Where

W_{amp}: the number amplifier wafers to be started per year

The C_{photo} before the introduction of opto-electronic wafers are $295. With the introduction of additional wafers, the total fixed cost will be shared by more wafers and so the cost per amplifier wafer and C_{photo} will go down. Each additional wafer processed in the fab will not incur any additional fixed cost, but will incur a marginal cost of in terms of material (photoresist, metal, chemical etchants....) and equipment ware and maintnance. In this analysis, we will assume that marginal cost of each additional photo step will be $100. Cost-per-wafer is calculated with the following formula:

$$C_{wf} = MS \times C_{photo} \times C_{sub} \quad (17)$$

Where

MS: number of photo steps for a process

C_{sub} : Cost of wafer substrate

Assuming a certain number of receivers, $N_{g,r}$, is to be produced per year, Table 8 presents results for different $N_{g,r}$.

Number of Receivers Produced / Year ($N_{g,r}$)	300,000	500,000	1,000,000
Cost per Amplifer Wafer	$4,441	$4,379	$4,453
Scenario I			
Number of Photodiode Wafers to Start	5	9	18
Number of TIA Wafers to Start	389	649	1297
Cost per Photo Step	$287	$282	$288
Photodiode Cost Per Die	$0.05	$0.05	$0.05
TIA Cost Per Die	$5.01	$4.94	$5.02
TIA and Photodiode Cost	$5.06	$4.99	$5.07
Scenario II			
Number of OEIC Wafers to Start	418	697	1393
Cost per Photo Step	$285	$279	$282
OEIC Cost Per Die	$5.46	$5.39	$5.47
Differnce in Receiver Cost between Scenario I an II	$0.40	$0.40	$0.40

Table 8: Results of Cost Model II

At a receiver annual volume of 1,000,000, an extra shift of labor is added to accommodate the capacity. In this analysis, OEIC die is $0.40 more expensive than a photodiode and TIA pair, but that difference does not increase with increasing volume of receivers.

The conclusion from two above cost calculations is that when the facility is operating at or near its maximum capacity, introducing an integration process with a larger number of photo steps over discrete process will shrink capacity and increase cost per die. The higher cost of OEIC over discrete will raise as production volume increases. In comparing overall process complexity, one should look beyond comparing the photosteps it takes to manufacture a wafer, but exam the difference in photosteps to manufacture all the desire components, as in Equation 15. In the case where photodiodes are much smaller than TIA, this made a big difference in the photosteps it takes to manufacture a certain volume of receivers. For a fab that has enough line capacity to spare, introduction of an OEIC will still cost more than a photodiode and TIA pair, but the difference in cost will not increase with production volume.

Although the analysis of photodiode and TIA integration did not show a chip manufacturing cost reduction, one must remember the cost savings that an integrated chip brings at the module assembly level. As long as the cost increase in an OEIC die is not higher than the savings at receiver module assembly, OEIC will still be a more cost effective product. Current module assembly is very labor intensive, and labor cost will be a more significant cost factor when module production volume increases. Then the value of an integrated chip will be much greater at higher module production volume.

Yield

This section discusses the yield of integrated process versus the discrete process. Generally there are a few different types of yield.

- line yield: the number of good and completed wafers versus the number of wafers started.
- Test yield: number of dies that meet the performance requirements.
- Die visual yield: the number of dies that look good visually, with no visual scum that can come from processing.

The die yield this thesis refers to combines test yield and die visual yield. For the yield for each step in each process, please refer to Appendix. Table 9 presents the final die yield for each process:

Product	Yield
Photodiode	82.7%
TIA	93.2%
OEIC I (diode and TIA)	85.0%
OEIC II (diode, TIA and EDMHEMT)	83.3%

Table 9: Yield of photodiode, TIA, OEIC I and OEIC II.

The die yield of a particular process is largely determined by a few yield determining step in the process. For photodiode this is the anode etch, passivation, and dice. Most of diodes fail due to high leakage current. Good anode profile and passivation is important in reducing leakage current. During dicing there can be significant chip-out because the photodiode are very small. For circuits that involve transistor gate, such as in TIA and EDMHEMT, the yield-limiting step is generally gate write, etch and metallization. Gate fingers width are on the range of 250nm to 175nm. Failure can come from a gate finger landing on a material defect, or a gate finger that has poor contact with semiconductor. Misalignment can cause a gate to short-out to the source-drain metal. Another critical yield step is via etch on the backside to form ground contacts to the front. Highly anisotropic etch is needed to form hole that are about 10μm wide but 100μm deep. Over etching can lower gain and under etching can create an open. And it is important to achieve etch uniformity across the wafer. Most other processing step, such as mesa etch and source-drain metallization, tend to have much higher yield with the small possibility of leaving scum on wafer. The minimum features on those steps are quite large.

Even though OEIC can save the number of photolithography to generate one receiver, the yield of a large and integrated die will be poor if yield for certain critical steps, such as gate and via, are not sufficiently high. But it is important to keep in mind that the yield OEIC is equivalent to the yield of a photodiode bonded to TIA at assembly. Therefore, a better yield comparison should include the bonding yield at assembly.

Larger Scale Integration

Integrated photonic circuits will include more optical and electrical elements than just photodiode and TIA. In this section, we look at the integration benefit of integrating

an extra electrical component. This electrical component could be another amplifier or a digital circuit for demultiplexing. On metamorphic GaAs substrates, enhancement-mode devices combined with depletion-mode devices can perform such digital functions. Cost approach II as discussed above is used for this analysis. One set of result is presented in Table 10 by assuming that there is no significant die area decrease with OEIC:

Photodiode die area:	0.09 mm^2
TIA die area	6.375 mm^2
ED MHEMT die area	6.375 mm^2
OEIC die area:	12.75 mm^2

Number of Receivers Produced / Year ($N_{g,r}$)	300,000	500,000
Cost per Amplifer Wafer	$4,441	$4,379
Scenario I		
Number of Photodiode Wafers to Start	6	10
Number of TIA Wafers to Start	389	649
Number of ED Wafers to Start	389	649
Cost per Photo Step	$279	$270
Photodiode Cost Per Die	$0.05	$0.05
TIA Cost Per Die	$4.91	$4.78
ED Cost Per Die	$4.91	$4.78
TIA, Photodiode and ED Cost	$9.87	$9.61
Scenario II		
Number of OEIC Wafers to Start	836	1393
Cost per Photo Step	$276	$265
OEIC Cost Per Die	$10.69	$10.44
Differnce in Receiver Cost between Scenario I an II	$0.82	$0.82

Table 10. Cost Model II results with OEIC that integrates EDMHEMT, with no significant area reduction in OEIC.

In this case, OEIC die is more expensive than the discrete dies. This is due to the greater number of photo steps and introduced and the lower yield that is associated with a larger die. But if and OEIC die can result in a smaller overall area, then OEIC dies can be cheaper. Results in Table 11 are obtained by assuming that OEIC die area is about 80% of the total die area of TIA, EDMHEMT and photodiode:

Photodiode die area:	0.09 mm^2
TIA die area	6.375 mm^2
ED MHEMT die area	6.375 mm^2
OEIC die area:	10.2 mm^2

Number of Receivers Produced / Year ($N_{g,r}$)	300,000	500,000
Cost per Amplifer Wafer	$4,441	$4,379
Scenario I		
Number of Photodiode Wafers to Start	6	10
Number of TIA Wafers to Start	389	649
Number of ED Wafers to Start	389	649
Cost per Photo Step	$279	$270
Photodiode Cost Per Die	$0.05	$0.05
TIA Cost Per Die	$4.91	$4.78
ED Cost Per Die	$4.91	$4.78
TIA, Photodiode and ED Cost	$9.87	$9.61
Scenario II		
Number of OEIC Wafers to Start	669	1115
Cost per Photo Step	$279	$270
OEIC Cost Per Die	$9.53	$9.27
Differnce in Receiver Cost between Scenario I an II	-$0.34	-$0.34

Table 11. Cost Model II results with OEIC that integrates EDMHEMT, with significant area reduction in OEIC.

Here we see that OEIC dies are less expensive, largely because the die area has decreased.

In conclusion, integration can reduce cost through: decreasing the number of photosteps it takes to manufacture a certain volume of products, improving die yield and increasing functionality per area. In the case of integration on GaAs and InP, since yield is mostly determined by gate processing, so there is no significant yield improvement with integration. Yield will actually significantly decrease with integration if yield at gate or via etch isn't sufficiently high. If an integrated die is not smaller in area than the areas of discrete dies combined, then integration will bring little cost benefits and may even increase cost. Functionality per area needs to increase and in turn will also save the number of photosteps to produce a certain function. The cost advantage of an integrated chip is very sensitive to process complexity, and that is important to keep in mind for integration research endeavors. As a reminder, cost conclusions drawn here only apply to integrated chip manufacturing. At module assembly, hybrid solution will be more costly in labor and there is a further decrease in yield then the photodiode is bonded with the TIA. Though an integrated chip may cost more than discrete chips, integrated solution will still be more desirable if the benefits it bring at module assembly exceeds its higher cost.

VIII. Conclusion

Future growth of optical communication relies on the ability of optical receivers to reduce cost and size while increase performance and functionality. Current industry is addressing these future needs through better manufacturing and monolithic integration. Three material platforms, InP, GaAs and Si, are contenders for the future optical receiver market. As the traditional platform for optically active components and record high-speed electronics, InP technology has demonstrated most maturity for waveguide integrated photonic circuit through achievements in photodetectors, low-loss waveguides, waveguide-detector coupling and fiber-waveguide coupling. But as the market is seeking to commoditize communication, InP is feeling pressure from GaAs and Si technologies that possess greater manufacturability. Metamorphic GaAs has demonstrated promising results in creating long-wavelength photodetectors and small-scale OEICs. Demonstration of waveguides and coupling has been limited, mainly due to the lack of funding during the current economy slump. Therefore, more work and resources are needed to make long-wavelength and integrated photonics on GaAs into a reality and marketable product. Research work on silicon has produced promising results for Ge detectors and low-loss waveguides, with ongoing work on waveguide-detector coupling. Whether GaAs or Si can successfully replace InP in future optical receivers will depend on their ability to provide needed performance and address receiver costs through their ability to integrate and manufacture cheap components.

Monolithic integration reduces receiver chip costs through higher integration density, yield improvement and reductions in number of photosteps. The cost model created in this thesis reveals that monolithic for GaAs and InP does not necessary mean less photosteps are needed to perform and yield improvement. Cost savings will mainly come from increased density in chip manufacturing, and improved yield and less assembly in module assembly.

Appendix: Yield

Photodiode	
Process steps	Yield
p-contact photo and metallize	99.5%
andoe photo and etch and passivate	96.0%
mesa photo and etch	99.5%
n-contact photo and mettalize	99.5%
air bridge, thick metal photo and metalize	99.5%
anode passivation	95.0%
backside mount	100.0%
grid pattern and mettalize	99.5%
demount	100.0%
dice	93.0%
final yield	82.7%

TIA	
Process steps	Yield
mesa pattern and etch	99.5%
Source Drain photo and metallize	99.5%
gate pattern etch and metallize	98.0%
capacitor bottom photo and metallize	99.5%
nitride deposition	100.0%
Tan protect photo	99.5%
Tan deposition	100.0%
Tan photo and etch back	99.5%
nitride photo	99.5%
airbridge, thick metal photo and metalize	99.5%
backside mount and thin	100.0%
via photo and etch	99.0%
grid photo and metallize	99.5%
demount	100.0%
dice	100.0%
final yield	93.2%

Microwave Amplifiers	
Process steps	Yield
mesa pattern and etch	99.5%
Source Drain photo and metallize	99.5%
gate pattern etch and metallize	98.0%
capacitor bottom photo and mettallize	99.5%
nitride deposition	100.0%
Tan protect photo	99.5%
Tan deposition	100.0%
Tan photo and etch back	99.5%
nitride photo	99.5%
airbridge, thick metal photo and metalize	99.5%
backside mount and thin	100.0%
via photo and etch	99.0%
grid photo and metallzie	99.5%
demount	100.0%
dice	100.0%
final yield	93.2%

EDMHEMT	
Process steps	Yield
mesa pattern and etch	99.5%
Source Drain photo and metallize	99.5%
gate pattern etch and metallize	98.0%
capacitor bottom photo and mettallize	99.5%
nitride deposition	100.0%
Tan protect photo	99.5%
Tan deposition	100.0%
Tan photo and etch back	99.5%
nitride photo	99.5%
airbridge, thick metal photo and metalize	99.5%
backside mount and thin	100.0%
via photo and etch	99.0%
grid photo and metallzie	99.5%
demount	100.0%
dice	100.0%
final yield	93.2%

OEIC, integrating photodiode and TIA	
Process steps	Yield
p-contact photo and metallize	99.5%
andoe photo and etch and passivate	96.0%
mesa photo and etch	99.5%
Source Drain photo and metallize	99.5%
gate pattern etch and metallize	98.0%
capacitor bottom photo and mettallize	99.5%
nitride deposition	100.0%
Tan protect photo	99.5%
Tan deposition	100.0%
Tan photo and etch back	99.5%
nitride photo	99.5%
airbridge, thick metal photo and metalize	99.5%
photodiode passivation	95.0%
backside mount and thin	100.0%
via photo and etch	99.5%
grid photo and metallzie	99.5%
demount	100.0%
dice	100.0%
final yield	85.0%

OEIC, integrating photodiode, TIA and EDMHEMT	
Process steps	Yield
p-contact photo and metallize	99.5%
andoe photo and etch and passivate	96.0%
mesa photo and etch	99.5%
Source Drain photo and metallize	99.5%
gate pattern etch and metallize	96.0%
capacitor bottom photo and mettallize	99.5%
nitride deposition	100.0%
Tan protect photo	99.5%
Tan deposition	100.0%
Tan photo and etch back	99.5%
nitride photo	99.5%
airbridge, thick metal photo and metalize	99.5%
photodiode passivation	95.0%
backside mount and thin	100.0%
via photo and etch	99.5%
grid photo and metallzie	99.5%
demount	100.0%
dice	100.0%
final yield	83.3%

References:

1. Professor Rajeev Ram

2. Rober G. Hussperger, Integrated Optics, Theory and Technology, 1995, 4th edition.

3. L. C. Kimerling, "Silicon Microphotonics: The Next Killer Technology,"2003 Kluwer Academic Publishers.

4. Corning website

5. Casimer DeCusatis, Eric Maass, Darrin P. Clement, Ronald C. Lasky, Handbook of Fiber Optic Data Communication, 1998.

6. M. F. Dautartas, J. Fisher, H. Luo, P. Datta, A. Jeantilus "Hybrid Optical Packaging, Challenges and Opportunities," Haleos Inc., *2002 Electronic Components and Technology Conference.*

7. Photonic Materials and Devices Lecture, 3.46, MIT by L.C. Kimerling

8. Akira Endoh, Yoshimi Yamashita, Keisuke Shinohra, Masataka Higashiwaki, Kohki Hikosaka, Toshiaki Matsui, Satoshi Hiyarnizu, Takashi Mimura, "InP HEMTs, Physics, Applications, and Future," Fujistu, 2003.

9. F. Robin, A. Orzati, R. Limacher, H. Meier, W. Bachtold, "InP HEMT Based CPW Amplifiers for 94 and 110 GHz," Swiss Federal Institute of Technology, *Indium Phosphide and Related Materials, 2003. International Conference on, 12-16, May 2003. Pages 110-113.*

10. S. Masuda, T. Hirose, T. Takahashi, M. Nishi, S. Yokokawa, S. Iijima, K. Ono, N. Hara, K. Joshin, "An over 110-GHz InP HEMT flip-chip distributed baseband amplifier with inverted microstrip line structure for optical transmission systems," Fujitsu Laboratories Ltd., *Gallium Arsenide Integrated Circuit Symposium, 2002. 24th Annual Technical Digest, 20-23 Oct. 2002. Pages 99-102.*

11. K. Washio, "SiGe HBT and BiCOMS Technologies for Optical Transmission and Wireless Communication Systems," Central Research Laboratory, Hitachi Ltd. *IEEE Transctions on Electron Devices, Vol. 50, No. 3, March 2003.*

12. C.L. Cheng, R.P.H. Chang, B. Tell, S. M. Z. Parker, Y. Ota, G.P. Vella-Coleiro, R.C. Miller, J.L. Zilko, B.L. Kasper, K.F. Brown-Goebeler, V.D.Mattera, "Monolithically integrated receiver front end: InGaAs p-I-n amplifer," AT&T Bell Labs, *IEEE Transactions on Electron Devices, Vol. 35, No. 9, Sept. 1988.*

13. L.M. Lunardi, S. Chandrasekhar, "Integrated p-I-n/HBT Photoreceivers for Optical Communications," *IEDM 96-645.*

14. P.M. Smith, D. Dugas, K. Chu, K. Nichols, K.G. Duh, J. Fisher, L. MtPleasant, D. Xu, L. Gunter, A. Vera, R. Lender, D Meharry, "Progress in GaAs Metamorphic HEMT Technology for Microwave Applications," BAE Systems, 2003 IEEE GaAs Digest.

15. D. R. Goff, "A Brief History of Fiber Optic Technology", *Fiber Optic Reference Guide, 3rd ed.* http://www.fiber-optics.info/fiber-history.htm

16. RHK Consulting services

17. L. Pavesi, D.J. Lockwood,editors, Silicon Photonics, page 5.

18. N. Savage, "Linking With Light", *IEEE Spectrum, Vol. 39, Iss. 8, Aug. 2002, Pages 32-36*

19. K. Takahat, Y. Muramoto, H. Fukano, K. Kato, A. Kozen, S. Kimura, Y. Imai, Y. Miyamoto, O. Nakajima, Y. Matsuoka, "Ultrafast Monolithic Receiver OEIC Composed of Multimode Waveguide p-I-n Photodiode and HEMT Distributed Amplifier", NTT Photonics laboratories, *IEEE Journal of Selected Topics in Quantum Electronics, vol. 6, No. 1, Jan/Feb 2000.*

20. Robetr J. Deri, Eli Kapon, "Low-Loss III-V Semiconductor Optical Waveguides", IEEE Journal of Quantum Electronics, Vol. 27, No. 3, March 1991.

21. Robert J. Deri, "Monolithic Integration of Optical Waveguide Circuitry with III-V Photodetectors for Advanced Lightwave Receivers," Journal of Lightwave Technology, Vol. 11, No. 8, August 1993.

22. Valery I. Tolstikhin, Adam Densmore, Kirill Pimenov, Sylvain Laframboise, "Single-Mode Vertical Integration of p-i-n Photodetectors With Optical Waveguide for Monitoring in WDM Transmission Systems", IEEE Photonics Technology Letters, Vol. 15, No. 6, June 2003.

23. K. Kato, S. Hata, A. Kozen, S. Oku, S. Matsumoto, J. Yoshida, "22GHz Photodiode Monolithically Integrated With Optical Waveguide on Semi-Insulating InP Using Novel Butt-Joint Structure," Electronics Letters, 4th June 1992, Vol. 28, No. 12

24. Robert J. Deri, O. Wada, "Impedance Matching for Enhanced Waveguide/Photodetecor Integration," Applied Physics Letters, 55(26), 25 December 1989.

25. Ingrid Loerman, Peter Vann Daele, Piet M. Demeester, "A Review on Fabrication Technologies for the Monolithic Integration of Tapers with III-V Semiconductor Devices," IEEE Journal of Selected Topics in Quantum Electronics, Vol. 3, No. 6, December 1997.

26. N. Hara, K. Makiyama, T. Takahashi, K. Sewada, T. Arai, T. Ohki, M. Nihei, T. Suzuki, Y. Nakasha, M. Nishi, "Highly Uniform InAlAs-InGaAs HEMT Technology for High-Speed Optical Communication Systems ICs," IEEE Transactions on Semiconductor Manufacturing, Vol. 16, No. 3, August 2003.

27. D.P. Docter, K.R. Elliott, A.E. Schmitz, K. Kiziloglu, J.J. Brown, D.S. Harvey, H.M. Karatnicki, "Low noise InAlAs/InGaAs HEMTs grown by MOVPE," 10th International Conference on InP and Related Materials, May 1998.

28. J.H. Jang, G. Cueva, R. Sankaralingam, P. Fay, W.E. Hoke and I. Adesida, "Monolithic Integration of InGaAs Photodiodes and InGaAs/InAlAs HEMTs on GaAs Substrates for Long Wavelength OEIC Applications," 2002 IEEE GaAs Digest.

29. Y. Zhang, C.S. Whelan, R. Leoni, P.F. Marsh, W.E. Hoke, J.B. Hunt, C.M. Laighton, T.E. Kazior, "40Gbit/s OEIC on GaAs substrate through metamorphic buffer technology", Raytheon RF Division, *Electron Device Letters, IEEE, Vol. 24, Issue: 9, Sept. 2003, Pages 529-531.*

30. D.C. Dumka, H.Q. Tseng, M.Y. Kao, E.A. Beam, P. Saunier, "High-Performance Double-Recessed Enhancement –Mode Metamorphic HEMTs on 4-In GaAs Substrates," IEEE Electron Device Letters, Vol. 24, No. 3, March 2003.

31. V. P. Kesan, P.G. May, E. Bassous, S.S. Iyer "Integrated Waveguide-Photodetector Using Si/SiGe Multiple Quantum Wells for Long Wavelength Applications," IBM Research Division, Watson Research Center, *Electron Devices Meeting, 1990. Technical Digest., International, 9-12 Dec. 1990. Pages 637-640.*

32. D.L. Harame, J.M.C. Stork, G.L. Patton, S.S. Iyer, B.S. Meyerson, G.J. Scilla, E.F. Crabbe, and E.Ganin, IBM Research Division, Watson Research Center. "High Performance Si and SiGe-based PNP transistors." *Electron Devices Meeting, 1988. Technical Digest, International, 11-14 Dec. 1998, pages 889-991.*

33. A. Umbach, D. Trommer, G.G. Mekonnen, W. Ebert, G. Unterborsch, "Waveguide integrated 1.55μm photodetector with 45GHz bandwidth," *Electronics Letters*, 7th November 196 Vol. 32, No.23.

34. Shih-Hsiang Hsu, F.G. Johnson, Y.C. Liu, F.J. Towner, S.A. Tabatabaei, Sambhu Agarwala, John V. Hryniewicz, Yen-Ping Ho, Wenhua Lin, Y.J. Chen, M. Dagenais, D.R. Stone, "InGaAs p-I-n photodiodes on AlGaAs/GaAs waveguides and monolithic integration applications," CLEO 1997

35. M. S. Acarlar, S.L. Moyer, S.D. Robinson, "Use of Low Cost Plastic DIPs and Injection Molded Parts in Packaging of Optical Data Links," AT&T Bell Laboratories, *1992 Electronic Components and Technology Conference, Proceedings., 42nd.*

36. N. Shimizu, K. Murata, A. Hirano, Y. Miyamoto, H. Kitabayashi, Y. Umeda, T. Akeyoshi, T. Furuta, N. Watanabe, "40Gbit/s monolithic digital OEIC composed of unitravelling-carrier photodiode and InP HEMTs", NTT Photonics Laboratories, *IEEE Electronics Letters, vol. 36, Issue 14, 6 July 2000.*

37. T. Wipiejewski, Y.A.Akulova, C.Schow, A. Kari, S. Nakagawa, P. Kozodoy, G. A. Fish, J. DeFranco, A. Dahl, M. Larson, D. Pavinski, T. Butrie, L.A. Coldren "Monolithic Integration of a Widely Tunable Laser Diode with a High Speed Electro Absorption Modulator", Agility Communication. *2002 Electronic Component and Technology Conference*

38. M. R. Gokhale, P.V. Studenkov, J.Ueng-McHale, J.Thomson, J.Yao, J. van Sanders, "Uncooled, 10Gb/s 1310nm Electroabsorption Modulated Laser," 2003 Optical Society of America, http://www.asipinc.com/pdf/1310nmuncooledEML.pdf

39. M.H. Choi, H.J. Koh, E.S. Yoon, K.C. Shin, K.C. Song, "Self-aligning Silicon Groove Technology Platform for the Low ost Optical Module," Optoelectronic Device Lab., LG Cable Ltd. Korea. *Electronic Components and Technology Conference, 1999 Proceedings. 49th, 1-4June 1999.*

40. Y. Akahori, T. Ohyama, T. Yamada, K. Katoh, T. Ito, "High speed photoreceiver using solder bumps and microstrip formed on a silicon optical bench," *IEEE Phtonics Technology Letters, Vol. 11, No. 4, April 1999.*

41. V.K. Yang, S.M. Ting, M.E. Groenert, M.T. Bulsara, M.T. Currie, C.W. Leitz, E.A. Fitzgerald, "Comparison of luminescent efficiency of InGaAs quantum well structures grown on Si, GaAs, Ge, and SiGe virtual substrates." *J. Applied Physics, 93, 5095 (2003).*

42. G. Masini, L. Colace, G. Assanto, H.C. Luan, L. Kimerling High Performance p-I-n Ge on Si Photodetectors for the Near Infrared: From Model to Demonstration. IEEE Transaction on Electron Devices, Vol. 48, No. 6, June 2001

43. N. Hara, K. Makiyama, T. Takahashi, K. Sawada, T. Arai, T. Ohki, M. Nihei, T. Suzuki, Y. Nakasha, M. Nishi, "Highly Uniform InAlAs-InGaAs HEMT Technology for High-Speed Optical Communication System ICs" Fujitsu Laboratories Ltd., *IEEE Transactions on Semiconductor Manufacturing, Vol. 16, No.3, August 2003.*