Packaging Solution for VLSI Electronic Photonic Chips

by

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B.S. Materials Science and Engineering
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ABSTRACT

As the demand of information capacity grows, the adoption of optical technology will increase. The issue of resistance and capacitance is limiting the electronic transmission bandwidth while fiber optic delivers data at the speed of light and is only limited by scattering as well as absorption. Electronic-photonic convergence is needed for communication systems to meet the performance requirement. Hence, an increasing number of Very-Large-Scale Integration (VLSI) electronic photonic chips are going to be designed and utilized. However, packaging for the chip is one of the major challenges for optoelectronic industry to overcome due to its high cost and lack of standards.

This thesis examines the trend in semiconductor technology and also in the package performance requirement. A transceiver platform to meet the future information capacity demand is proposed by reviewing several materials and devices of current state. Lastly, the package design is demonstrated with the analysis of cost, performance, and materials.

Thesis Supervisor: Lionel C. Kimerling
Title: Thomas Lord Professor of Materials Science and Engineering

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Chapter One: Introduction

1.1 Background

As the technology node advances, transistor dimension keeps going down. The improving performance and increasing data rate of microprocessors result in a demand for large-bandwidth signal transmission to a VLSI (Very Large Scale Integration) chip[1]. However, accompanied with the decreasing feature size, interconnect performance has become a critical issue for overall system performance. Electrical interconnect through copper wire remains some issues such as power dissipation, electromagnetic interference (EMI), RC delay, and the increasing loss of energy with increasing data rate, which make it difficult to meet the high bandwidth requirement of the rapid-growing transistors speed. For signal transmitted through copper wire, $P \propto CV^2 f$. While the technology scales down, the power dissipation still grows due to the faster data transmission rate and higher interconnect density. Repeater circuitry employed for shortening the interconnect latency also contributes to the power dissipation as a trade-off between energy and delay[2]. Significant electromagnetic interference between electrical signals operated at high frequency and crosstalk limit the information density of electrical interconnects. The

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[1] A. V. Krishnamoorthy, D. A. B. Miller, *Scaling Optoelectronic-VLSI Circuits into the 21st Century: A Technology Roadmap.* IEEE JOURNAL OF SELECTED TOPICS IN QUANTUM ELECTRONICS, VOL. 2, NO. 1 , APRIL 1996

[2] M. Haurylau, G. Chen, H. Chen, J. Zhang, N. A. Nelson, D. H. Albonesi, E. G. Friedman, P. M. Fauchet. *On-Chip Optical Interconnect Roadmap: Challenges and Critical Directions.* IEEE Journal of Selected Topics in Quantum Electronics, Vol. 12, No. 6, November/December 2006

length of electrical interconnects are confined by distortion and attenuation in high speed data communication systems since these physical effects are strongly related to the frequency[3]. Photons transmitted through optical fibers are capable of reducing interconnection latency, decreasing the power dissipation, preventing interconnects from electromagnetic interference, and carrying signals with higher bandwidth in order to match transistor performance enhancement[4]. Therefore, the electronic-photonic convergence integrating optical technology with current semiconductor devices such as an electronic photonic chip has become the path to achieving system performance requirement in the future.

1.2 Trend

Technology Pushes Forward

Figure 1 shows trends in the number of transistors on chip as well as in the chip size of high performance microprocessor based on ITRS[5] (International Technology Roadmap of Semiconductor) projection[6]. It is indicated by the graph that the number of transistors will double every three years in the future while the chip size will be in a three-year cycle for each transistor generation. Since chip sizes of the same number of transistors is going to decrease during each three-year period, transistors density will be growing at the same time.

---

[3] E. Berglind, L. Thylén. *A Comparison of Dissipated Power and Signal-to-Noise Ratios in Electrical and Optical Interconnects.* JOURNAL OF LIGHTWAVE TECHNOLOGY, VOL. 17, NO. 1, JANUARY 1999

[4] M. J. Kobrinsky, B. A. Block, J.-F. Zheng, B. C. Barnett, E. Mohammed, M. Reshotko, F. Robertson, S. List, I. Young, K. Cadien. *On-Chip Optical Interconnects.* Intel Technology Journal, Vol. 8, Issue 2, 2004

[5] ITRS. *International Technology Roadmap For Semiconductors, 2006 Update,* International Technology Roadmap for Semiconductors. 2006

[6] The following projections are according to ITRS 2006 Update data

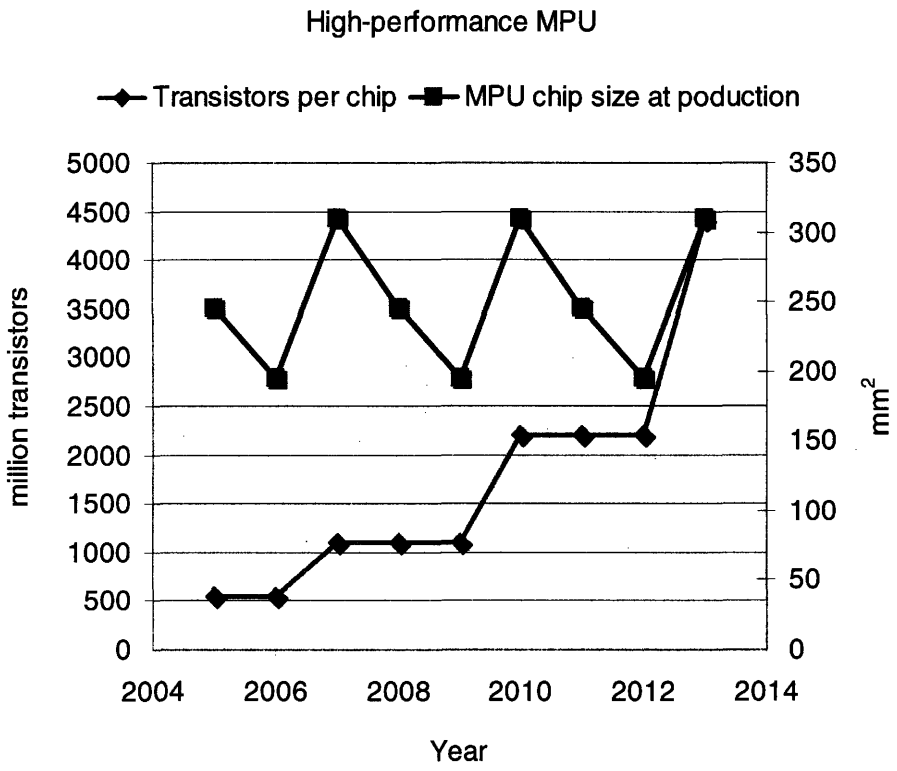

Figure 1: Transistors growth and corresponding chip size based on 2006 Update projection

Figure 2 gives a picture of the trend in transistor density which suggests that an increasing number of transistors are going to be integrated on a single chip. Therefore, enormous on-chip bandwidth as well as input/output(I/O) bandwidth will be needed in order to make full exploitation of microprocessors with high clock frequency.

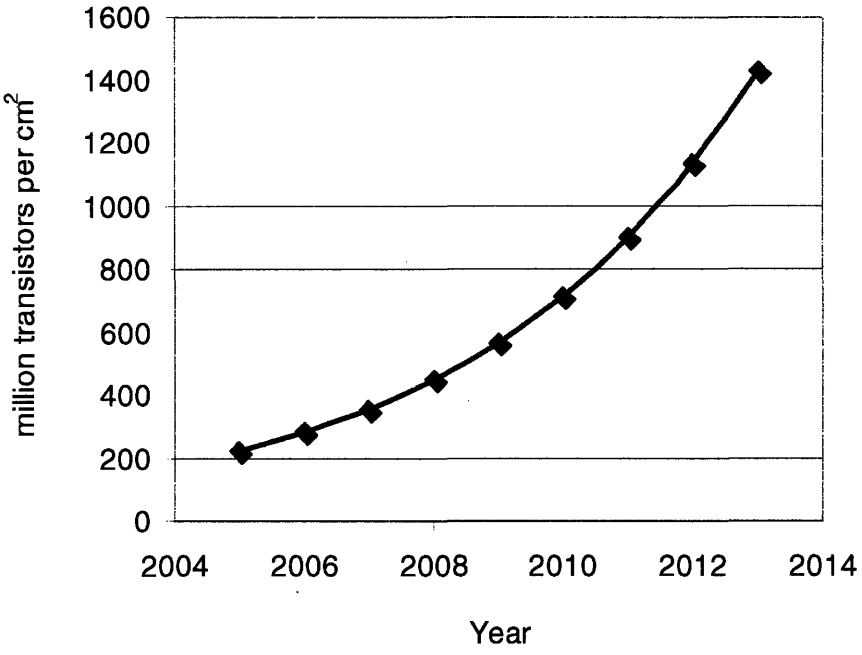

Figure 2: Trend in transistor density, as predicted by ITRS 2006 Update

Challenges

The bandwidth of input and output data transmission necessitates a huge growth as the components on a single chip doubles every 3 years. As an example of the huge bandwidth demand in the future, bandwidth per pin as well as aggregate off-chip bandwidth required will come to approximately 9.5 Gbps and 7 Tbps, respectively, in year 2010[7]. Future requirements of per-pin bandwidth, aggregate off-chip bandwidth, and the maximum number of package pin counts are shown in figure 3. Limitation comes from the slack growth in maximum number of package pin counts while I/O pins remain a constant

[7] According to ITRS data with following assumptions:
a. Only 30% of total pins are for I/O
b. Aggregate off-chip bandwidth = (Bandwidth per pin) × (I/O pin counts)
c. Only 1% of I/O pins operate at the highest frequency, 99% of them run at half of the maximum frequency

percentage of total pins. Failing to keep pace with the fast-increasing bandwidth demand may limit the advance of overall system performance.

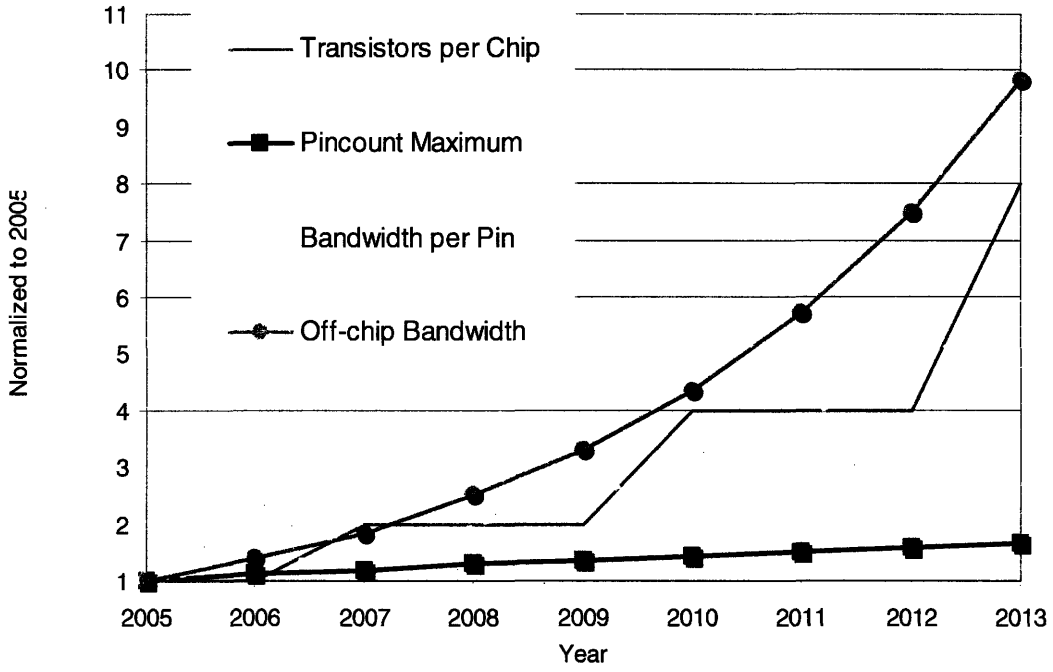

Figure 3: Requirements of aggregate off-chip bandwidth, bandwidth per pin, and maximum pin counts projected by ITRS 2006 Update

Due to the slow growth in the maximum package pin counts and the exponential increase in number of transistors, the number of pins for each transistor is falling over years. A large portion of pins on the package will be needed to provide power as the functionality of the chip improves, which is going to limit the number of pins available for input and output signaling. Simply increasing the number of pins for parallel interconnects is not sufficient for the future trend. In order to fulfill the aggregate off-chip bandwidth requirement, bandwidth per pin is projected to increase as the technology node moves

forward. Figure 3 shows that bandwidth per pin has to increase in order to compensate the decrease in number of pins per million transistors.

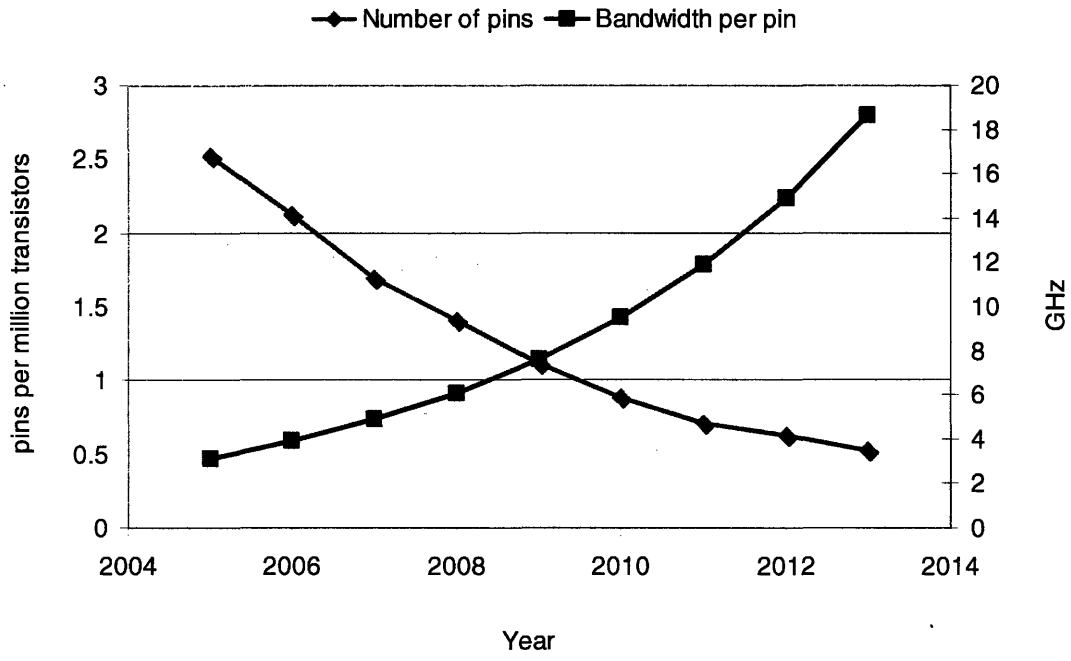

Figure 4: Number of pins per million transistors and bandwidth per pin from ITRS 2006 Update

Fiber Optics

The distance-bandwidth product of Ethernet standard over optical fiber has a trend of growing faster than that of signals traveling over twisted pairs, as indicated in figure 5. Introduction of electronic-photonic convergence into the electronic packaging has a potential of bringing out a solution to the bandwidth thirst problem. Optical fiber offers advantages over metal wire in several perspectives such as transmitting signals with relatively small loss which is almost frequency-independent, low crosstalk, short delay, and reaching even higher data rate via CWDM (Coarse Wavelength-Division Multiplexing), or DWDM (Dense Wavelength-Division Multiplexing) technology. These

technologies are able to integrate multiple channels in a single I/O pin, which save the pin counts and efficiently increase the information density.

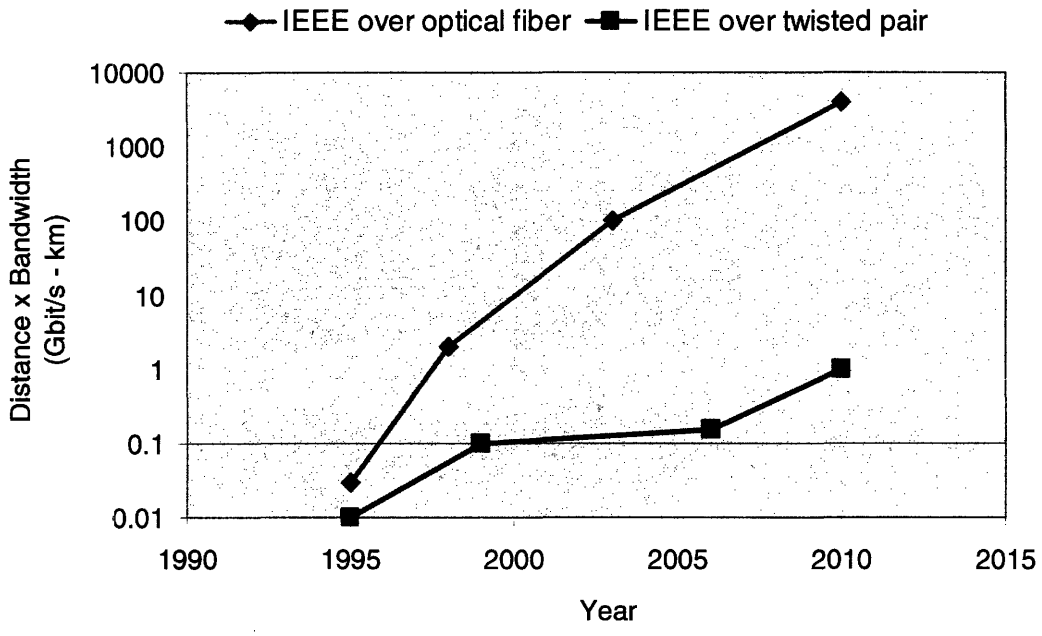

Figure 5: Roadmap in distance-bandwidth product of ethernet standard in optical fiber and in electrical interconnect[8]

1.3 Objective

Packaging, which offers a platform so that electronic-photonic components, optical devices, and electronic circuitry can be incorporated into it, is a crucial segment of optoelectronic systems. The goal of this paper is to reach a potential solution to the optoelectronic packaging with the analysis in cost, performance, and compatibility perspectives.

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[8] Wikipedia, *IEEE 802.3*. http://en.wikipedia.org/wiki/IEEE_802.3-2005.
Gigabit Ethernet. http://en.wikipedia.org/wiki/Gigabit_ethernet.
10 gigabit Ethernet. http://en.wikipedia.org/wiki/10_gigabit_Ethernet.
Fast Ethernet. http://en.wikipedia.org/wiki/Fast_Ethernet.
100 gigabit Ethernet. http://en.wikipedia.org/wiki/100_gigabit_Ethernet. Accessed on August 2007

Chapter Two: Transceiver Design[9]

2.1 Performance Requirements

Prior to come out with a packaging solution, characteristics of the transceiver inside of the package have to be defined by considering the length of link, data transmission rate, wavelength, and selecting values that meet these requirements[10]. The performance is determined by distance bandwidth product (bit rate × transmission length) and the transceiver is designed to address the following 4 different markets:

- FTTH (Fiber To The Home): Fiber length of 10 km, 1 Gbps bandwidth
- Storage Network: Fiber length of 25 m, 40 Gbps bandwidth
- Server: Fiber length of 1 m, 1000 Gbps bandwidth
- LAN (Local Area Network): Fiber length of 1 km, 10 Gbps bandwidth

2.2 Communication Wavelength

Choosing the appropriate wavelength of light propagating in the optical fiber medium is the most basic issue in system design. The performance of photons transmitting signals through optical fiber is limited by two factors: dispersion and attenuation. A performance

[9] Based on in-class design review of MIT course 3.46 Spring 2007

[10] The Microphotonics Center, Massachusetts Institute of Technology. *Communication Technology Roadmap 2005*. http://mph-roadmap.mit.edu/about_ctr/report2005/, 2005. Accessed on March, 2007

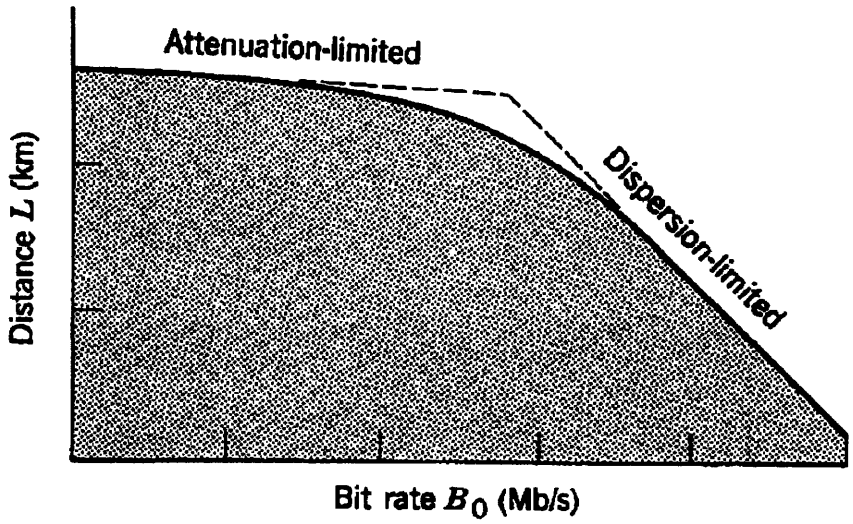

Figure 6: Figure of Merit Optimization Plot

figure of merit was formulated as (Distance)×(Bit rate). Figure 6 shows how the distance bandwidth product relates to an attenuation-limited region as well as a dispersion-limited region. To design for distance, attenuation of light will be the major concern; to design for bit rate, dispersion of light in the medium will be the limiting factor. Figure 7 shows 3

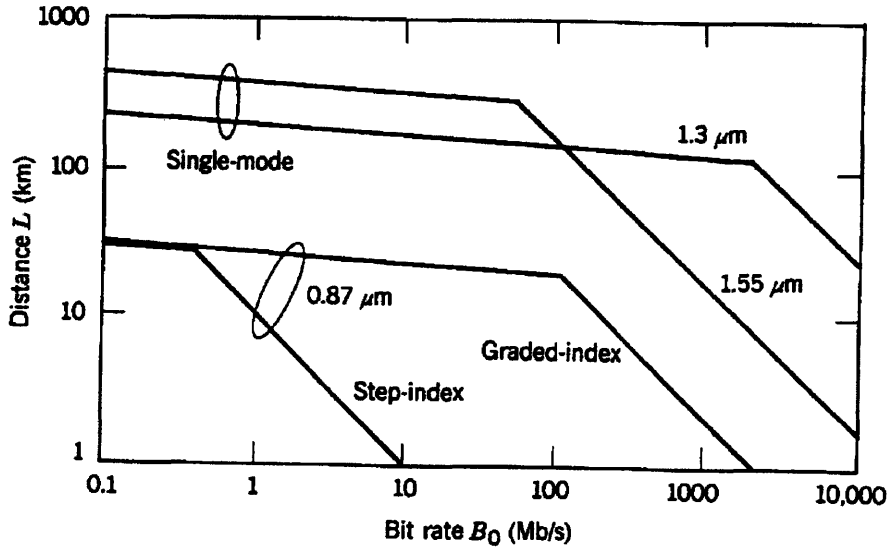

Figure 7: Attenuation and Dispersion of Light Propagation in Silica Fiber

different wavelengths of light and their bit rate distance relationship. To meet the bandwidth requirement defined in 2.1, 1.3 μm and 1.55 μm are two candidates as shown above. It is indicated in Figure 8[11] that a local minimum attenuation appears at 1.3 μm

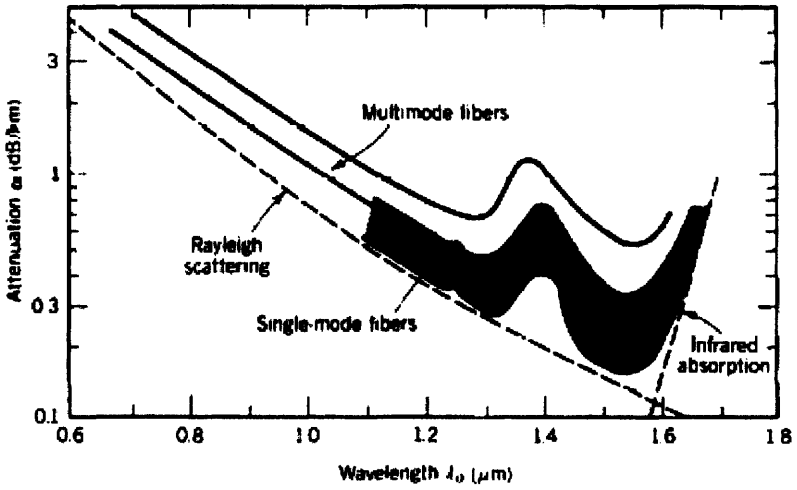

Figure 8: Ranges of attenuation coefficients of silica glass single-mode and multimode fibers

for single-mode silica fibers and an absolute minimum attenuation occurs at 1.55 μm, which make both of them suitable for long distance data transmission. A low dispersion coefficient is also required for the high data rate transmission since the desired bandwidth falls in the dispersion-limited region. Figure 9[12] shows that the dispersion coefficient in silica glass fibers varies with different wavelength. It can be seen that the dispersion coefficient comes to zero at the wavelength around 1310 nm and becomes approximately 20 ps/km-nm at the wavelength of 1.55 μm. As a result, light of 1310 nm transmitting signals through single mode silica fibers is chosen for the system since it offers a relatively low attenuation and zero dispersion.

[11] B. E.A. Saleh, M. C. Teich. *Fundamentals of Photonics*. Wiley-Interscience, 1991
[12] B. E.A. Saleh, M. C. Teich. *Fundamentals of Photonics*. Wiley-Interscience, 1991

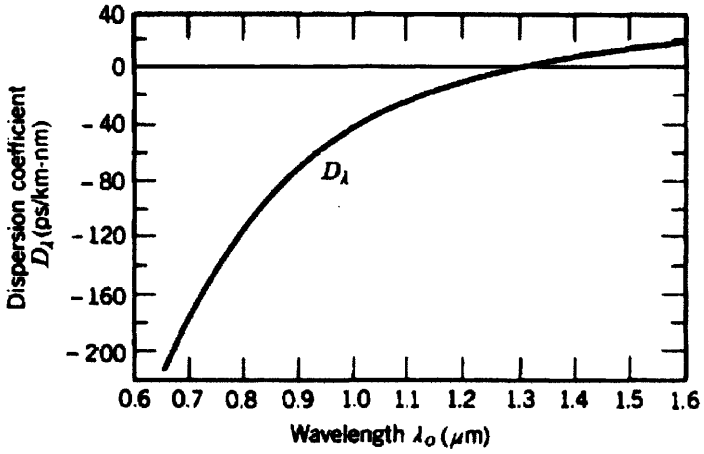

Figure 9: Dependence of dispersion coefficient and wavelength in silica glass fibers

2.3 Materials Selection and Devices

Basic components in a transceiver system are listed below:

- Laser light source and Modulator
- Photodetector
- WDM filter
- Coupler

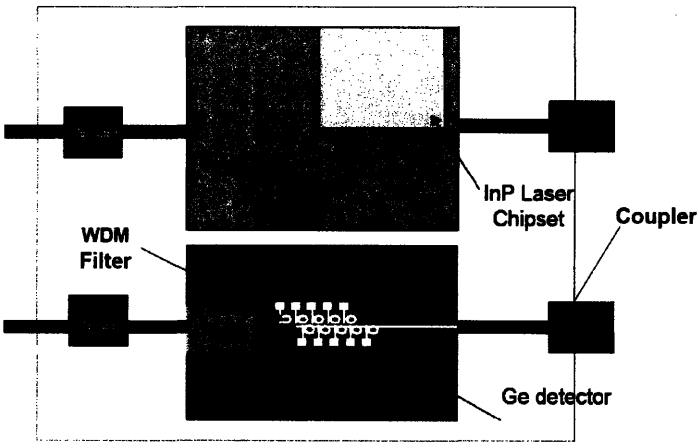

Figure 10: A Transceiver Platform

Devices to meet the performance requirement and potential materials for integration are reviewed in this section.

Laser/Modulator

A laser responsible for generation of light at a specific wavelength, which is 1310 nm here, and a modulator capable of operating signal at high data rate are required. InGaAsP (Indium Gallium Arsenide Phosphorous) is a kind of compound semiconductor material which can emit light at 1310 nm. Also, the technology of fabricating InGaAsP laser on a InP (Indium Phosphate) substrate has been proven successful and reliable[13]. A DFB (Distributed-feedback) laser structure is adopted. Light emitted from the laser can be confined to a single frequency via DFB grating and the bandgap of this compound semiconductor is tunable so that it can emit light with multiple wavelengths for WDM (Wavelength-division multiplexing) transmission. Furthermore, the DFB laser has the capability to be integrated with EAM (electroabsorption modulator). A monolithically integrated devices composed of DFB laser operating at 1310 nm and EAM has been reported by P. Gerlach et al., as shown in figure 11 [14].

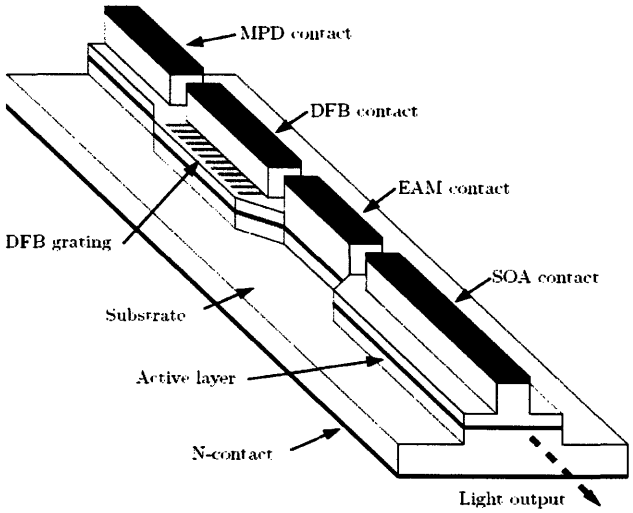

Figure 11: DFB laser integrated with EAM

[13] M. J. Speerschneider. *Technology and Policy Drivers for Standardization: Consequences for the Optical Components Industry.* Massachusetts Institute of Technology, 2004

[14] P. Gerlach, M. Peschke, T. Wenger, B. K. Saravanan, C. Hancke, S. Lorch, R. Michalzik. *Complex-coupled distributed feedback laser monolithically integrated with electroabsorption modulator and semiconductor optical amplifier at 1.3 μm wavelength.* Proc. of SPIE Vol. 6183, 2006

Photodetector

A photodetector absorbs the energy of photons and converts it to electric current. The bandgap energy of photodetector must be lower than the energy of incoming light because photons have to provide energy for electrons in conduction band so that they can transit to valence band and create electron-hole pair. In addition to the absorption coefficient, quantum efficiency is also an important parameter. It gives the the probability that absorbed photons convert to electron-hole pairs which actually go into the detector current. Quantum Efficiency $\eta = (1-R)\xi(1-e^{-\alpha d})$, where R is the reflectance, ξ is the charge collection efficiency, α represents the absorption coefficient, and d is the photodetector depletion width. The responsivity, which is the ratio of detector current to the incident optical power, of photodector can be expressed as: $R_{esp} = \eta \frac{\lambda(\mu m)}{1.24} \frac{A}{W}$.

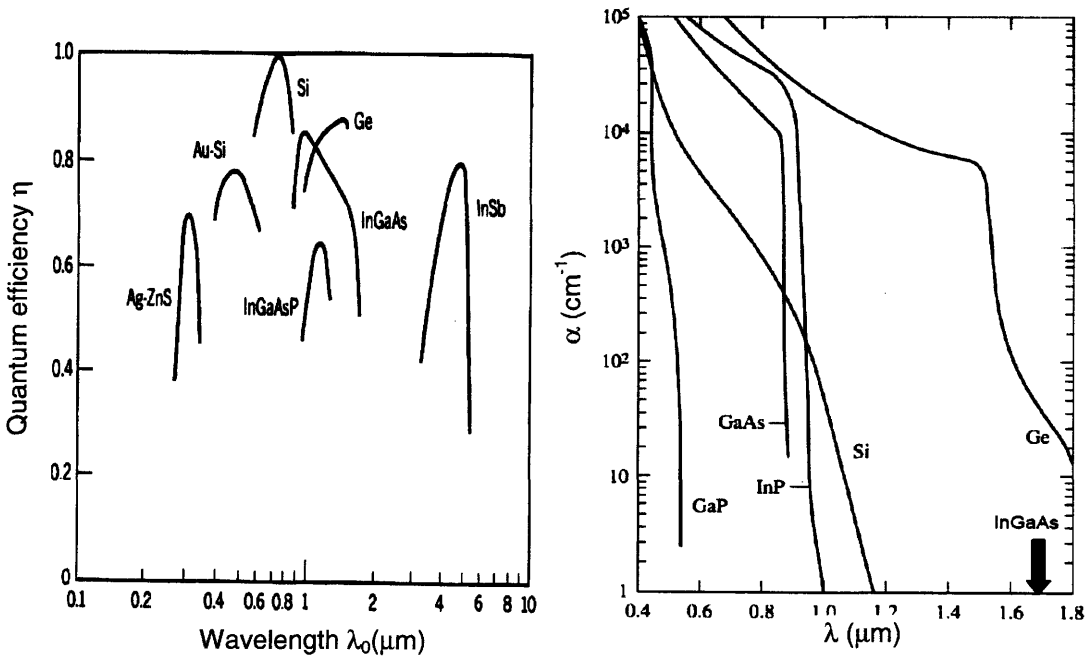

Figure 12: Quantum efficiency and absorption coefficient of semiconductor materials

According to figure 12[15], Ge has an large absorption coefficient of 10^4 cm^{-1} and a high quantum efficiency of approximately 0.9 at 1310 nm, combined with the fact that germanium can be grown on silicon substrate, which make it a proper material for the photodetector.. Considering the high bit rate requirement, PIN photodiode with short response time would be superior to the APD structure. Therefore, the device structure would be germanium on silicon PIN photodetector. Figure 13[16] is a novel design which applies tensile strain into Ge resulting in a bandgap shrinkage, which increases the hole mobility to reach a higher response rate.

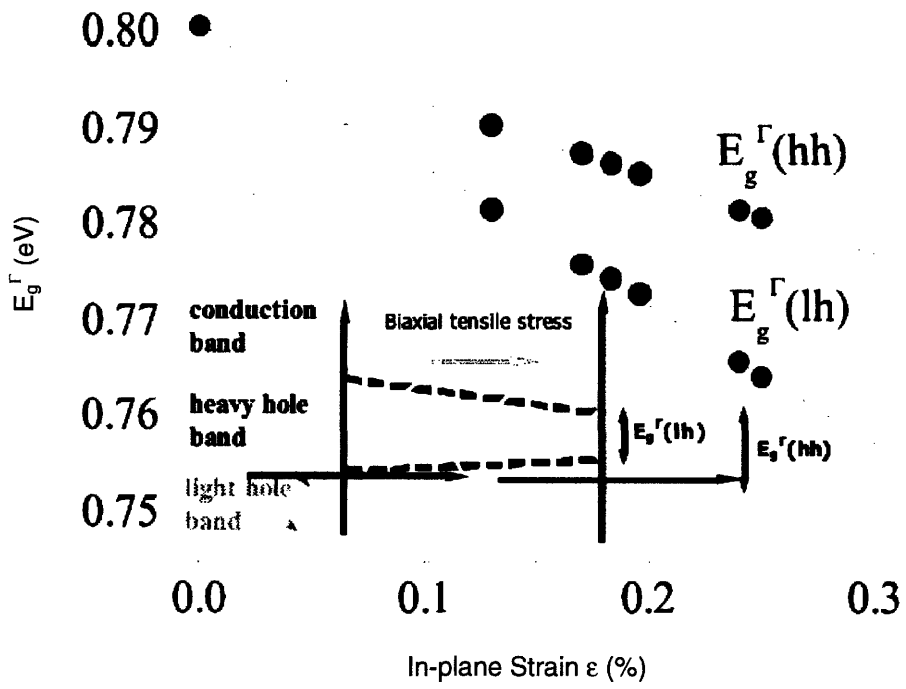

Figure 13: Tensile Strained Ge

[15] B. E.A. Saleh, M. C. Teich. *Fundamentals of Photonics*. Wiley-Interscience, 1991

[16] J. Liu, J. Michel, W. Giziewicz, D. D. Cannon, S. Jongthammanurak, D. T. Danielson, D. Pan, J. Ysaitis, K. Wada, L. C. kimerling. *A 20GHz, Tensile Strained Ge Photodetector on Si Platform with Broad Detection Spectrum for Optical Communications and On-chip Applications.* Lasers and Electro-Optics Society, The 17th Annual Meeting of the IEEE, Vol. 1, pp. 150-151, 2004

WDM filter

WDM (Wavelength-Division Multiplexing) is a technology to transmit multiple channels (wavelength) of light generated from individual laser and modulator through a single fiber or waveguide. It offers a way to multiply information capacity. A multiplexer is required to add signals of different wavelengths into the same waveguide while a demultiplexer is responsible for separating signals into multiple lights with their original wavelength and drop them to the corresponding photodetector.

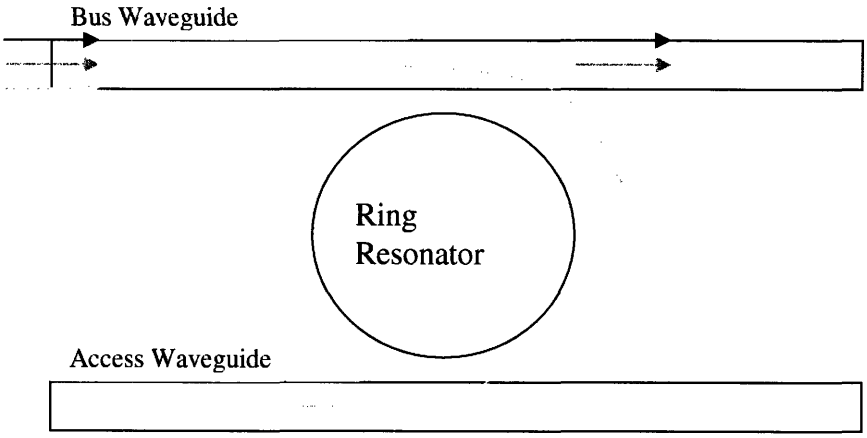

Figure 14: Ring Resonator

A ring resonator is a waveguide in the shape of a closed loop. Light from the bus waveguide will be coupled into the ring only if its wavelength meets the resonant condition and this light with certain wavelength will then be dropped to the access waveguide. The size of ring resonator is related to the FSR (Free Spectral Range) as: $r = \frac{\lambda^2}{2\pi FSR_\lambda}$, where r is the radius of the ring. The free spectral range can be determined

from the number of WDM channels and the channel spacing. Possible materials for ring resonator are SiON high refractive index waveguide[17] and III-V semiconductor[18].

Coupler

A single-mode fiber has a core about 8 μm in diameter while the cross-section area of silicon waveguide is approximately 0.1 μm^2, hence a significant power loss would occur if the light is directly transferred between optical fiber and silicon waveguide. Coupler functions as an intermediate medium which transmits the light and reduces the energy loss simultaneously. One approach is using the taper to connect optical fiber and the waveguide. The thickness of each layer is discreetly designed with corresponding index so that it is able to perform a parabolic index profile. The incident wave is guided to the bottom of the graded index layer with the highest index which is the waveguide material.

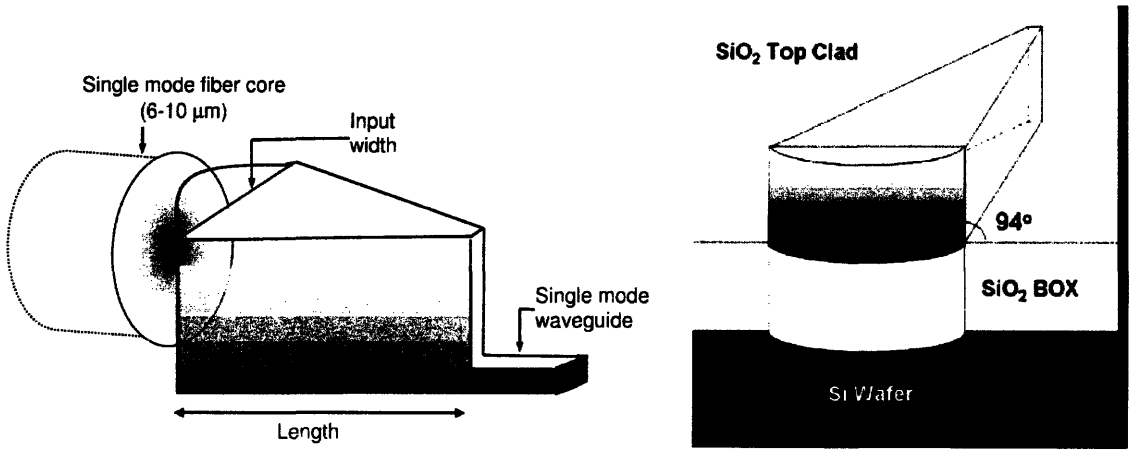

Figure 15: Taper with graded index and GRIN lensed coupler,

[17] G.-L. Bona, R. German, B. J. Offrein. *SiON high refractive-index waveguide and planar lightwave circuits*. IBM J. RES. & DEV. VOL. 47 NO. 2/3 MARCH/MAY 2003

[18] R. Grover, P. P. Absil, T. A. Ibrahim, P.-T. Ho. *III-V Semiconductor Optical Micro-Ring Resonators.* AIP Conference Proceedings, Volume 709, pp. 110-129. May 10, 2004

Figure 15[19,20] shows a taper with graded index which confines light in the vertical direction and a GRIN lensed coupler which combines a lens to help confine light horizontally. As a result, the coupling loss can be reduced down to about 0.4 dB and is independent of wavelength.

2.4 Summary

Table 1: Summary of basic transceiver characteristics

	FTTH	Storage Network	Server	LAN
Fiber Length (m)	1000	25	1	10000
Bandwidth (Gbps)	1	40	1000	10
Wavelength	Centered at 1310 nm			
Fiber	Single Mode			
Detector	Ge on Si			
Laser	InGaAsP on InP - Single Quantum Well			
Modulator	InGaAsP on InP - Multi Quantum Well			
Coupler	MIT GRIN Lensed Coupler			

Basic components of a transceiver platform have been reviewed. Materials and devices were selected in order to meet performance requirements. From the summary of transceiver characteristics shown in table 1, it is indicated that two kinds of substrates are needed for this structure – Silicon and Indium Phosphide. The silicon electronic devices such as driver and TIA are fabricated on Si substrate. InP substrate with laser, modulator, ring resonator grown on it is then bonded to the Si substrate.

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[19] V. T. Nguyen. *Efficient Power Coupling to Waveguides in High Index Contrast Systems.* MASSACHUSETTS INSTITUTE OF TECHNOLOGY, 2005

[20] R. Sun, V. Nguyen, A. Agarwal, C.-Y. Hong, J. Yasaitis, L. Kimerling, J. Michel. *High performance asymmetric graded index coupler with integrated lens for high index waveguides.* APPLIED PHYSICS LETTERS **90**, 201116. 2007

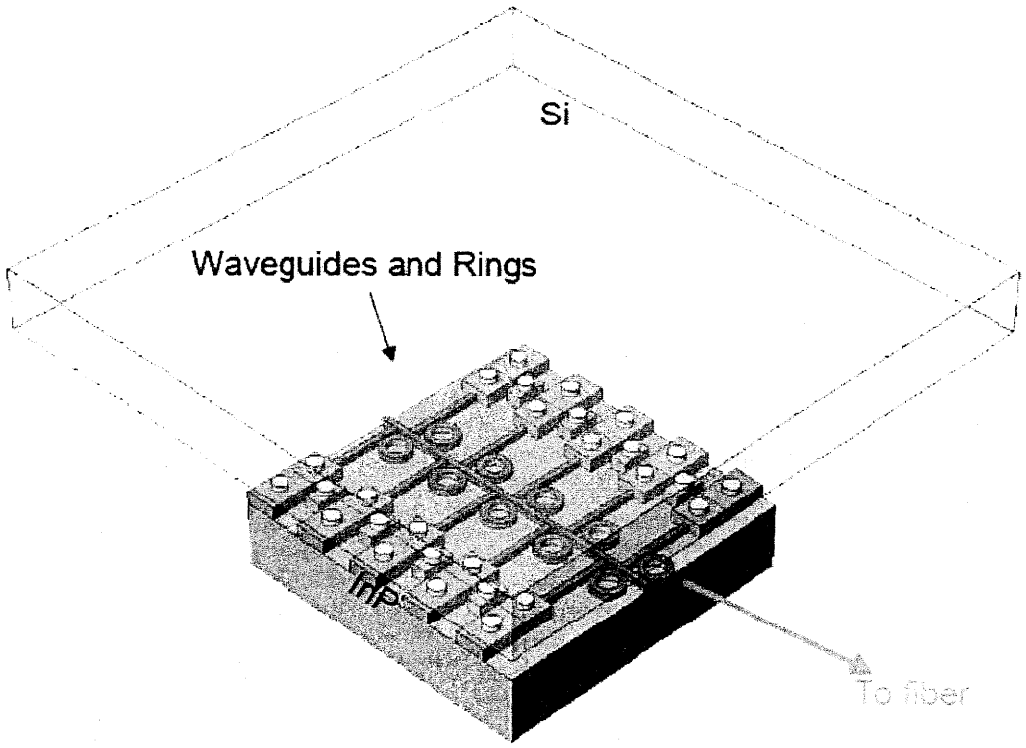

Figure 16: InP top view of the chip

Chapter Three: Package Analysis

3.1 Package Overview

In the history of microelectronic packaging, different types of packages have been designed and adopted as the technology evolves.

Dual-in-line Package and Flatpack Package

Both dual-in-line package (DIP) and flatpack package are the type of packaging technology which places its leads on edges of a rectangular housing. Electrical pins of dual-in-line package only extend from two parallel side and line in the direction perpendicular to the package. As a result, plated through holes technology is usually used to mount dual-in-line package onto printed circuit boards. Unlike dual-in-line technology, the flatpack leads coming out from each edge are in the same plane with the package and specific processing technology is required for mounting it. Therefore, the dual-in-line package which is capable of being mounted by automated operation had become the mainstream for years before the invention of surface-mount packages[21]. Figure 17[22,23] shows an example of DIP package as well as a flatpack package.

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[21] R. K. Ulrich, W. D. Brown. *Advanced Electronic Packaging*. Wiley-IEEE Press, 2006

[22] BEAM Pieces. *Electrical part packages*. http://www.solarbotics.net/library/pieces/pix/74ac139.jpg. Accessed on August 2007.

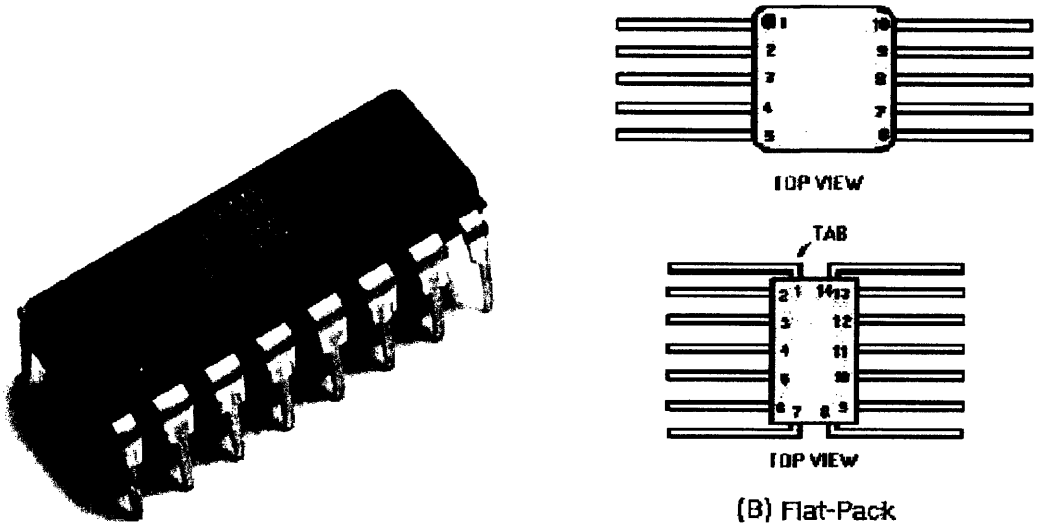


Figure 17: DIP and Flatpack package

Ball Grid Array

Solder bumps are used in ball grid array packages to transmit signals from chips to printed circuit boards. It is a surface-mount technology created in order to support the demand of high interconnects density. Solder bumps in a grid pattern can be placed over the entire surface of the package or a rectangular part of the surface is left unoccupied. Balls with exact amount of solder required for mounting make BGA superior to pin-grid array packages and DIP in that the problem of bridging between pins with small pitches can be avoided. Ball grid array package provides large pin count capability, small footprint, and faster speed due to the shorter connection length between chips and printed circuit boards. A reflow oven is used to melt the self-align solder balls and then mount

[23] Electrical Engineering Training Series. *IC PACKAGE LEAD IDENTIFICATION (NUMBERING) – Continued.* http://www.tpub.com/content/neets/14186/css/14186_42.htm. Accessed on August 2007.

the BGA package onto printed circuit board[24]. A picture of BGA package is shown in figure 18[25].

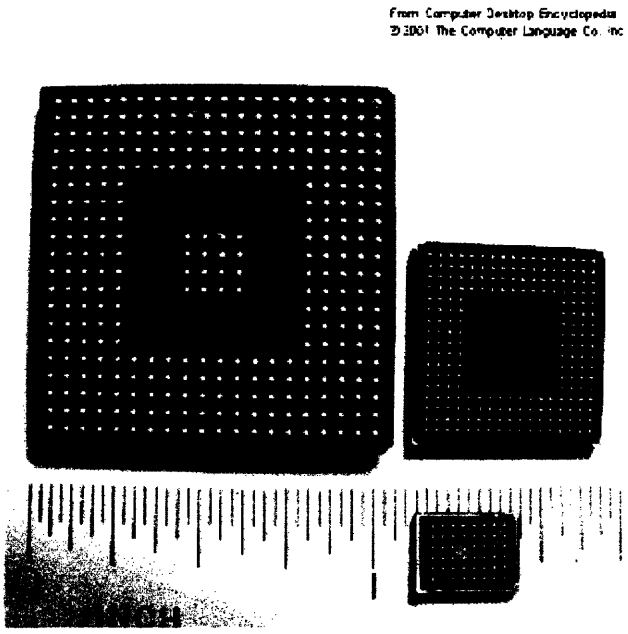


Figure 18: BGA package

Instead of using wire bonds connecting the die to the substrate, Flip-Chip technology adopts the concept of area array interconnect and spread bond pads over the entire surface of chips for solder bump attach. In wire bonding, connectors extend from edges of the chip and thus require additional space to accommodate these wires. With the use of entire chip surface, flip-chip bonding can significantly reduce the footprint of the package. The reduction of the interconnect length significantly also decreases inductance and capacitance of electrical signal transmission and therefore enhances the performance.

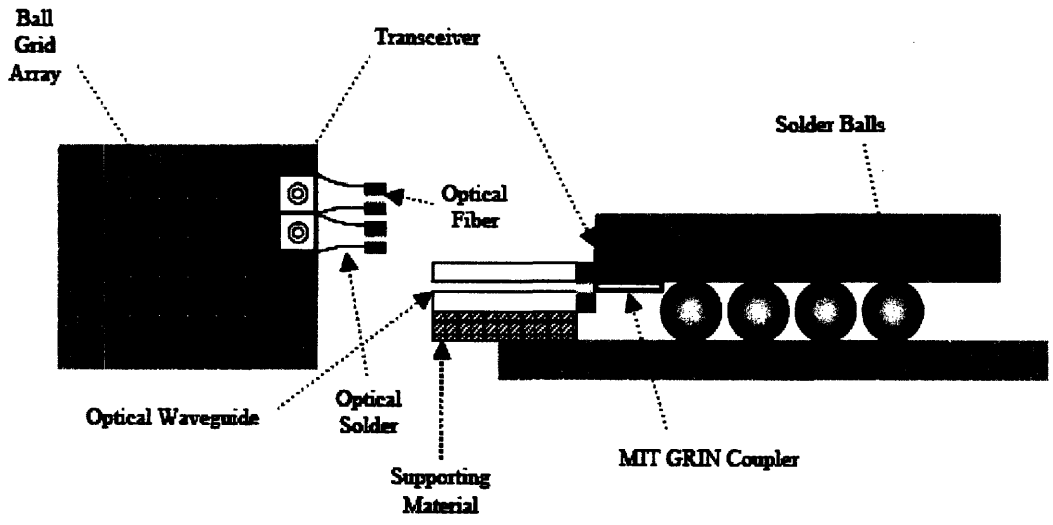
[24] Siliconfareast.com. *Ball Grid Array (BGA).* http://www.siliconfareast.com/bga.htm. Accessed on August 2007

[25] Answer.com. *ball grid array.* http://www.answers.com/topic/bga?cat=technology . Accessed on August 2007

3.2 Package Attributes

Structure

In order to provide data transmission for electronic circuitry and photonic devices on the chip, optical pins as well as electrical pins are implemented on a single package. For electrical signals, a flip-chip ball grid array is used for the connection between printed circuit board and the package. Single-mode optical fibers that can transmit light at the wavelength of 1310 nm exit on edges of the package. The structure of this electronic photonic package is illustrated in figure 19.



	μm
Fiber Core Diameter	8~10
Fiber Cladding Diameter	125
Coupler Height	8~10
Solder Bump Thickness	300

Figure 19: Illustration of the Optoelectronic Package

Certain numbers of transmitter and receiver set are installed around the periphery of the package. Light originated from the edge-emitting laser will be guided into optical fiber

through MIT GRIN coupler described in section 2.3. The optical signal is then transmitted to the waveguides on the printed circuit board through optical pins of the package. For a chip with edge length of 2 cm and single-mode fibers with 250 μm pitch, the maximum number of optical pins can be placed at each side is 80. Considering the high bit rate of optical transmission, the package is capable of scaling to future package design by which the enormous I/O bandwidth is needed.

Optical Solder

Optical solders are required to provide connection between chips and single-mode silica fibers on the package. In order to successfully transfer the light coming through the GRIN coupler, these connectors are needed to be transparent at the wavelength of 1310 nm. The refractive index of the optical solder material at communication wavelength is expected to be around 1.5 which is equal to the refractive index of the single–mode silica fiber at 1310 nm. Polymer materials with low glass-transition temperature, which is about 200°C, have the potential to be ideal for this application since they can be processed with solder bumping at the same time.

Table 2: Optical Solder Material

Optical Solder Material Characteristics
Polymer with low glass-transition temperature
Transparent at the wavelength of 1310 nm
Refractive Index is equal or slightly above 1.5

When heated above its glass-transition temperature, this polymer layer, as shown in figure 20, is able to flow toward optical fibers and then attach on them. Therefore, the

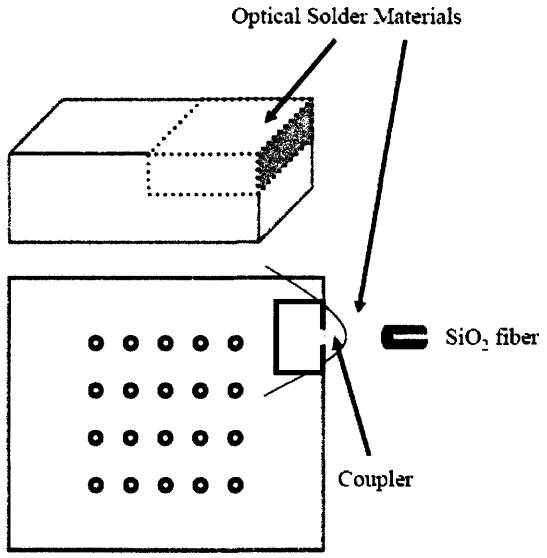


Figure 20: Optical Solder Material

wave mode which propagates through the coupler tip fills the optical solder and being transmitted into optical fibers. Potential materials are fluorinated polyimide reported by S. Ando[26] which has high transparency at 1.31 μm and a glass-transition temperature of 240°C. Kapton®[27] polyimide film produced by DuPont™ is a commercial optical polymer which might be ideal for optical solder. Another optical solder material candidate is UV curable polymer. A thin film layer of this kind of polymer is applied at the connection region then the optical path can be defined by UV light curing. If the low glass-transition polymer and solder bump are capable of being processed simultaneously,

[26] S. Ando. *Optical Properties of Fluorinated Polyimides and Their Applications to Optical Components and Waveguide Circuits*. Journal of Photopolymer Science and Technology, Vol. 17, Number 2, 2004 pp. 219-232

[27] DuPont. *Kapton® Polyimide Film.* http://www2.dupont.com/Kapton/en_US/. Accessed on July 2007

which means that these 2 kinds of material are compatible under physics concern, they may save the cost of an additional processing step.

Board Modification

The optoelectronic package requires a printed circuit board that allows both optical and electrical signals transmission. A waveguide layer on which optical signals at the center wavelength of 1310 nm can be efficiently transmitted is going to be needed on the printed circuit board. Figure 21 is an illustration of how the board being modified to accommodate the optoelectronic package.

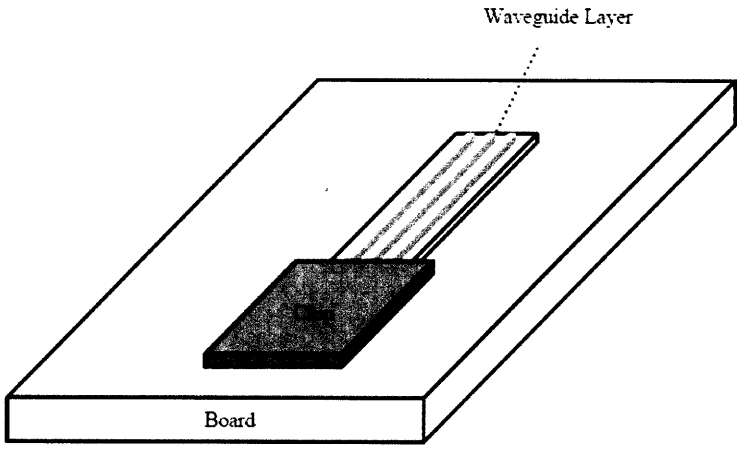


Figure 21: Board modification

3.3 Package Analysis

Performance: Bandwidth

Due to differences in pitch as well as in bit rate per pin, bandwidth density is used to analyze the performance of I/O pins. Figure 22 shows the minimum number of optical channels required per pin for the package to meet or exceed the bandwidth density of electrical pins[28]. Therefore, optical data transmission using multiplexing technology such as CWDM and DWDM can significantly outpace electrical signaling in information capacity.

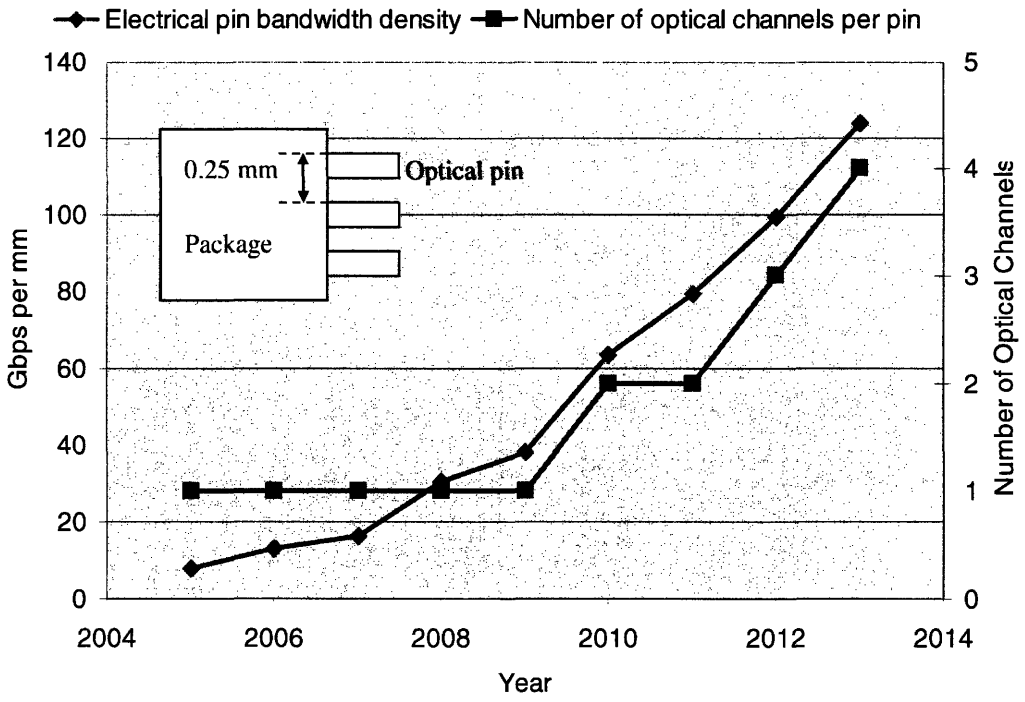


Figure 22: Minimum number of optical channels per pin to meet the bandwidth density projected by ITRS 2006 Update

[28] Assumptions:

- Optical per-pin bandwidth is fixed at 10 Gbps
- Optical pin pitch: 0.25 mm, liner array of single-mode fibers at edge
- Optical channel counts is variable
- Electrical pin pitch: FBGA ball pitch projected by ITRS

Figure 23 shows the optical pin counts needed to meet the overall off-chip bandwidth requirement projected by ITRS for high-performance package. It is under the circumstance that all of the I/O pins, which mean 30% of total pins, are substituted with optical pins. The number of pins varies with different multiplexing technologies. These results of calculation were based on the assumption that optical bandwidth per channel is fixed at 10 Gbps and the pitch is 0.25 mm. Improving the bit rate of single channel may further reduce the number of optical pins.

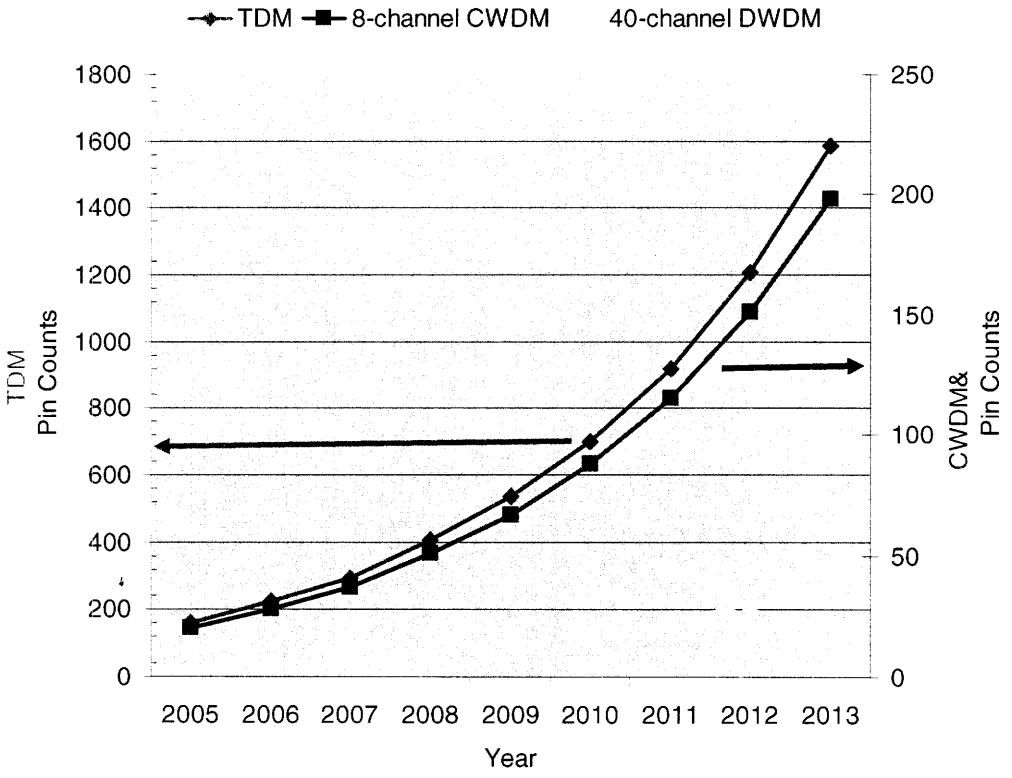


Figure 23: Pin counts for TDM, CWDM, and DWDM to meet the aggregate off-chip bandwidth projected by ITRS 2006 Update

Power Dissipation

There are several sources of the energy loss for a light coming out from the laser, transmitted through the waveguide, and then received by the photodetector. The biggest contributor to power loss is the slope efficiency of laser light source, which is the ratio of output power to pump power. Figure 24 shows the power dissipated from laser slope efficiency and power dissipation and from other sources as a function of length[29]. As an

Table 3: Sources of loss

Transmission Loss	0.2	dB/cm
Coupling Loss	0.6	dB
Laser Slope efficiency	50%	
P_{min}[30] at receiver	0.025	mW

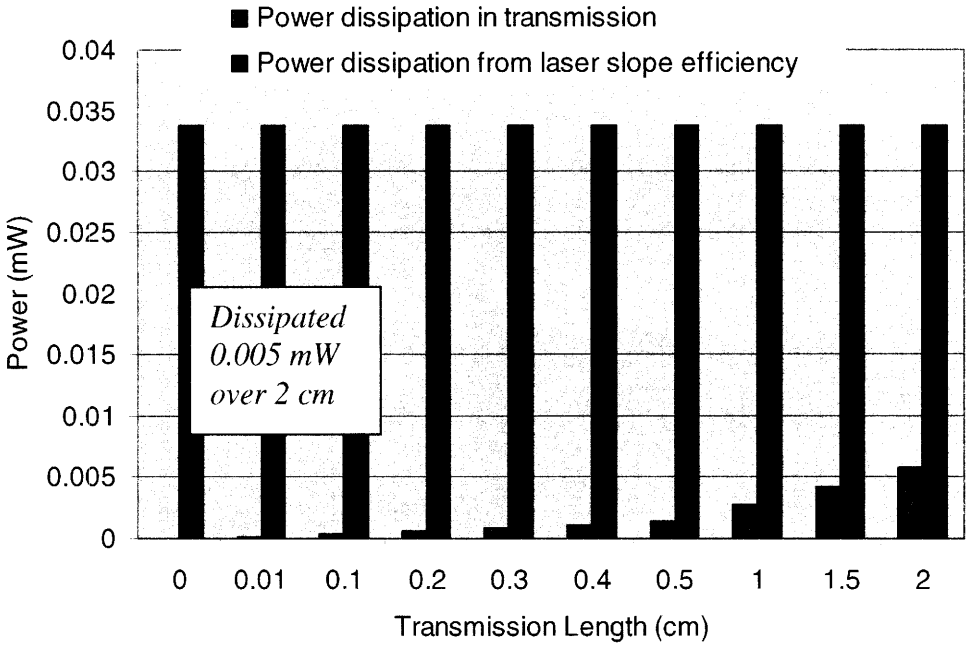


Figure 24: Power dissipation from laser slope efficiency and from other sources as a function of transmission length

[29] The power dissipation due to laser slope efficiency is for laser operated at 10 GHz; The power dissipated in transmission is assumed to be the loss for point-to-point interconnect.

[30] Minimum power required for a signal to be detected by a 10 GHz receiver with the signal-to-noise ratio of 20 and 10^{-12} BER (bit error rate).

example, about 85% of the power loss is generated at the laser source for a signal propagating 2 cm. Figure 25 is the power loss of an electrical signal path. In contrast to optical interconnects, the power dissipation of electrical wires is greatly dependent on the length and width of interconnection. The power dissipated in electrical interconnect is much greater than that in optical interconnect as labeled in figure 24 and figure 25. Repeaters contribute up to 40% the dissipated power depending on the interconnect width. However, the insertion of repeaters is inevitable because it is able to improve the performance in delay, transition time, and crosstalk noise. As a result, optical data transmission is superior to electrical signal transmitted through metal wire in that it provides lower power dissipation and isn't limited by propagation distance.

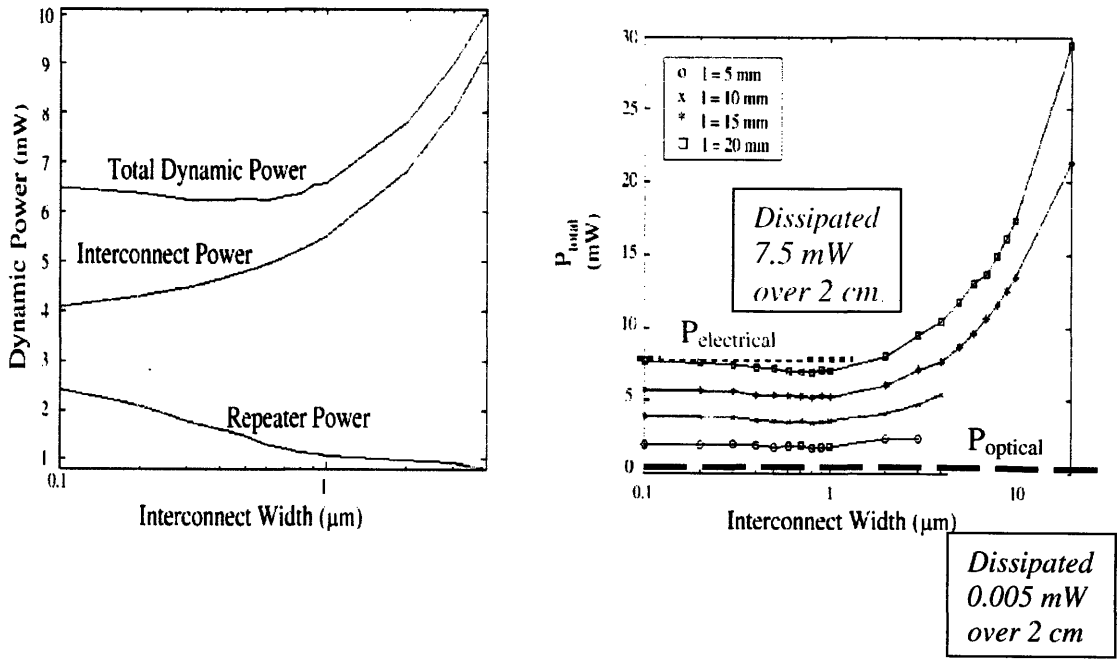


Figure 25: Dynamic power loss as a function of interconnect width, length = 20 mm and total power dissipation as a function of interconnect width[31]

[31] M. A. El-Moursy. E. G. Friedman. *Optimum Wire Sizing of RLC Interconnect with Repeaters.* INTEGRATION, the VLSI Journal 38, 2004, pp. 205-225

Cost

Package cost is estimated as: (Per-pin cost) × (Pin count maximum)

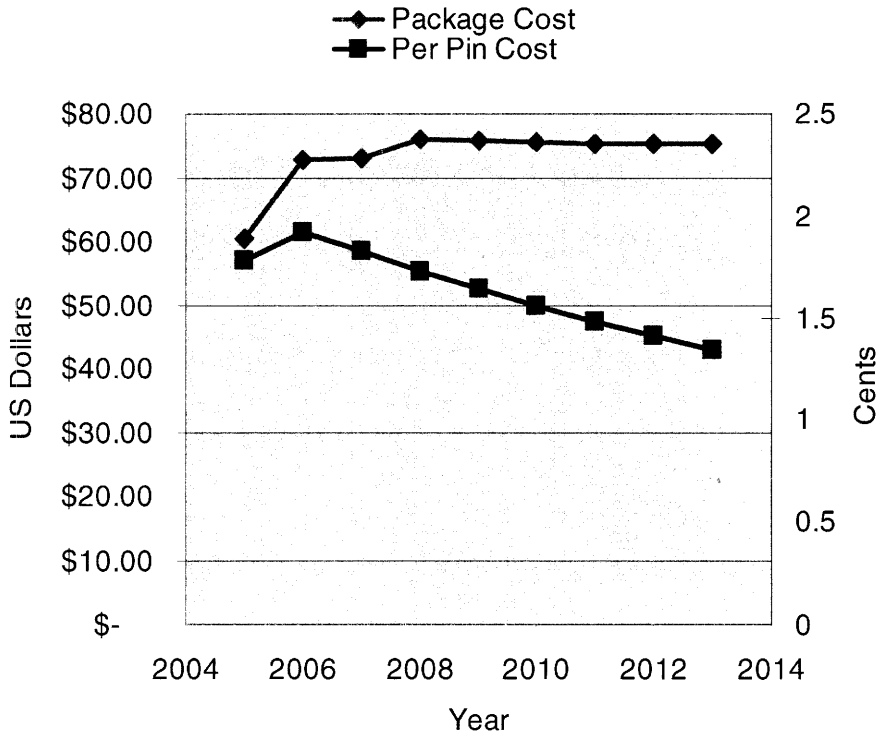


Figure 26: Per-pin cost and Package cost projected by ITRS 2006 Update

According to figure 26, the cost per I/O pin is expected to fall at a steady rate and approach one cent per pin while the growth of package cost is going to be flat after year 2008. The replacement of electrical pins with optical pins in the optoelectronic package will have to provide a competitive cost in order to meet the goal projected by ITRS. The goal is to hold package cost as projected by ITRS 2006 Update. Consequently, 30% of the package cost, which represent the cost of I/O pins, is for the implementation of optical pins. The analysis is trying to find out how much bandwidth optical pins can offer

under the constant package cost or how much cost the package needs for the same data rate Cents per Gbps of bandwidth is used for evaluating cost of the optoelectronic package. The aggregate bandwidth has to be sufficient for total off-chip bandwidth requirement projected by ITRS. Therefore, the number of I/O pins is required to be even with or larger than those indicated in figure 23.

Table 4[32]: BGA cost data for 2 kinds of BGA products

	BGA-S	**BGA-S+**
Number of Units Produced	50	10
Selling Price	$1,300.00	$3,200.00
Direct labor cost	$120.00	$300.00
Direct material cost	$500.00	$1,200.00
Direct labor hours per unit	$4.00	$10.00
Cost per direct labor hour	$130.00	$130.00
Cost per unit	$22.80	$280.00
Material Cost %	*43.86%*	*42.86%*

Elements contribute to the total cost of a ball grid array package are displayed in Table 4. BGA-S and BGA-S+ represent two different package products. However, material cost comprises nearly the same percentage of the aggregate cost in both products. Consequently, it is assumed that material cost contains certain percentage of the optoelectronic package cost in order to estimate cost per optical pin. Since package cost is formulated as: (Per-pin cost) × (Pin counts), cost per optical pin can be obtained from (Material cost per optical pin) / (Materials cost %). For a 1 cm long optical pin which is made of a $4.75-per-meter single mode fiber[33], the material cost is 4.75 cents per pin.

[32] R. K. Ulrich, W. D. Brown. *Advanced Electronic Packaging.* Wiley-IEEE Press; 2 edition ,2006
[33] THORLABS. *1060XP Singlemode Optical Fiber, 1060-1600nm, X-High Performance.* http://www.thorlabs.com/thorProduct.cfm?partNumber=1060XP. Accessed on August 2007.

Figure 27[34] provides a cost breakdown for the optoelectronic device which shows that

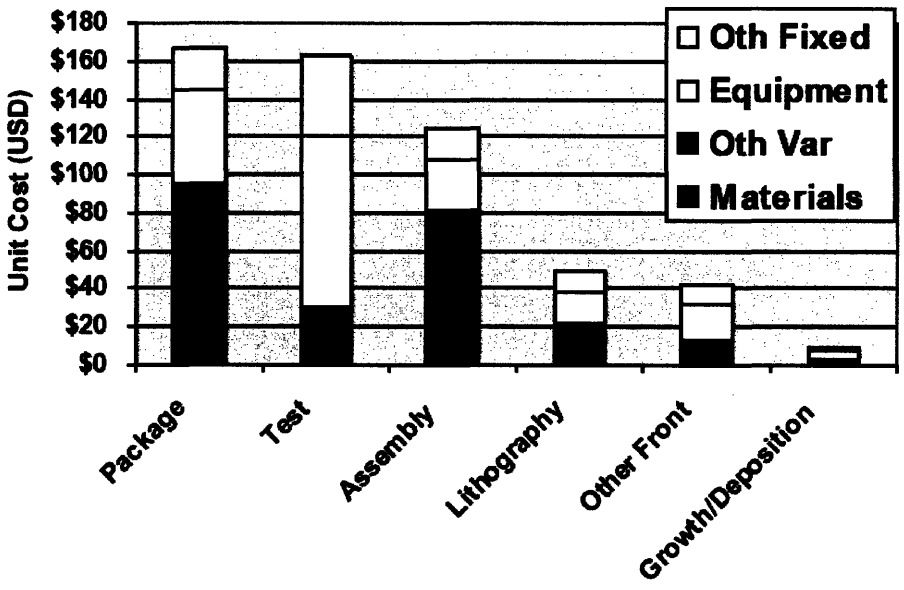


Figure 27: Cost breakdown for an integrated device

material cost comprises about 35% of package cost. Therefore, the cost of an optical pin can be calculated by: (4.75 cents per pin) / (35%), which is equal to 14 cents. Figure 28 shows cost per Gbps for different numbers of channels per pin and compares them with the ITRS projected value. Optical pins are able to offer lower cost per Gbps with multiple channels transmitted through a single pin. Channel counts have to increasing with the growing bandwidth requirement. The number of optical pins available is also indicated in the figure, which is sufficient for CWDM as well as DWDM to meet aggregate off-chip bandwidth demand.

[34] E. R. H. Fuchs, R. E. Kirchain. *Changing Paths: The Impact of Manufacturing Offshore on Technology Development Incentives in the Optoelectronics Industry.* http://web.mit.edu/erhf/www/Fuchs_ChangingPaths.pdf. Accessed on August 2007

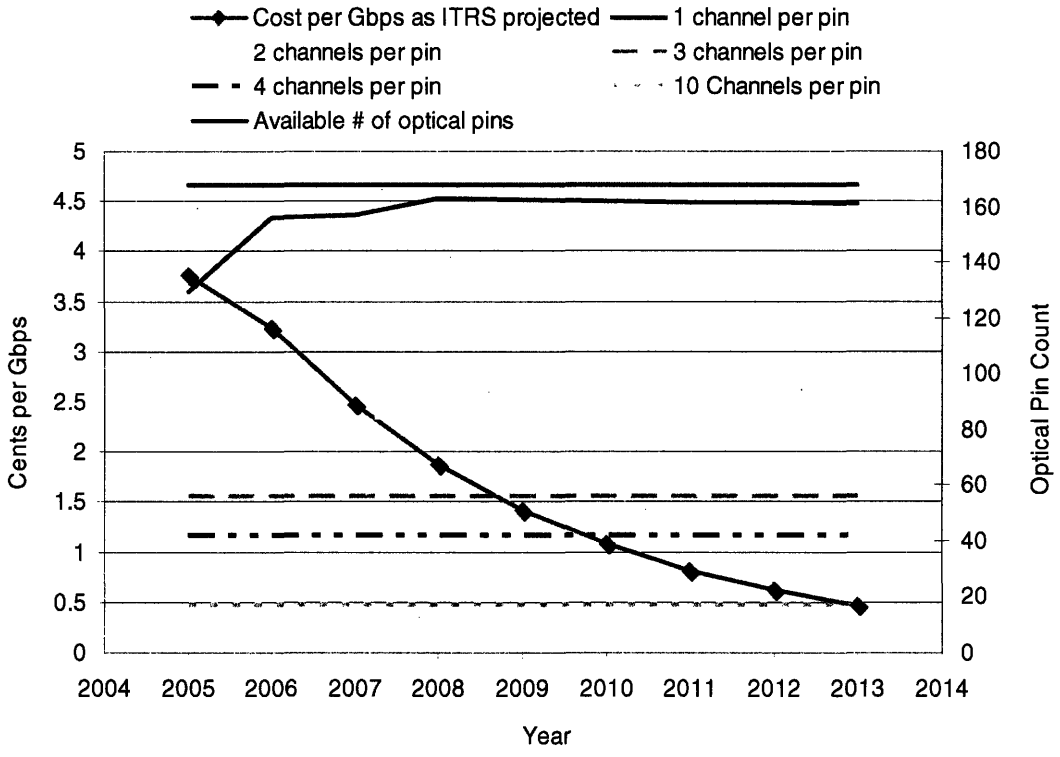


Figure 28: Comparison of cost per Gbps between optical pins and ITRS projection

As a result, transmitting multiple channels of light through each optical pin is the way to reduce cost per bandwidth so that it can be cost-effective compared with electrical I/O.

Chapter Four: Summary

4.1 Optoelectronic Packaging

A packaging solution for VLSI electronic photonic chips is proposed. Ball grid array for electrical interconnect is placed at the center of this package while single-mode optical fibers for optical signal transmission are installed around the edge. The photon transmission is horizontal since due to the use of edge emitting laser. Light is propagating in the direction parallel to the surface of printed circuit board. As a result, no mirror is required in this electronic photonic package design. For connecters between chips and packages, flip-chip bonding is adopted for electrical interconnect while optical solders are used to transfer light wave coming out from chips into single-mode fibers. An optical waveguide layer, which is responsible for optical signal transmission, is incorporated into printed circuit board. Input and output pin counts in can be saved using wavelength-division multiplexing technology. In addition to the high bandwidth density, optical interconnects provides advantages in performance such as lowering power dissipation. Future needs for off-chip bandwidth are projected according to ITRS data; it is essential to meet this demand so that the advance of overall system performance won't be restricted. Electrical interconnect through copper wire is reaching the limit and being costly to have further improvement. The electronic photonic packaging is capable of offering a solution when electronic interconnect cannot meet these requirements.

Table 5: MIT Optoelectronic Packaging for Year 2013

MIT Package 2013					
Chip Size	2cm × 2cm				
	BGA	**Electrical Power**	**Electrical I/O**	**Optical I/O**	**Optical pins per Edge**
Number of Pins	5600	3920	1680	320	80
Number of Channels per Pin	N/A	N/A	1	*CWDM*	*DWDM*
				10	40
Bandwidth per Pin (Gbps)	N/A	N/A	10	100	400

Total Bandwidth (Tbps)		
Electrical I/O		16.8
Optical I/O	*CWDM*	32
	DWDM	128

Table 5 is a summary of the packaging for electronic photonic chips in 2013. Optical I/O shows great performance in terms of overall bandwidth. CWDM supports a data rate of 32 Tbps while DWDM offers an even higher one at 128 Tbps. Both of CWDM and DWDM technologies outperform the electrical I/O which has a total bandwidth of 16.8 Tbps. In the cost point of view, running multiple channels per optical pin is more effective. Figure 29 shows the number of optical channels per pin required to provide a lower cost-per-Gbps than that of electrical pins. In order to convert electrical I/O into optical pins, CWDM and DWDM are essential for the optical signal transmission. Although using optical interconnect can reduce the cost for each Gbps, there are some trade-offs such as reliability and yield. In optoelectronic packaging, thermal control is highly required since the device's sensitivity to temperature may affect its performance. For electronic segment, the thermal management is mainly for reliability issue. Accurate alignment of laser light source is also needed to maintain the performance under all circumstances.

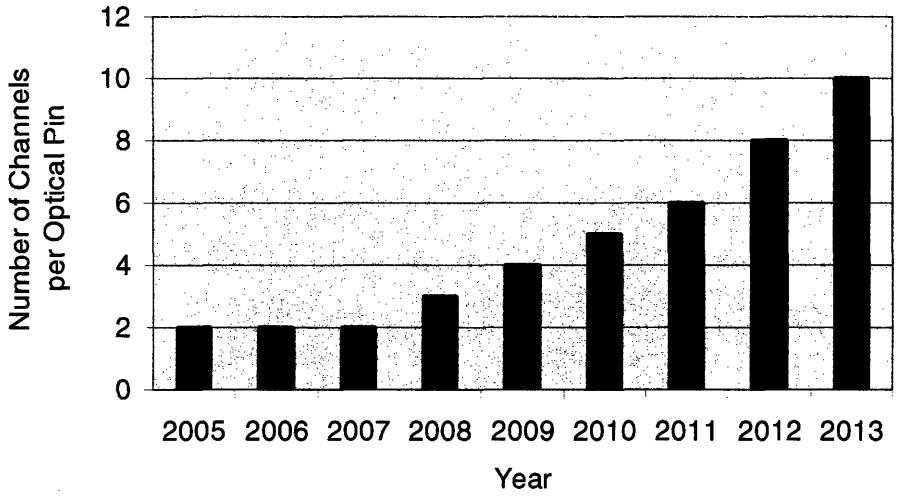


Figure 29: Minimum number of channels per optical pin in order to have lower cost-per-Gbps than that of electrical I/O

4.2 Future Research & Discussions

Increasing number of functions on a single chip results in the growing demand for power. The number of signaling pins is assumed to be 30% of total pins here. However, it is possible to become less than the current percentage in the future. If all of I/O pins are substituted with optical pins, there is a better chance for electronic photonic packages being widely adopted. The reason is that every electrical pin on the package can be used for power supply in order to support the large amount of devices on chips. Another issue is power dissipation. Since laser slope efficiency is dominating the power dissipation of optical interconnect, the future research should be addressed on lowering the energy loss from laser.

In terms of bandwidth density, the concept of multi-layer fiber ribbons has the potential to data rate per unit length. Packaging design reported here uses a single layer of optical pins, which means that there is only one single-mode fiber in vertical direction. Multi-layer fiber ribbons enable each optical solder connecting to more than one optical pin. Therefore, the bandwidth between each pitch is multiplied. Bandwidth density, which is data rate divided by pin pitch, is then increased.

The simultaneous processing of solder bumps and optical solders is worth a detail study considering their physics condition as well as processing compatibility. Instead of using polymer material such as polyimide, UV curable polymer is another option. Connectors are defined by UV light on a film of UV curable polymer grown on the bonding area.